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Review:

A review of automatic schematic generation techniques and their application to printed circuit boards*#

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Abstract: The printed circuit board (PCB) stands as the cornerstone of electronic equipment, with its schematic holding paramount importance for system performance and reliability. In light of the pervasive use of electronic devices in society, concerns regarding maintenance, safety, backdoors, and other latent issues have garnered significant attention. Automatic schematic generation (ASG), with its distinct capability for generating circuit schematics autonomously, not only plays a pivotal role in electronic design automation (EDA) but also aids in deciphering the fundamental principles of PCB equipment to effectively address these underlying issues. However, constrained by the increasingly sophisticated manufacturing processes of PCBs and the inherent legal and ethical controversies surrounding reverse engineering, the development of related technologies faces notable bottlenecks. To break through technical barriers and advance technological progress, this paper comprehensively combs through the existing ASG, offers in-depth description of the core algorithms of the technology—layout and routing, and for the application of the technology in PCB reverse engineering, analyzes in detail the current challenges and the faced problems. Around these challenges, feasible solutions are discussed in this paper, with the aims of promoting the research of automatic PCB schematic generation technology and contributing new strength to EDA and PCB reverse engineering automation.

Key words: Automatic schematic generation; Layout; Routing; Printed circuit board; Reverse engineering; Automation

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1 Introduction

The rapid advancement of electronic information technology has rendered electronic devices an essential infrastructure in contemporary society, which greatly promotes the facilitation of life and work. In this development process, the printed circuit board (PCB) plays a pivotal role. As the "nervous system" of electronic devices, it is the carrier of circuits, providing a foundation for the realization of device functions.

However, as electronic technology progresses and equipment functions become more complex, PCBs face new challenges such as potential hardware Trojan insertions, intellectual property rights verification, and the maintenance of older equipment (Rematska and Bourbakis, 2016; Botero et al., 2020). Therefore, conducting reverse engineering research on PCBs to accurately reconstruct their original circuit diagrams has become a key strategy to tackle these challenges. Through reverse engineering, designers can analyze circuit structures,

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optimize design schemes, and ultimately enhance the performance and safety of electronic devices.

In PCB reverse engineering, schematic generation stands out as a critical phase. Serving as a visual representation of the circuit, the schematic illustrates the interconnections among electronic components. It not only forms the foundation for understanding and analyzing circuits, but also serves as a valuable guide for circuit design and optimization (Yang et al., 2024). However, the complexity and time-consuming nature of this process should not be underestimated, especially when dealing with the large-scale, high-density PCBs. Manual generation of schematic diagrams becomes notably challenging in such scenarios. Therefore, the study of automatic schematic generation (ASG) is not only an important prerequisite to promote the automation of PCB reverse engineering, but also an important technical demand to enhance the potential safety of electronic devices.

Despite the strides made in research on ASG over the past decades, the extensive adoption of this technology in the realm of PCBs is hindered by the complex and irregular nature of PCB schematic structures, leading to various challenges. To tackle these challenges and promote the extensive adoption of ASG in PCBs, this paper provides a review of the current research situation, fundamental procedures, and prevalent algorithms of ASG. Building upon this foundation, the paper further discusses the specific difficulties of ASG in PCB reverse engineering, and analyzes the possible solutions. The purpose of this research is to promote the further development of ASG in PCB reverse engineering and provide technical support for the application expansion and security of PCB electronic products.

2 Overview of ASG

The technology of ASG holds a significant position in the realm of PCB reverse engineering. This section first introduces the basic concepts of ASG, including traditional forms of schematic generation and basic methods of ASG. Subsequently, the current situation of ASG is briefly analyzed, and the main classifications of ASG are summarized from the perspective of different circuit forms. Finally, the fundamental process of ASG is briefly introduced.

2.1 Basic concepts

Schematic diagrams, as a graphical carrier describing the connection relationship between electronic components, are the cornerstone for in-depth understanding and analysis of circuits (Stok and Koster, 1989). Traditionally, the schematic generation process has been predominantly manual, relying on the designer's expertise and meticulous manual interventions. Leveraging advanced electronic design automation (EDA) tools such as Altium Designer and an integrated synthesis environment (ISE) for inputting netlists and component details, a preliminary graphical depiction of components is crafted, followed by a step-by-step manual refinement of circuit layouts and component interconnections. This process is cumbersome and time-consuming, ranging from a few weeks to a few months, making it challenging to adapt to the increasing complexity and timeliness requirements of modern electronic devices.

Therefore, the research and implementation of ASG are of paramount importance. This technology endeavors to enhance the efficiency and precision of schematic generation without human intervention, employing automated layout and routing algorithms to construct circuit configurations that align with the design requisites, ensuring precise component interconnections (Jehng et al., 1991). This approach not only significantly reduces human involvement in the schematic generation cycle, thereby reducing time and labor costs, but also paves the way for large-scale and high-density reverse schematic generation. Such advancements hold profound implications in fortifying the security of electronic devices.

2.2 Situation

ASG is currently at a critical turning point. Although the technology has been accumulated and applied, its development still faces some core problems. Its core algorithms have made very few breakthroughs in the past decades, which are slow compared to the overall pace of innovation in electronic technology. With the rapid innovation of electronic technology, the inherent ASG is still limited to the generation of simple circuits, and in practical applications, especially for complex and high-density circuits, the outcomes are often meager or even unattainable.

Reverse engineering, especially PCB reverse

engineering, involves in-depth analysis of existing products to obtain design and process information, which is prone to intellectual property and ethical disputes (Sharma et al., 2022). Automated schematic generation is an important part of reverse engineering. Concerns about the legality and ethics of reverse engineering in both academia and industry have restricted the development of ASG. Moreover, the swift evolution of electronic devices has heightened the complexity of relevant technologies, thereby exacerbating the challenges associated with research in this area. Consequently, due to a combination of internal and external factors, the innovation of ASG technology has been slow, which has hindered its broader application in the electronic design processes.

Despite numerous challenges, the significance of ASG cannot be overlooked, and its importance still merits acknowledgment. As a crucial method for netlist visualization, this technology significantly contributes to EDA (Lageweg, 1998). It serves as an essential tool for various tasks, including hardware security protection (Tehranipoor and Koushanfar, 2010) and the maintenance of legacy equipment (Mata et al., 2006). The evolution of ASG is intricately tied to the advancements in EDA throughout history. Since the 1970s, ASG has found extensive applications in electronic design, primarily focusing on the automation of layout and wiring tasks. In recent years, rapid advancements in deep learning technology have significantly enhanced ASG performance and broadened its application scope, solidifying its integral role in contemporary EDA tools. An illustrative example is Synopsys DSO.ai (short for design space optimization artificial intelligence) tool, which achieves automated optimization of chip layout and routing design through the integration of a reinforcement learning engine. Similarly, the Cadence Innovus system uses the cutting-edge GigaPlace engine to enable timing slack-driven layout optimization.

Overall, according to different circuit types, the technology can be categorized into two groups: ASG in integrated circuits and ASG in PCBs (Botero et al., 2020). Integrated circuits typically consist of numerous general-purpose circuits integrated into a small chip to achieve a specific chip function. Based on the functional structure of the chip, they can be further classified into analog integrated circuits (AICs), digital integrated circuits (DICs), and other forms. In contrast, PCBs, in circuit form, are more macroscopic than integrated circuits. They serve as the carriers of integrated circuits, usually with the chip as the core, to construct complex peripheral circuits, and thereby realize the product's functions. Fig. 1 illustrates typical styles of DICs (Fu et al., 2020), AICs (Wang et al., 2020), and PCB circuits (Yang et al., 2024). The structure of DICs typically follows a layer-by-layer arrangement, where component symbols are placed based on the sequential order of rows and columns from left to right. AICs, on the other hand, demonstrate a mirror-symmetric configuration, where component symbols are placed based on the signal flow direction from top to bottom. The structure of PCB circuits exhibits a circular arrangement focused on the chip, adhering to the sequential placement from left to right and top to bottom, thereby forming a circular peripheral circuit. Table 1 summarizes the structural characteristics of different circuit types.

The advent of deep reinforcement learning (DRL) technology has led to its widespread application across various fields, including games (Mnih et al., 2013), biology (Jumper et al., 2021), and

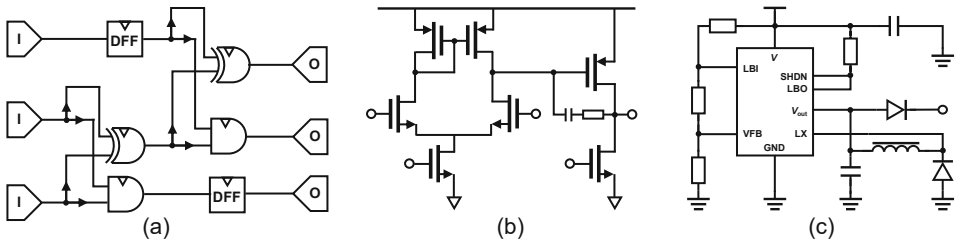

Fig. 1 Examples of different circuit types: (a) digital integrated circuits; (b) analog integrated circuits; (c) PCB circuits. I: input; O: output; DFF: data flip-flop; LBI: low-battery input; VFB: voltage feedback; SHDN: shutdown; LBO: low-battery output; LX: step-up inductor connection; GND: ground

Table 1 ASG techniques for different circuit types

Circuit type	Structural characteristic
DIC	Progressive
AIC	Symmetrical
PCB	Circular flared

chip design (Goldie and Mirhoseini, 2020). This technology has demonstrated remarkable efficacy in decision-making and layout optimization tasks, thereby presenting new opportunities for advancing ASG. DRL possesses the capability to autonomously learn and optimize complex tasks by simulating human decision-making processes. It effectively addresses intricate circuit layout and wiring challenges encountered during schematic generation, offering the potential to overcome existing technical bottlenecks. Moreover, chip layout design and ASG exhibit a high degree of compatibility, as both domains emphasize component placement and routing optimization. In recent years, significant breakthroughs (Liao et al., 2020; Cheng and Yan, 2021; Roy et al., 2021) in chip layout design have been achieved through the application of DRL, and these advancements serve as a vital reference for research in ASG.

2.3 Process

ASG takes a circuit netlist as an input, and outputs a circuit schematic that maintains consistent electrical relationships with the netlist. The netlist, a detailed circuit description file, specifies the components in the circuit and their wire network connections. Displayed graphically, the output circuit schematic illustrates the circuit's structure and connections, facilitating circuit analysis. The technical process, depicted in Fig. 2, involves netlist parsing, component layout and routing, and circuit labeling. Layout and routing, as the core processes, are crucial. Initially, the input circuit netlist is read, and the component information and connection relationships are analyzed, forming a hypergraph $H = (U, N)$, which is used as the input for subsequent layout and routing. Among them, $U = \{u_1, u_2, ..., u_n\}$ denotes the set of components and $N = \{n_1, n_2, ..., n_m\}$ denotes the set of signal networks.

ASG will then lay out any $u_i \in U$. This process is carried out on an empty canvas, with the typical goal of positioning all components in the set on the canvas with minimal placement cost, resulting in clear, easy-to-view layout outcomes. The layout

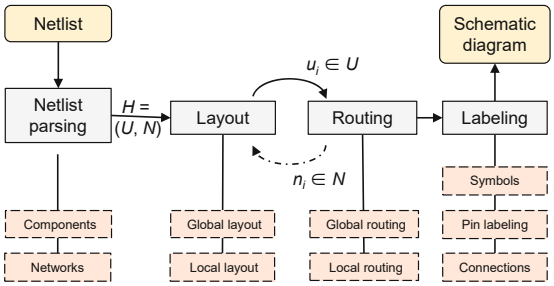

Fig. 2 Automatic schematic generation process

process is commonly divided into global layout and local layout, also known as logical layout and geometric layout (Jehng et al., 1991; Kim et al., 2000). Global layout serves to establish the abstract component locations, and offers macro placement guidance, while local layout specifies the actual geometric coordinates of the components on the canvas and addresses any potential rule violations during the process.

Routing is generally performed after layout. It refers to the process of interconnecting circuit elements on the canvas based on the circuit connection relationships outlined in the netlist. The signaling network $n_i \in N$ contains information about the endpoints (pins) with connection relationships to direct the routing process. Routing is typically categorized into global and local routing. Global routing serves to establish a preliminary routing of the network, while local routing refines the initial routing from global routing to resolve inter-wire congestion and overlap, enhancing the schematic readability.

Upon finishing the layout and routing, the automatic generation method will add suitable symbols and annotations to the circuit schematic diagram based on the type and attributes of the circuit components. This typically includes component symbols, pin labeling, connection point labeling, and more, all aimed at aiding designers in comprehending and analyzing the circuit.

3 Layout algorithms

The layout algorithm, responsible for generating the initial layout of the circuit schematic, is a key step in the ASG. This algorithm sequentially places the components in the circuit netlist on the flat canvas based on the schematic design norms. The process entails thorough consideration of component connectivity, layout density, routing

length, and other factors to ensure that the initial layout meets design constraints while offering enough routing paths. Fundamentally, the layout algorithm tackles a combinatorial optimization problem. In recent decades, research on layout algorithms can be mainly classified into heuristic-based algorithms and DRL-based algorithms. This section presents an overview of layout algorithms in ASG, focusing on these two aspects.

This section reviews the layout algorithms for ASG, which mainly covers two major categories: heuristic- and DRL-based layout algorithms. The advantages and shortcomings of various layout algorithms are summarized in Table 2.

3.1 Heuristic-based layout algorithms

Abstracting the schematic layout process as a mathematical problem, heuristic-based layout algorithms model and design solutions based on specific rules or natural principles to achieve a satisfactory outcome. In the realm of ASG, classical heuristic-based layout algorithms encompass the barycenter algorithm (Swinkels and Hafer, 1990), the bubble algorithm based on value propagation (Jehng et al., 1991), and the simulated annealing algorithm (Steinbrunn et al., 1997).

Swinkels and Hafer (1990) argued that the generation of DICs with visualization and specification requirements is a non-deterministic polynomial (NP)-hard optimization problem, and typically, one can only find a standard solution rather than the optimal solution. Therefore, they proposed a logical layout algorithm for DICs based on an expert knowledge system and a barycenter algorithm. Usually, the logical layout can be divided into two phases: horizontal and vertical ordering. It is used to determine the logical position of component symbols in the layout. In the horizontal layout phase, a recursive graph traversal algorithm is used to ensure that the signal flow direction of the circuit follows the left-to-right layout norm. This algorithm detects and removes feedback loops from component connections, and determines the columns where the component symbols are located. Once column positions are assigned to all component symbols, the vertical sorting phase assigns rows where the component symbols are located based on the barycenter algorithm. This algorithm calculates the average row position with respect to the connected symbols or the row position where the center of gravity is located to determine the row position of the current symbol. Finally, the knowledge system is used to find a standard layout based on heuristic layout criteria such as the number of crossings between networks and the number of wire bends.

The barycenter algorithm is a classical sorting method used in logical layout. It exhibits a time complexity of $O(n)$ and a space complexity of $O(1)$ when sorting n elements. This algorithm is characterized by its rapid computational speed and minimal space requirements. Consequently, it finds a broad array of applications in the automatic generation of schematics for DICs. The bubble algorithm, based on value propagation proposed by Jehng et al. (1991), is categorized as a variant of the barycenter algorithm. During the horizontal sorting phase of the logical layout, circuit leveling is used to assign each symbol its respective column position from left to right. During the vertical sorting phase, the bubble algorithm based on value propagation is employed to assign the symbols their respective rows. The algorithm process is depicted in Fig. 3. At the outset, a value is set for each input symbol according to its initial row position. Subsequently, each symbol in

Table 2 Advantages and shortcomings of various layout algorithms

Category	Name	Advantage		Shortcoming
Heuristic-based	Heuristics with rules	Higher interpretability, more quickly		Lacking the ability to obtain optimal solutions
	Simulated annealing	Strong search capability for optimal solutions		Slow convergence and sensitive to parameters
DRL-based	The method of Hsu and Lin (2022)	Embedded building block features for high quality	Insensitive to parameters and able to obtain optimal solutions	Dramatically expanded search space with increasing schematic density
	AEM-PCB reverser	Introducing objective PCB schematic quality metrics		

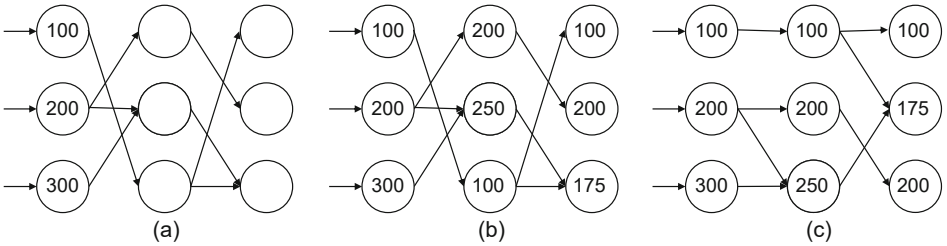

Fig. 3 Bubbling algorithm process: (a) initializing; (b) value propagation; (c) re-ordering

the netlist calculates its value by averaging the values of the connected symbols. Once all symbols have been assigned values, each column is reordered according to the symbol value, thereby assigning the column position to each symbol. In comparison to the barycenter algorithm, this algorithm exhibits a higher time complexity of $O(n^2)$ due to the need to compare all symbols at each iteration. However, it compensates for this increased complexity by generating layout results with fewer signal line crossings.

In schematic generation for AICs, Arsintescu (1996) employed a rule-based heuristic approach. Symmetric symbol pairs were identified and arranged in a mirror pattern. These pairs were then placed on a grid, and the layout was optimized by minimizing the wire length and the number of wire bends. The heuristic rules acted as supervisors to ensure smooth layout paths during generation. In addition, the vertical layout method proposed by Garg et al. (2008) assigns vertical positions to function block symbols in a top-to-bottom manner according to the signal flow direction incrementally. By ensuring both horizontal and vertical alignment in symbol placement, the method is able to avoid crossover and overlap between networks as much as possible. Wu YP et al. (2009) proposed a function block symbol layout method with the aim of minimizing wire length. This method integrates symmetry, alignment, and other constraints during the placement of component symbols.

The advantage of these heuristic methods lies in their ability to generate layouts using explicit rules and strategies. These rules and strategies can be adjusted and optimized to meet specific generation needs with high interpretability. Additionally, feasible standard solutions can be generated quickly to ensure layout efficiency. However, the heuristic rules used in these methods lack the capability to achieve the global optimal solution, making it challenging to ensure the quality of the layout.

The simulated annealing algorithm, inspired by the physical process of material annealing, aims to find the global optimal solution through probabilistic searching. This algorithm involves randomly exploring the solution space, and has been extensively applied to address layout optimization challenges. Regarded as a high-performance heuristic algorithm, it was used by Lee and McNamee (1989) for automatic generation of DICs. The method focuses on optimizing symbol row sequences within the layout space by iteratively and randomly swapping the positions of symbols in the same column to reduce wire crossings. Its detailed algorithmic pseudo-code can be found in Algorithm S1 in the supplementary materials. Theoretically, the algorithm possesses the capability to approximate a global optimal solution as the termination temperature T_f approaches 0. The time complexity of this algorithm is contingent upon the temperature settings and the number of iterations conducted in each round. It is mathematically represented as $O\left(\frac{\mathcal{N}\log(T_\mathrm{f}/T_0)}{\log r}\right)$, where $\mathcal{N}$ is the number of iterations at each temperature, T_0 is the initial temperature, and r is the temperature decline rate.

Although the simulated annealing algorithm has shown some potential in layout, subsequent research on ASG has not been thoroughly investigated. One reason is its low search efficiency, especially in large-scale schematic layout tasks, leading to slow convergence and unsatisfactory results. In contrast, the simulated annealing algorithm has excelled in very-large-scale integrated circuit design. The optimization of its search efficiency has been studied (Sechen, 1988; Sergey et al., 2019; Katsuki et al., 2022), which greatly overcomes the challenge of slow convergence speed. These studies provide valuable insights into the application of the algorithm in ASG. Further

optimizations to the simulated annealing algorithm are anticipated to enhance the quality of ASG while ensuring a certain level of search efficiency and convergence speed. This advancement is expected to enhance the practical application value of the layout algorithm for ASG.

3.2 DRL-based layout algorithms

DRL-based layout algorithms have become a recent research hotspot in the realm of ASG. The algorithms tackle the schematic generation problem by converting it into a combinatorial optimization problem. Through guidance from the reward function, reinforcement learning agents are trained to determine the placement of component symbols, thereby achieving the schematic layout.

The method, based on building block classification and reinforcement learning, is a classic example of automatic AIC schematic generation algorithms (Hsu and Lin, 2022). This approach achieves intelligent component placement through the interaction between the agent and the layout environment. At each step, the agent observes the canvas's current state, feeding this information into the neural network along with the embedded features detailing building blocks and signal flow to receive layout suggestions. Subsequently, guided by the neural network's output, the agent executes suitable placement actions for the component symbols on the canvas. Through continuous iteration and guided by the reward function, the reinforcement learning agent engages in trial-and-error processes and self-improvement within the solution space. This allows the agent to autonomously discover the optimal layout strategy, leading to the best layout outcomes. Among them, the reward function covers the optimization of several metrics, such as the area of building blocks, the number of network crossings, the number of wire bends, and the total length of wires, to ensure that the schematic layout meets the requirements of circuit generation. Algorithm S2 in the supplementary materials shows the process of the layout algorithm based on reinforcement learning.

In the realm of reverse automatic generation of PCB schematics, Yang et al. (2024) introduced a reinforcement learning layout method centered on aesthetic evaluation metric (AEM), called AEM-PCB reverser. The method is shown in Fig. 4. A key feature of this method is the introduction of metrics that objectively quantify the quality of PCB schematic diagrams. These metrics consider factors like the normality and readability of layout and routing, ensuring a high level of consistency between the metric scores and the designer's subjective evaluation. By incorporating these metrics into the reward function, the reinforcement learning agent is guided to perform layout optimization. This addresses the problem that PCB schematics are difficult to generate automatically due to the lack of objective standards in the past. It provides a reliable metric foundation for the automatic generation and optimization of PCB schematics.

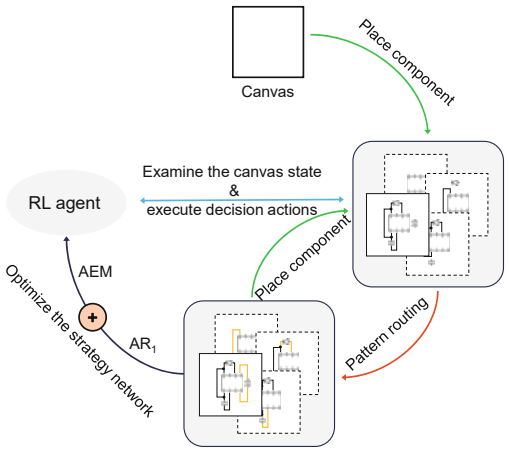

Fig. 4 The method of the AEM-PCB reverser. RL: reinforcement learning; AR: aesthetic reward

Overall, in ASG, the DRL-based layout algorithms demonstrate good performance. They not only discover the optimal solution in the layout space, but also operate solely through agents spontaneously without manual parameter adjustments. However, a drawback is that the state and action space of reinforcement learning experiences an exponential expansion as schematic density increases. This poses challenges such as reduced convergence speed or even difficulty in converging in complex schematic environments. Taking the analog schematic diagram generation method (Hsu and Lin, 2022) as an example, although certain results were achieved, the number of schematic components did not exceed 40, which has certain limitations. This underscores constraints of layout algorithms based on DRL when confronted with complex schematics.

However, despite facing challenges in ASG due to increasing schematic density, the layout

algorithms based on DRL still hold significant potential for generating complex schematics. This potential is exemplified by the widespread application of this algorithm in chip layout design (Agnesina et al., 2020; Vashisht et al., 2020; Lai et al., 2023; Shi et al., 2023; Zhong et al., 2024a). These applications integrate layout problems with DRL, aiming to optimize the power, performance, and area (PPA) of chip designs, significantly improving the floorplanning results. It is well known that chip layout designs typically deal with hundreds of millions of transistors, and their complexity is even greater. To mitigate layout density, transistors are often grouped and abstracted into higher-level standard cells and macro-cells. Following this approach, the chip layout algorithm employs DRL-based layout for fewer, more functional macro-cells, while heuristic enhances layout speed for a larger number of standard cells. This hierarchical layout strategy serves as a valuable reference for reducing layout density and enhancing the algorithm's generation efficiency in complex and densely-packed circuits within ASG.

4 Routing algorithms

The core of routing involves path searching, which entails a specific search strategy to locate the optimal path that meets certain constraints in a complex routing setting. According to the different order of the wire network arrangement, routing algorithms can be divided into two categories: sequential and simultaneous routing algorithms.

Sequential routing algorithms follow a specific iterative order to wire the network step by step. Common sequential routing algorithms are maze search algorithms and pattern routing algorithms. In addition, reinforcement learning-based routing algorithms that appear in recent years adaptively adjust the routing strategy by employing agents to control the direction of the routing that also belongs to sequential routing algorithms. Simultaneous routing algorithms, in contrast, simultaneously route all the networks, and typically rely on integer linear programming (ILP) to search for routing paths under multiple optimization objectives.

This section provides an overview of the main routing algorithms, including those used in ASG. The algorithms are categorized based on sequential and simultaneous routing approaches from an algorithmic perspective. Table 3 summarizes the advantages and shortcomings of the various routing algorithms.

4.1 Sequential routing algorithms

During the routing process, the sequential routing algorithms arrange the networks in a specific order. They interconnect the endpoints in the wire network one by one, selecting a relatively better routing path in each interconnection. These paths are optimized through multiple iterations to achieve the best routing results. Classical sequential routing algorithms include Lee's algorithm (Abel, 1972), A* algorithm (Hart et al., 1968), pattern routing algorithm (Kastner et al., 2000), and the right-angle minimum Steiner tree (RMST) algorithm (Lee and McNamee, 1992).

4.1.1 Lee's algorithm and A* algorithm

Lee's algorithm (Abel, 1972) is a shortest path method that calculates the routing cost between a source point and a target point through wave propagation. The algorithm employs a breadth-first strategy, starting from the source point and calculating the routing cost of its neighboring points. It then uses these neighboring points as a new base point to continue spreading outward, calculating the routing cost of the neighboring points from the source point. This process repeats until the base point reaches the target point, marking the end of the spreading. Finally, the algorithm selects the routing path with the lowest cost. Due to the necessity of calculating the routing cost for all points between the source and target points, Lee's algorithm has high computational complexity, requires significant memory resources, and operates at a slow speed.

In contrast, the A* algorithm (Hart et al., 1968) improves upon Lee's algorithm by searching for the shortest path more efficiently. It achieves this by incorporating a heuristic function to direct the routing search. The A* algorithm calculates the sum of the actual cost from the source point to the current point and the estimated cost from the current point to the target point. This sum serves as a reference value, guiding the selection of the next base point with the smallest total cost. The algorithm then proceeds to compute the total cost of the neighboring points of this base point, and continues this process, gradually

Table 3 Advantages and shortcomings of various routing algorithms

Category	Name	Advantage	Shortcoming
Sequential routing	Maze search routing	Detailed path search, good ability to obtain optimal solutions, and good routing quality	High computational complexity and memory footprint, slow computation
	Pattern routing	Low computational complexity and routing cost, allowing for fast routing	Fixed-mode routing, a lack of flexibility, and poor routing quality
	Right-angle minimum Steiner tree	Capable of handling the routing of multi-terminal wire networks	NP-complete problem with high algorithmic complexity
	DRL-based routing	Strong global routing capability, spontaneous optimization without manual intervention	Slow agent training and inefficient routing
Simultaneous routing	Totally simultaneous routing	Avoiding adverse effects caused by routing sequences through synchronized routing	Dramatically increased computational complexity with the increase of constraint conditions
	Hybrid routing	The reduced optimization solution space and improved routing speed by predefined candidate paths	Reduced routing quality

directing the search toward the target point. Unlike Lee's algorithm, the A* algorithm computes only the total cost along the search path, reducing computational complexity to some extent and enhancing routing speed. Algorithm S3 in the supplementary materials shows the process of the A* algorithm.

Frezza and Levitan (1993) introduced the schematics placement and routing (SPAR) method for ASG. The method employs the A* algorithm for path searching in global routing. It calculates the actual cost based on the path congestion and the Manhattan length from the source point to the base point. The estimated cost is set at 0.8 times the Manhattan length from the base point to the nearest endpoint in the network. By using a low estimate, the method ensures an optimal solution for path searching.

4.1.2 Pattern routing algorithm

Despite significant improvements based on Lee's algorithm, the traditional A* algorithm still faces the challenge of high computational and memory overhead for complex routing. This challenge stems from the fact that the A* algorithm is based on a search-based pathfinding approach and complex routing over long distances leads to high time and memory overhead.

In contrast, unique advantages are demonstrated by the pattern routing algorithm (Kastner et al., 2000). The algorithm significantly reduces the complexity by employing predefined routing patterns to guide the pathfinding process, and achieves a time complexity of only $O(1)$. Several common routing patterns in pattern routing, such as I-type, L-type, Z-type, and U-type, are demonstrated in Fig. 5. The routing patterns can also be customized for various application scenarios or circuit characteristics to ensure the applicability and scalability of pattern routing. However, compared to the A* algorithm, flexibility is lost by the pattern routing algorithm, resulting in relatively lower routing quality. Taking L-pattern routing as an example, only two routing paths can be selected. In extreme cases, both paths may not be ideal, which can adversely affect the quality of the routing results.

Combining pattern routing with maze search algorithms is an efficient way to tackle this issue, where pattern routing is applied for quick routing at a reasonable cost, and maze search is used to provide better routing results when the path cost is too high. This method is used in the generation of AICs by Hsu and Lin (2022). The routing process is greatly accelerated by using pattern routing algorithms to connect the component symbols on the schematic canvas. For components that could not be fully

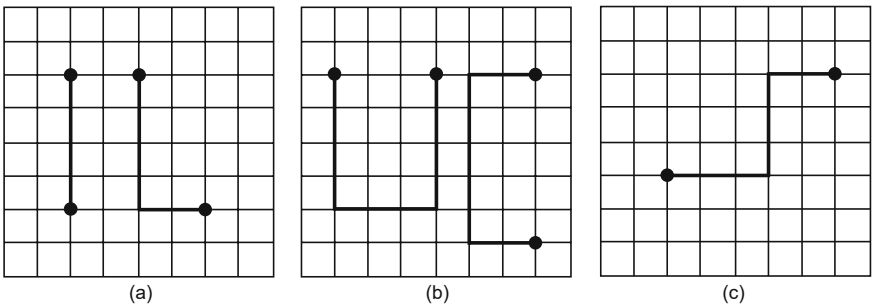

Fig. 5 Pattern routing style: (a) I-type and L-type; (b) U-type; (c) Z-type

connected by pattern routing, a maze search algorithm is used as a supplement to routing. In addition to yielding good routing results, this integrated use of maze search algorithms and the pattern routing algorithm greatly lowers the complexity, providing a fast and effective strategy for generating schematics.

4.1.3 RMST algorithm

Both the A* algorithm and pattern routing algorithm are usually used to deal with the routing of two-ended wire networks; i.e., they can effectively solve the pathfinding problem with only one source point and target point. However, for more complex multi-terminal wire network routing, these algorithms appear to be inadequate. To cope with this problem, the commonly adopted routing method is the RMST (Lee and McNamee, 1992).

The RMST algorithm implements the routing of a multi-terminal wire network by introducing auxiliary Steiner points in the network with the goal of minimizing the routing cost. To ensure the rationality of the routing, Steiner points are typically selected in the right-angle space of the multi-terminal wire network. This means that the Steiner point is always aligned horizontally or vertically with either endpoint in the multi-terminal wire network.

Let the nodes in the multi-terminal network be defined as a terminal set of size k. The RMST algorithm employs dynamic programming to construct the minimum tree, with the primary source of computational complexity stemming from this approach. The core idea of dynamic programming is to decompose complex problems into simpler subproblems which can then be recombined. In RMST, the terminal set is partitioned, and these subsets are enumerated to form subtrees. Ultimately, these subtrees are merged to derive the minimum Steiner tree for the terminal set. This process has a computational complexity of $O(n3^k)$. Consequently, while RMST is capable of addressing the routing issues in multi-terminal networks, it faces challenges related to high computational complexity and the difficulty of achieving optimal solutions.

To address these challenges, researchers have proposed heuristic-based RMST algorithms (Hanan, 1966). A Steiner tree heuristic routing algorithm based on continuous iteration was proposed by Lee and McNamee (1992). This algorithm uses minimum spanning trees to adjust the rectangular space and reduce the generation complexity of Steiner trees. As shown in Fig. 6, the method first generates a minimum spanning tree for a multi-terminal wire network, and then iteratively works on edges with common nodes in the spanning tree. If there is a Steiner point in the rectangular space of these common edges, the two edges are replaced with three edges connected to that point. This process continues iteratively until no new Steiner points are generated. Finally, the line edges are converted to straight edges to generate the routing result. The rectangular space is a set of nodes aligned horizontally or vertically with the endpoints of edges.

Additionally, Chu and Wong (2008) introduced a fast lookup table-based RMST algorithm, significantly reducing the algorithm's time complexity at the expense of some storage space. For multi-terminal wire networks with nine or fewer endpoints, the optimal RMST can be directly obtained through table lookup. For networks with fewer than 100 endpoints, the algorithm can still achieve suboptimal solutions with high accuracy.

This subsection presents various common sequential routing algorithms, each with distinct

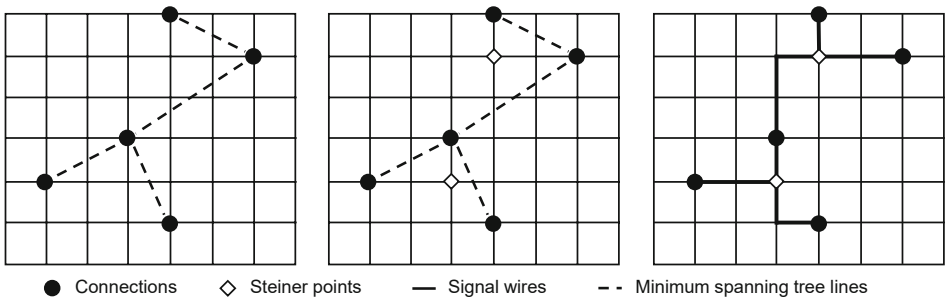

Fig. 6 Iteration-based Steiner tree heuristic routing

advantages and disadvantages, capable of yielding different outcomes based on the scenario. Apart from the aforementioned algorithms, routing algorithms leveraging DRL have recently emerged as significant methods.

The DRL global routing method proposed by Liao et al. (2020) controls routing direction through agents to determine routing paths, surpassing the A* algorithm and showcasing the broad application potential of DRL in routing planning problems. Meanwhile, the HubRouter algorithm introduced by Du et al. (2023) represents a novel generative approach to global routing. This method is structured into two distinct phases. In the first phase, it employs image generation models, including generative adversarial networks (GANs) and variational auto-encoders (VAEs), to create hubs. The second phase integrates an RSMT algorithm with a deep learning model to effectively connect these hubs. This strategy significantly enhances performance by thoroughly merging traditional algorithms with advanced deep learning techniques. Furthermore, the PreRoutGNN algorithm proposed by Zhong et al. (2024b) incorporates a pre-training technique within the routing process. This integration effectively addresses the challenges of signal decay and error accumulation that arise in long-timing paths, achieving state-of-the-art results in the spare prediction tasks of several realistic circuits. These advancements underscore the evolving trend of deep learning technology in the routing domain, and pave the way for new explorations in both theoretical research and practical applications of future routing technologies.

4.2 Simultaneous routing algorithms

Sequential routing algorithms execute the routing of each network one by one in a predetermined order. The front–end routing may have a detrimental impact on the subsequent routing, leading to diverse outcomes based on different sequences (Abel, 1972). At times, regional congestion may arise due to constraints in wiring paths, posing challenges in attaining optimal outcomes in sequential wiring.

Simultaneous routing algorithms offer greater flexibility compared to sequential routing algorithms. They are not constrained by a specific routing order; instead, they process all the networks in the circuit simultaneously. These approaches help address suboptimal solution issues that may arise by following a predetermined routing order. Typically rooted in ILP, these algorithms treat edges or points of the routing networks as independent variables. They comprehensively consider various routing constraints, construct the objective function, and determine the optimal routing scheme by minimizing the objective function while meeting the constraints. Ou et al. (2014) introduced a simultaneous routing approach, which integrates the four constraints of symmetry, concentricity, topology matching, and length matching into the AIC routing problem. By employing an ILP formulation and binary decision variables (0–1), they achieved precise edge assignments in routing, leading to superior results compared to sequential routing strategies.

However, the complexity of ILP is intricately linked to the complexity of both the objective function and the constraints. Consequently, common ILP algorithms, such as the branch-and-bound method and the cut-plane method, typically exhibit exponential time complexity in most scenarios. This characteristic renders this class of algorithms computationally inefficient. To tackle this issue, Wu CY et al. (2015) introduced a hybrid strategy. They employed a rapid sequential routing algorithm as an initial

step to generate candidate routing paths for each wire network. Subsequently, an ILP formula with binary decision variables was constructed to determine the adoption of specific candidate paths. This strategy skillfully balances the quality and efficiency of routing, significantly improving the efficiency of simultaneous routing by reducing the solution space.

In general, the simultaneous routing algorithms exhibit their superiority in improving routing quality. Through the utilization of a global optimization approach, the algorithms can identify the optimal solution while simultaneously adhering to multiple constraints. However, the simultaneous routing algorithms demonstrate a relatively high time cost. Subsequent research efforts could further explore the enhancement of the simultaneous routing algorithms to improve their solution efficiency while maintaining routing quality.

5 PCB automatic schematic generation

The typical structure of a PCB is centered around a main chip as the core, multiple secondary chips as subcores, and surrounded by active and passive components forming the peripheral circuit. The main chip typically serves as the central component of the overall circuit, controlling and coordinating the operation of the entire system. Secondary chips are tasked with executing specific functions, such as signal processing and power management. Peripheral circuits encompass passive components, such as resistors, capacitors, and inductors, and active components, such as transistors and operational amplifiers. In contrast to integrated circuits, the schematic structure of a PCB is more macroscopic, and the shapes and sizes of components are different, exhibiting complexity and specificity. In the past, the ASG method was primarily based on DICs or AICs, characterized by high regularity, displaying progressive and symmetrical layout patterns, distinct from PCB circuits. Consequently, the conventional automatic schematic layout and routing techniques pose challenges when directly employed for PCB generation tasks.

This section addresses the technology of ASG in PCBs, discusses its metrics, and analyzes the current difficulties and challenges encountered in this field. Based on this analysis, viable solutions are explored to offer valuable references and insights for the future advancement of automatic PCB schematic generation technology.

5.1 Metrics

Schematic drawings represent a fusion of artistic aesthetics and technical accuracy, where their legibility plays a crucial role in ensuring the precise communication of information. Designers infuse their distinct perspectives and styles into the creation of schematics, which undoubtedly adds to the complexity and subjectivity of evaluating schematics (Jehng et al., 1991). Nevertheless, they always follow a common set of design norms when creating schematics. For example, the flow of signals usually follows the principle of left-to-right, and the numbers of wire crossings and bends are minimized. These established norms serve the purpose of ensuring the clarity, consistency, and precision of schematics, as well as facilitating mutual comprehension and utilization of designs by various designers. Hence, although the evaluation of schematics may differ based on personal aesthetics and viewpoints, adhering to standard design norms is unquestionably crucial for ensuring the quality of schematics.

These design norms play a crucial role in the generation of schematics as they are essential prerequisites for the automated optimization of layout and routing. Traditional heuristics commonly employ optimization objectives, such as minimizing the numbers of wire crossings and bends and reducing the wire length in the routing, to generate schematics that meet the design norms. The intricate nature of the PCB schematic structure necessitates a more comprehensive metric for optimization objectives, as traditional criteria may not adequately capture all aspects of its design norms. For instance, the optimization objective of minimizing the numbers of wire crossings and bends makes it difficult to express the design specification for the flow of signals from left to right and top to bottom in the PCB schematic design. Similarly, efforts to reduce wire length often result in overly compact component arrangement in the layout, thereby diminishing the schematic readability.

To solve the problem of the lack of objective metrics for evaluating PCB schematic quality, Yang et al. (2024) introduced the AEM as a method for objectively assessing the quality of PCB schematics,

which was based on the layout and routing norms found in PCB schematic diagrams. Through a comprehensive analysis of common regular features in numerous schematic diagrams, they identified the fundamental elements that influenced the attributes of PCB schematic diagrams. These attributes encompass clarity, readability, and neatness. Subsequently, by employing mathematical quantification methods and the refinement of relevant formulas, the evaluation metric was effectively developed to align closely with the subjective assessments of designers, maintaining a high level of consistency with them. This marks the initial step toward supporting the automatic generation of PCB schematics by establishing a foundation for the metric. The formula is presented as follows:

$$\mathrm{AEM}=\sum_{i=1}^{n}\mathrm{AR}_i, \tag{1}$$

$$\mathrm{AR}=\frac{\sum\limits_{j=1}^{m}\left(R_{\mathrm{L}_j}\cdot D_{\mathrm{RB}_j}\cdot D_{\mathrm{NC}_j}\right)}{m}, \tag{2}$$

$$R_{\mathrm{L}_j}=\frac{R_{\mathrm{b}_j}}{\alpha}+\frac{(\alpha-1)(R_{\mathrm{b}_j}-P_j)}{\alpha}, \tag{3}$$

where AR_i denotes the aesthetic reward generated per layout i, R_{L_j} denotes the baseline score after alignment checks and distance penalties for routing j, n denotes the number of layouts, which is equal to the number of components in the circuit, m denotes the routing counts after each layout, D_{RB_j} and D_{NC_j} denote the discount factors determined by the number of routing bends and the number of network crossings, R_{b_j} is affected by the alignment of the components and denotes the baseline fraction, P_j denotes the penalty fraction to constrain a single routing to be in a given range of lengths, and α is the single routing robustness factor which is generally taken to be a value of 2 in the experiments.

5.2 Difficulties and discussion

5.2.1 Difficulty in reverse residual netlist processing

In the process of forward design, the transformation from the PCB schematic to the netlist involves comprehensive information about electronic components, such as component footprints, parameters, and the interconnection relationships. In contrast, when generating schematic diagrams in reverse engineering, the netlist is typically obtained by scanning the PCB image for deduction. This process can easily result in information loss, which is predominantly evident in indeterminate component footprints, missing parameters, and ambiguous connections, leading to the circuit netlist obtained with residuals. These residual netlists are crucial for ensuring the accuracy and completeness of the schematic generation. Therefore, the automatic restoration of the schematic based on residual netlists poses a significant challenge in reverse engineering for PCB schematic generation.

The utilization of graph neural network technology for matching and identifying residual networks has proven to be an effective approach in tackling the challenges associated with generating schematic diagrams for residual netlists. During the PCB design process, the circuit design builds its peripheral circuits based on the core chip, and these peripheral circuits are usually derivatives of the chip's reference circuits. Therefore, there are similarities in the connection relationships and schematic structures between the peripheral circuits on the PCB and reference circuit. By training the graph neural network model with ample reference circuit data, it can learn the underlying correlations among component types, parameters, and connections. This enables the model to supplement components and connections in the residual netlists, offering precise and complete circuit netlists for PCB schematic generation, thereby reducing the complexity of reverse circuit schematic generation.

In addition, the image recognition method employing convolutional neural networks is used for analyzing the PCB image. When integrated with the component library, this method can effectively identify the types and footprints of components in the circuit, thereby supplementing any missing parameter information in the residual netlist. The component library is a collection of information containing various electronic component footprints and types, device parameters, and pin parameters. Through the utilization of an image recognition method, the identifiers of components in the PCB image are recognized, and the corresponding footprints and parameters are matched from the component library. Convolutional neural networks, known for their superior performance in image recognition tasks, have the potential to significantly improve the recognition accuracy and matching precision of missing component

information in PCB circuits. This process aids in filling in the gaps in the netlist's information and improving the clarity and readability of the generated PCB schematic.

5.2.2 Difficulty in generating complex and dense schematics

In PCBs, especially in densely populated ones with numerous components and complex connections, fast layout and routing are crucial for generating clear and readable PCB schematics. This is essential to guarantee their efficient implementation and application in PCB reverse engineering.

However, global optimization algorithms used for layout and routing, such as layout algorithms based on DRL or heuristic layout algorithms based on simulated annealing, necessitate conducting numerous searches in the global space. This results in slow convergence of the algorithms. When confronted with tasks of generating PCB schematics, the complexity of the layout increases nonlinearly as the quantity of components sharply increases. This causes the above algorithms to be stretched in terms of processing efficiency, and may not even be able to complete the schematic generation. Therefore, improving the efficiency of complex and intensive schematic generation while ensuring the quality of layout and routing is one of the current PCB reverse engineering problems that need to be solved.

The incorporation of heuristic rules into global algorithms has been identified as an effective strategy for enhancing search efficiency. These rules are usually based on expert knowledge, and have the capability to remove numerous invalid subsolutions within the solution space through straightforward and efficient computation. By restricting the search scope, efficient pruning can be implemented during the global search process. In tasks involving the intensive automatic generation of PCB schematics, the utilization of heuristic rules to eliminate actions that do not adhere to design norms or lead to suboptimal results can significantly decrease the search space of the global layout and routing algorithms. This enhances the efficiency of the generation process.

By simplifying netlists and partitioning functional modules within dense PCB schematics, it is possible to substantially reduce the search depth of global algorithms. Positive PCB design generally adheres to the "top–down" approach, starting from the overall circuit function and systematically decomposing it into functional modules. Subsequently, the components in each specific module are placed and routed to form a complete circuit schematic design. This design concept is characterized by its well-organized structure, which can greatly simplify complex problems and improve design efficiency.

The algorithm for netlist partitioning based on graphs (Hong et al., 2023) uses a graph neural network to automatically analyze and understand the graph structure of complex circuit netlists. The algorithm segregates the circuit netlist into different modules based on the functional and structural characteristics of the circuit. This process facilitates the potential for automated generation of schematic representations in a "top–down" manner. In PCBs, Meng and Zheng (2022) used an attribute-based netlist partitioning approach, segmenting the PCB netlist into functional modules. Followed by the independent layout and routing of each module, it can significantly decrease the global search algorithm depth, leading to a significant enhancement in the efficiency of automatically generating densely populated schematics for PCBs. It is important to note that the division results significantly influence the comprehensibility of the schematic. Therefore, the accuracy and effectiveness of the netlist partitioning algorithm are pivotal factors that need to be taken into account in this strategy.

Overall, schematic generation and reduction based on the residual netlist is an important feature and challenge of PCB reverse engineering. Improving the accuracy and reliability of automatic PCB schematic generation technology with a residual netlist is an important prerequisite to enabling designers to understand and read the reverse schematic effectively. Efficiently addressing the challenge of generating intensive PCB schematics is fundamental to the engineering and application of this technology. It enhances the breadth and speed of automated generation, facilitating its widespread application in practical engineering. There exists a progressive relationship between the two issues; the current PCB ASG technology is an important research direction.

6 Conclusions

This paper provides an overview of ASG, detailing its process, methodology, and core algorithms,

specifically focusing on layout and routing. Drawing from the current state of automatic PCB schematic generation, this paper delves into three aspects: objective evaluation metrics, difficult challenges, and feasible solutions. The goal is to propel the future development of automatic PCB schematic generation.

The core algorithms for ASG are layout and routing. For layout, this paper introduces heuristic- and DRL-based layout algorithms. Heuristic-based layout algorithms offer high interpretability and faster layout speed, but face challenges in achieving the optimal layout. Although the simulated annealing method can achieve the global optimal solution, it encounters low search efficiency. Further research on the convergence speed of the simulated annealing algorithm can enhance the application and development of ASG.

DRL-based layout algorithms operate without human intervention, and depend solely on the autonomous learning of the agent. They exhibit low reliance on the initial layout. However, as circuit complexity increases, the action space and state space expand significantly, posing challenges for convergence in learning. The solution to this issue lies in the exploration of hierarchical schematic generation algorithms.

For routing, this paper introduces sequential and simultaneous routing algorithms. The sequential routing algorithms typically conduct path search for each wire network individually, exhibiting low algorithmic complexity, resulting in a faster routing speed. Nevertheless, varying routing sequences may lead to suboptimal solutions. The simultaneous routing algorithms address the issue of suboptimal solutions due to the routing sequences. However, the computational complexity associated with linear optimization for multiple objectives is notably higher compared with that of sequential routing, resulting in a lower routing efficiency. Therefore, further exploration of routing algorithm efficiencies while maintaining quality is a significant research area in the realm of ASG.

This paper also emphasizes the discussion on ASG for PCB reverse engineering. The structure of the PCB schematic is unique, and the shape and size of its components are different. The challenges faced in the automated generation of schematics for PCB reverse engineering are significantly influenced by the uniqueness and differentiation. Under the premise of having an automatic optimization metric, the schematic generation problem of residual netlist is the primary challenge in PCB reverse engineering. The identification and matching algorithm based on deep learning is an effective way to complement the residual netlist and improve the accuracy of PCB schematic generation. Furthermore, the engineering application of PCB schematic generation technology faces a significant challenge of low efficiency in intensive PCB schematic generation. Heuristic algorithms and modular generation serve as crucial breakthroughs in tackling this challenge.

Contributors

Bin YAN designed the outline of the review. Jie YANG and Kai QIAO drafted the paper. Chen CHEN helped organize the paper. Lixiang GUO and Jian CHEN revised and finalized the paper.

Conflict of interest

All the authors declare that they have no conflict of interest.

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List of supplementary materials

Algorithm S1 Simulated annealing algorithm based on the logical layout

Algorithm S2 Layout algorithm based on reinforcement learning

Algorithm S3 A* algorithm