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One-dimensional reconfigurable three-stage Doherty power amplifier with load mismatch resilience*

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Abstract: This article presents a comprehensive theoretical analysis of the resilience demonstrated by the three-stage Doherty power amplifier (DPA) when operating under load mismatch conditions. Additionally, a novel reconfigurable three-stage DPA architecture is introduced, with the aim of enhancing resilience to load mismatch using exceptionally simple circuits and a one-dimensional (1D) control method. To validate the efficacy of this proposed architecture and control approach, a DPA prototype employing commercial gallium nitride (GaN) active devices has been designed and meticulously fabricated at 2 GHz. With a matched 50 Ω load, the fabricated three-stage DPA achieves a high-efficiency range of 9.5 dB with larger than 51% back-off drain efficiency (DE). Through the proposed 1D control, the DPA presents 47.0%–55.1% back-off efficiency with ≤ 2 dB power fluctuation at a 2:1 voltage standing wave ratio (VSWR) over a 360° phase span. When driven by a 20 MHz long-term evolution (LTE) signal with an 8 dB peak-to-average power ratio (PAPR), the DPA achieves 46.2%–53.9% average efficiency and better than −21 dBc adjacent channel power ratio (ACPR) without digital pre-distortion (DPD) under load mismatch conditions.

Key words: Doherty power amplifier; Load mismatch; One-dimensional (1D) control; Reconfigurable; Three-stage
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1 Introduction

As wireless communication systems transition into the fifth generation (5G) era, multiple-input multiple-output (MIMO) and phased array technologies are extensively used to boost spectral efficiency and enable beam scanning capabilities. However, with the increasing popularity of large-scale arrays, the integration of nonreciprocal components, such as circulators and isolators, into wireless communication equipment has become a crucial design challenge. This poses a significant obstacle, as the load condition of array systems often varies with different beam scanning configurations. Consequently, there is a strong demand for wireless communication equipment that exhibits resilience against load mismatch. Additionally, the compact size requirements of terminal devices present a similar challenge, further emphasizing the need for innovative solutions in this domain.

Power amplifiers (PAs), as the active component closest to the antenna in the transmitter, are normally sensitive to load mismatch, which can seriously affect their performance in current and future wireless communication systems. Moreover, to adapt to the widely adopted high peak-to-average power ratio (PAPR) signal characteristics, PA architectures with a large high-efficiency range such as Doherty power amplifier (DPA) (Fang et al., 2018; Nikandish et al., 2020; Zhou XY et al., 2020; Pang et al., 2022) and out-phasing (Barton T, 2016; Barton TW et al., 2016; Wang et al., 2020) have been widely used, and these architectures present even worse load

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mismatch adaptability due to their more complex circuits. To improve the PA load resilience, several techniques have been explored in recent years, such as dynamic supply voltage (Gonçalves et al., 2021, 2022), six-port network load mismatch correction (Singh et al., 2021), reconfigurable output matching network (OMN) (Donahue et al., 2020), digital Doherty architecture (Hu et al., 2015), dual-mode Doherty operation (Lyu and Chen, 2020, 2022; Lyu et al., 2021; Shi et al., 2023), and modified load modulated balanced amplifier (LMBA) (Quaglia et al., 2022b; Guo et al., 2023).

It is noteworthy to mention that, due to the originally employed PA architectures, the majority of resilience enhancement methods currently available offer a high-efficiency range of $\leq$ 6 dB. This falls short of satisfying the signal peak-to-average power ratio (PAPR), which typically ranges from 8 dB to 12 dB for 5G and beyond 5G systems. In efforts to expand the high-efficiency range for normal matched loads, several techniques have been explored. These include asymmetrical (Kim et al., 2011; Jang et al., 2014; Pang et al., 2016) and multi-way/multi-stage (Neo et al., 2007; Golestaneh et al., 2013; Xia et al., 2019; Gao et al., 2022; Zhou H et al., 2022a; Piacibello et al., 2023) Doherty architectures, DPAs employing complex combining loads (Fang and Cheng, 2014), LMBAs with extended high-efficiency ranges (Quaglia and Cripps, 2018; Cao et al., 2019, 2021; Quaglia et al., 2022a), distributed efficient power amplifiers (DEPAs) (Saad et al., 2018; Lv et al., 2022), and circulator load-modulated power amplifiers (CLMAs) (Zhou H et al., 2022b, 2023). However, despite their ability to expand the high-efficiency range, these amplifier architectures often lack mismatch resilience either.

Recently, a three-way dual-mode DPA architecture has been introduced, exhibiting a remarkably-high-efficiency range against load mismatch (Pang et al., 2024). This innovation underscores the potential of multi-branch Doherty architectures to simultaneously achieve an extensive high-efficiency range and resilience against load mismatch. Nevertheless, the dual-mode reciprocal gate bias configuration employed in the three-way DPA, as described in Pang et al. (2024), necessitates the control of numerous circuit variables. This increases the complexity of the circuits, echoing the challenges encountered in other dual-mode DPAs (Li et al., 2019; Lyu et al., 2021; Lyu and Chen, 2022; Shi et al., 2023). To address this challenge, a modified sequential LMBA was introduced in Guo et al. (2023); it uses one-dimensional (1D) drain voltage control to achieve a significant high-efficiency range against load mismatch. This approach effectively reduces the number of circuit control variables. However, controlling the large drain current remains a challenge, limiting the application of this method in high-power scenarios.

In this paper, we propose a novel three-stage DPA architecture that provides a large high-efficiency range against load mismatch, through the utilization of a 1D control method. The mismatch adaptability of three-stage DPAs is analyzed in detail based on a nonlinear active device model. Additionally, a simple 1D control circuit is introduced to enhance the mismatch resilience of the proposed DPA, by changing the reactance conditions at a single control port in the proposed load modulation network (LMN).

2 Theoretical analysis

By harnessing the diverse responses exhibited by various branches in the multi-branch architecture to alterations in load impedance, it is possible to partially enhance the impedance mismatch resilience of the PA, a prime example of which is the balanced PA. Similarly, according to the theory of transmission lines, for a 90° transmission line, the change of impedance at its ends has an opposite trend when the load changes. Therefore, it can be hypothesized that a PA constructed using this structure has the potential to compensate for impedance transformations at both ports, mitigating the effects of load mismatch and thus enhancing resistance to such mismatches.

The three-stage DPA architecture has proven to be an effective way to increase the high-efficiency range. In this architecture, the carrier PA and one of the peaking PAs have a 90° phase difference. According to previous conjectures, the structure may be able to guarantee a high-efficiency range in the case of load mismatch. To discuss this ability, a nonlinear model of the current source will be established in this section to analyze the load impedance mismatch resistance of the three-stage DPA architecture. Meanwhile, a simple 1D circuit control method will be proposed to improve the load mismatch resilience.

The architecture of the proposed three-stage

DPA is shown in Fig. 1. The input power is distributed to three identical sub-PAs using a three-way equal power divider. At the output port, a modified three-stage LMN is used to combine the output power of the three sub-PAs and provide three-stage Doherty operation. By adding a reconfigurable 1D control network between the carrier PA and peaking PA_1, the reactance condition at the control port can be changed based on different load mismatch conditions, thereby improving mismatch resilience. To ensure that the currents are in the same phase at the combiner, some phase compensation lines are added in front of the sub-PAs. The load mismatch resilience performance of the proposed three-stage DPA will be discussed in detail later in this section.

2.1 Load mismatch analysis of the three-stage DPA using nonlinear current models

To analyze the operation of the proposed architecture, the modified three-stage DPA LMN in Fig. 1 is simplified to the theoretical block diagram shown in Fig. 2, where current generators (CGs) are used instead of sub-PAs, I_{ca} denotes the current of the carrier PA, and I_{pk1} and I_{pk2} denote the currents of two peaking PAs.

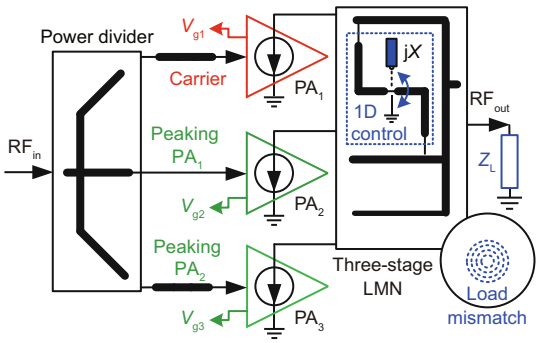

Fig. 1 The proposed three-stage DPA architecture (RF: radio frequency)

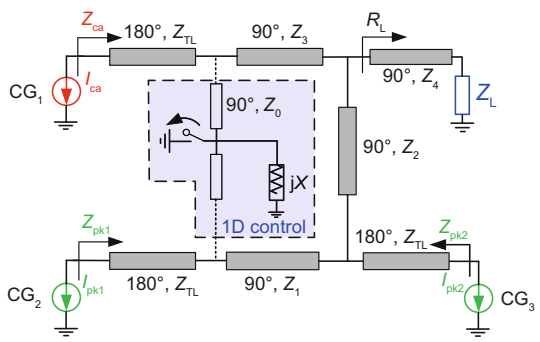

Fig. 2 Theoretical block diagram of the proposed sub-network (TL: transmission line)

When the load is matched, no control is added, and the transmission line is grounded to counteract its effect according to the characteristics of the 90° transmission line, which is then operated as shown in Fig. 3a. From Golestaneh et al. (2013), the impedance of 90° transmission lines that comprises the structure can be expressed as

$$\begin{cases} Z_1 = \dfrac{R_{\mathrm{opt}}}{k_2(\frac{1}{k_1}-1)}, \\ Z_2 = \sqrt{\dfrac{R_{\mathrm{L}}R_{\mathrm{opt}}}{k_1}}\dfrac{1}{\frac{1}{k_1}-1}, \\ Z_3 = \sqrt{\dfrac{R_{\mathrm{L}}R_{\mathrm{opt}}}{k_1}}, \\ Z_4 = \sqrt{Z_{\mathrm{L}}R_{\mathrm{L}}}, \end{cases} \tag{1}$$

where R_{L} and Z_{L} refer to the combined point load impedance and the terminal load impedance respectively, k_1 indicates the ratio of the input current to the transistor saturation current when peaking PA_1 is turned on, k_2 indicates the ratio of the input current to the transistor saturation current when peaking PA_2 is turned on, and R_{opt} indicates the optimum load impedance of the transistor. In this paper, we choose $k_1 = 1/3$, $k_2 = 0.5$, and $R_{\mathrm{L}} = R_{\mathrm{opt}}$ to achieve a high-efficiency range of 9.5 dB.

In Fig. 2, 180° transmission lines are used between the output of CGs and LMN as OMNs for load modulation, with the characteristic impedance Z_{TL} being equal to R_{opt}, and they do not participate in the load modulation process as part of the impedance transformation, thus simplifying the theoretical architecture in Fig. 2 to the four-port networks shown in Fig. 3a, where Z_{c}, Z_{p1}, Z_{p2}, Z_{out} and I_{c}, I_{p1}, I_{p2}, I_{out} denote the impedance and current of each port, respectively. The voltage–current relationship

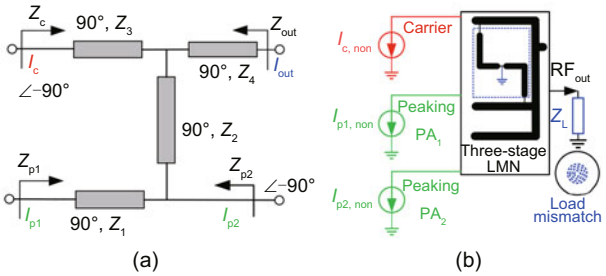

Fig. 3 Proposed initial three-stage DPA LMN when the 1D control network grounded: theoretical block diagram (a) and schematic (b) to analyze the three-stage DPA performance under load mismatch conditions using nonlinear current models

between the ports of the simplified structure shown in Fig. 3a can be expressed as

$$\begin{bmatrix} V_{\mathrm{c}} \\ V_{\mathrm{p1}} \\ V_{\mathrm{p2}} \\ V_{\mathrm{out}} \end{bmatrix} = \hat{\boldsymbol{Z}}_1 \begin{bmatrix} I_{\mathrm{c}} \\ I_{\mathrm{p1}} \\ I_{\mathrm{p2}} \\ I_{\mathrm{out}} \end{bmatrix}, \tag{2}$$

where V_{c}, V_{p1}, V_{p2}, and V_{out} denote the voltage of each port. $\hat{\boldsymbol{Z}}_1$ denotes the Z-parameter matrix of the LMN.

Based on the voltage–current transformations at each port, the Z-parameter matrix in Fig. 3a at the center frequency is derived as

$$\hat{\boldsymbol{Z}}_1 = R_{\mathrm{opt}} \begin{bmatrix} 0 & -\mathrm{j}2 & 0 & 0 \\ -\mathrm{j}2 & 0 & +\mathrm{j} & -\mathrm{j}\frac{5}{2\sqrt{3}} \\ 0 & +\mathrm{j} & 0 & 0 \\ 0 & -\mathrm{j}\frac{5}{2\sqrt{3}} & 0 & 0 \end{bmatrix}. \tag{3}$$

To simplify the analysis, the currents mentioned in Fig. 3a and Eq. (2) refer only to the current amplitude, and their phase correspondence can be described as

$$[I_{\mathrm{ca}}, I_{\mathrm{pk1}}, I_{\mathrm{pk2}}] = [-\mathrm{j}I_{\mathrm{c}}, I_{\mathrm{p1}}, -\mathrm{j}I_{\mathrm{p2}}]. \tag{4}$$

To ensure the three-stage Doherty operation, the linear current relationship of the sub-PAs can be described as

$$I_{\mathrm{c}} = \begin{cases} I_{\max} v_{\mathrm{in}}, & 0 \le v_{\mathrm{in}} < V_{\max}, \\ I_{\max}, & v_{\mathrm{in}} \ge V_{\max}, \end{cases} \tag{5}$$

$$I_{\mathrm{p1}} = \begin{cases} 0, & v_{\mathrm{in}} < V_{\max}/3, \\ I_{\max}(1.5v_{\mathrm{in}} - 0.5), & V_{\max}/3 \le v_{\mathrm{in}} < V_{\max}, \\ I_{\max}, & v_{\mathrm{in}} \ge V_{\max}, \end{cases} \tag{6}$$

$$I_{\mathrm{p2}} = \begin{cases} 0, & v_{\mathrm{in}} < V_{\max}/2, \\ I_{\max}(2v_{\mathrm{in}} - 1), & V_{\max}/2 \le v_{\mathrm{in}} < V_{\max}, \\ I_{\max}, & v_{\mathrm{in}} \ge V_{\max}. \end{cases} \tag{7}$$

According to Golestaneh et al. (2013), in Eqs. (5)–(7), the high-efficiency range can be derived as 9.5 dB when the load is matched.

To analyze the operation of DPA of this design under the condition of impedance mismatch, we change the load impedance Z_{L} on the circle of equal reflection coefficients with voltage standing wave ratio (VSWR)=2:1. In this situation, the operating state of the CG voltage and current is beyond the extent that can be described by the linear current model, so we introduce the nonlinear current model used in Chen et al. (2022) and Pang et al. (2024). Based on the linear current relationship described in Eqs. (5)–(7), and the nonlinear current model introduced in Chen et al. (2022) and Pang et al. (2024), the nonlinear current model for the three-stage DPA can be established as

$$I_{\mathrm{c,non}} = \begin{cases} I_{\max} v_{\mathrm{in}} \tanh(v_{\mathrm{ds}}/v_{\mathrm{knee}}), \\ \qquad 0 \le v_{\mathrm{in}} < V_{\max}, \\ I_{\max} \tanh(v_{\mathrm{ds}}/v_{\mathrm{knee}}), \\ \qquad v_{\mathrm{in}} \ge V_{\max}, \end{cases} \tag{8}$$

$$I_{\mathrm{p1,non}} = \begin{cases} 0, \quad 0 \le v_{\mathrm{in}} < V_{\max}/3, \\ I_{\max}(1.5v_{\mathrm{in}} - 0.5) \tanh(v_{\mathrm{ds}}/v_{\mathrm{knee}}), \\ \qquad V_{\max}/3 \le v_{\mathrm{in}} < V_{\max}, \\ I_{\max} \tanh(v_{\mathrm{ds}}/v_{\mathrm{knee}}), \quad v_{\mathrm{in}} \ge V_{\max}, \end{cases} \tag{9}$$

$$I_{\mathrm{p2,non}} = \begin{cases} 0, \quad 0 \le v_{\mathrm{in}} < V_{\max}/2, \\ I_{\max}(2v_{\mathrm{in}} - 1) \tanh(v_{\mathrm{ds}}/v_{\mathrm{knee}}), \\ \qquad V_{\max}/2 \le v_{\mathrm{in}} < V_{\max}, \\ I_{\max} \tanh(v_{\mathrm{ds}}/v_{\mathrm{knee}}), \quad v_{\mathrm{in}} \ge V_{\max}, \end{cases} \tag{10}$$

where v_{ds} and v_{knee} refer to the drain-source voltage and knee voltage at the turn-on point of the field effect transistor, respectively. Using the nonlinear current model in Eqs. (8)–(10) instead of the CGs in Fig. 2, the voltage–current relationship at each port of the four-port network shown in Fig. 3a can still be expressed by Eq. (2).

Once the current behavior is established, the operating state of the proposed DPA can be represented by the model shown in Fig. 3b, grounding the control port, i.e., without making any changes to the original three-stage DPA circuit structure. In this case, the load impedance Z_{L} is mismatched and the phase is rotated on the circle of equal reflection coefficients with VSWR=2:1 to analyze the variation of the output power and drain efficiency (DE) in the mismatched condition, and at the same time compare it with that in the matched condition. The variations of the output power and DE under the load matched and mismatched conditions are presented in Fig. 4a. It can be observed that the overall efficiency of the DPA can still be able to maintain the three-stage Doherty characteristic under load mismatch, but a high-efficiency range can

be achieved only in a part of the phase interval of VSWR=2:1. From Fig. 4a we can see that compared to the load matched condition, the saturated output power under mismatch conditions decreases by 2 dB, and the DE shows different variations depending on the VSWR phase. Nevertheless, the three-stage Doherty operation can be maintained under load mismatch conditions, while the efficiency performance decreases significantly in some VSWR phase condtions.

To better present the effect of mismatch on the output back-off (OBO) efficiency of the three-stage DPA, the back-off DE under different VSWR phase conditions is plotted in Fig. 4b. From Fig. 4b, it is evident that the DPA can still be able to maintain high efficiency at the OBO point, especially when the VSWR phase is within the ranges of [0°, 90°] and [270°, 360°], with back-off DE above 50%. However, when the VSWR phase is within the range of [120°, 240°], the back-off DE of the DPA under the mismatch condition is lower than 43%, so the circuit structure might need to be adjusted appropriately.

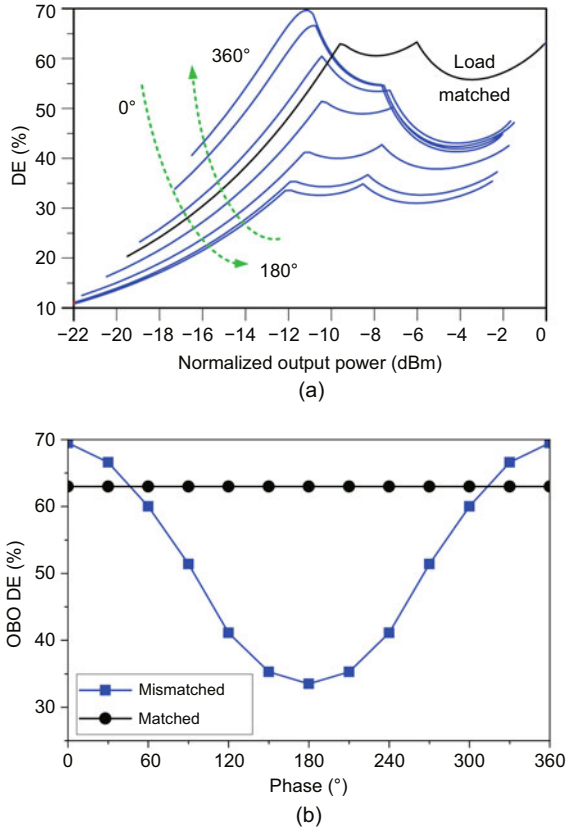

Fig. 4 Theoretical DE versus normalized output power when VSWR=2:1 within the range of [0°, 360°] (a) and DE at OBO versus phase (b)

2.2 Proposed 1D control for the three-stage DPA against load mismatch

From the above analysis, we can see that the three-stage DPA itself has a certain degree of load mismatch resilience. However, this resilience does not guarantee that the three-stage DPA maintains a high back-off DE in all VSWR phase intervals. To improve the mismatch resilience, the architecture shown in Fig. 3a has been modified, by adding a control network to reconfigure the output network of the three-stage DPA with one circuit variable. Based on the architectural nuances, the resilience of the three-stage DPA against load mismatch can be attributed to the distinct impedance variations exhibited by the carrier and peaking PA_1 under such conditions. This divergence in impedance behavior stems from the quarter-wavelength transmission line spacing between the two sub-PAs, resulting in the formation of load mismatch resilience in the overall three-stage DPA configuration. Therefore, it is natural to consider further enhancing the mismatch resilience by adjusting the impedance characteristics of these two sub-PAs. As shown in Fig. 5a, the modified 1D reconfigurable three-stage DPA is realized by adding the reactance $\mathrm{j}X$ to the outputs of the carrier and peaking PA_1 through two 90° transmission lines with a characteristic impedance of Z_0. In this scenario, the voltage–current relationship of the proposed DPA is similar to that described in Eq. (2), but the Z-parameter matrix of the modified LMN will be changed as follows:

$$\hat{\boldsymbol{Z}}_2 = R_{\mathrm{opt}} \begin{bmatrix} 0 & \frac{-\mathrm{j}2}{1+\beta} & 0 & 0 \\ \frac{-\mathrm{j}2}{1+\beta} & 0 & \frac{+\mathrm{j}}{1+\beta} & \frac{-\mathrm{j}\frac{5}{2\sqrt{3}}}{1-\beta} \\ 0 & \frac{+\mathrm{j}}{1+\beta} & 0 & \frac{-\mathrm{j}\frac{5}{4\sqrt{3}}}{\beta} \\ 0 & \frac{-\mathrm{j}\frac{5}{2\sqrt{3}}}{1-\beta} & \frac{-\mathrm{j}\frac{5}{4\sqrt{3}}}{\beta} & 0 \end{bmatrix}, \tag{11}$$

where $\beta = \frac{2x}{z_0^2}$, and z_0 and x are the normalized values of Z_0 and X for R_{opt}, respectively.

Using a similar method illustrated in Section 2.1 with the nonlinear current models, we can build a simulation schematic, as shown in Fig. 5b, to analyze the DPA operation under the load mismatch condition when considering the proposed 1D control method. Similarly, the load impedance is varied with the phase when VSWR=2:1, and the results under the load matched condition would be given as

a comparison. It is important to note that the effect of different control reactance values under load mismatch will be discrepant for the proposed DPA. As shown in Fig. 6, under the load mismatch condition, selecting different X values will result in different variations of the first back-off DE. Since the situation is similar to the second back-off point, it will not be repeated. It can be seen that for values of X between $-0.1R_{\rm opt}$ and $0.1R_{\rm opt}$, there is a significant improvement in the corresponding regions compared to the original conditions. In the following analysis, we will select two different sets of values as examples to illustrate the impact of different jX values on the proposed DPA.

First, the variation of DE versus output power under the load mismatch condition for inductive reactance jX is obtained, as shown in Fig. 7. In this scenario, X takes the value of 0.14 $R_{\rm opt}$, with $Z_0 = R_{\rm opt}$. Compared to the results obtained in Section 2.1, there are significant changes in the VSWR phase range corresponding to high-efficiency performance, while the saturated output power is

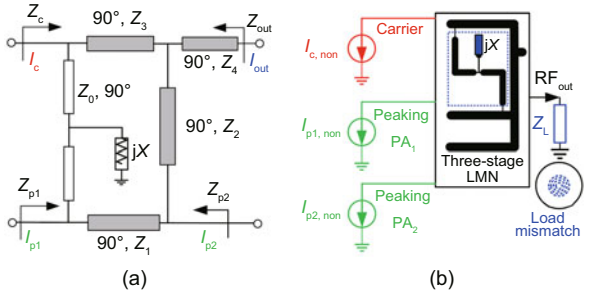

Fig. 5 Proposed 1D control LMN: theoretical block diagram (a) and schematic (b) to analyze the three-stage Doherty performance under load mismatch conditions using nonlinear current models

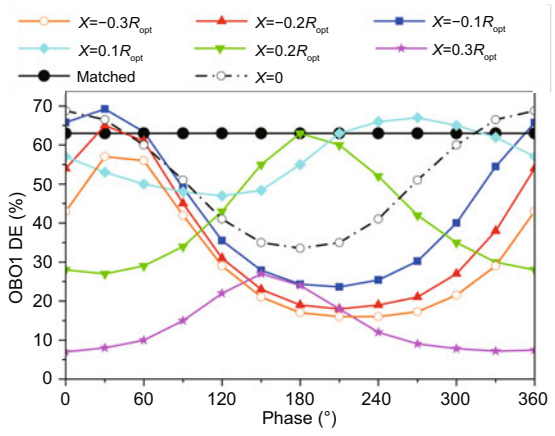

Fig. 6 Theoretical DE at OBO1 versus phase with different X values of 1D control

just slightly reduced in both [0°, 60°] and [300°, 360°] VSWR phase conditions. Defining the turn-on point for peaking $\rm PA_1$ as OBO1 and the turn-on point for peaking $\rm PA_2$ as OBO2, Figs. 7c and 7d plot the performance of DE at OBO points for different VSWR phase changes after adding the capacitive reactance, which more intuitively demonstrates that there is a great improvement in the efficiency throughout the VSWR phase range of [120°, 240°]. More than a 20% efficiency improvement can be achieved compared to the initial three-stage DPA setting. However, at other phase conditions, there is a significant reduction in the efficiency compared to the initial DPA.

Second, we consider adjusting jX to be capacitive to observe the change in the saturated output power and DE under different VSWR phase conditions. By tuning the control reactance X in the opposite direction towards a capacitive reactance of $-0.04R_{\rm opt}$, a similar simulation is performed again. The simulation produces diverse DE outcomes with varying VSWR phases, monitoring the DE precisely at the OBO points, as shown in Figs. 8c and 8d. As clearly depicted in Fig. 8, there is a discernible reduction in the saturated output power within the angular range of [120°, 240°]. Conversely, a remarkable improvement in efficiency is observed within [0°, 60°], whereas a substantial decrease in efficiency is evident at other phase angles.

From the above analysis, we can see that by switching the control reactance to zero (ground connection) or different jX values of 1D control, the efficiency performance exhibited by the proposed three-stage DPA under load mismatch conditions can be significantly improved. Comparing Figs. 7 and 8, we can see that using different jX values in different phase ranges can achieve better mismatch resistance. To more visually see the impact of 1D reconfiguration on OBO1 efficiency, the comprehensive outcome of this control method is graphically depicted in Fig. 9. Compared to the case where no adjustments are made to the circuit, reconfiguration through 1D circuitry can lead to a significant increase in circuit performance in the presence of mismatches. By choosing different reactance values at the control port, it becomes feasible to regulate the DE to surpass 47% even in the presence of a load mismatch. Meanwhile, over 60% back-off DE can be obtained in most VSWR phase conditions.

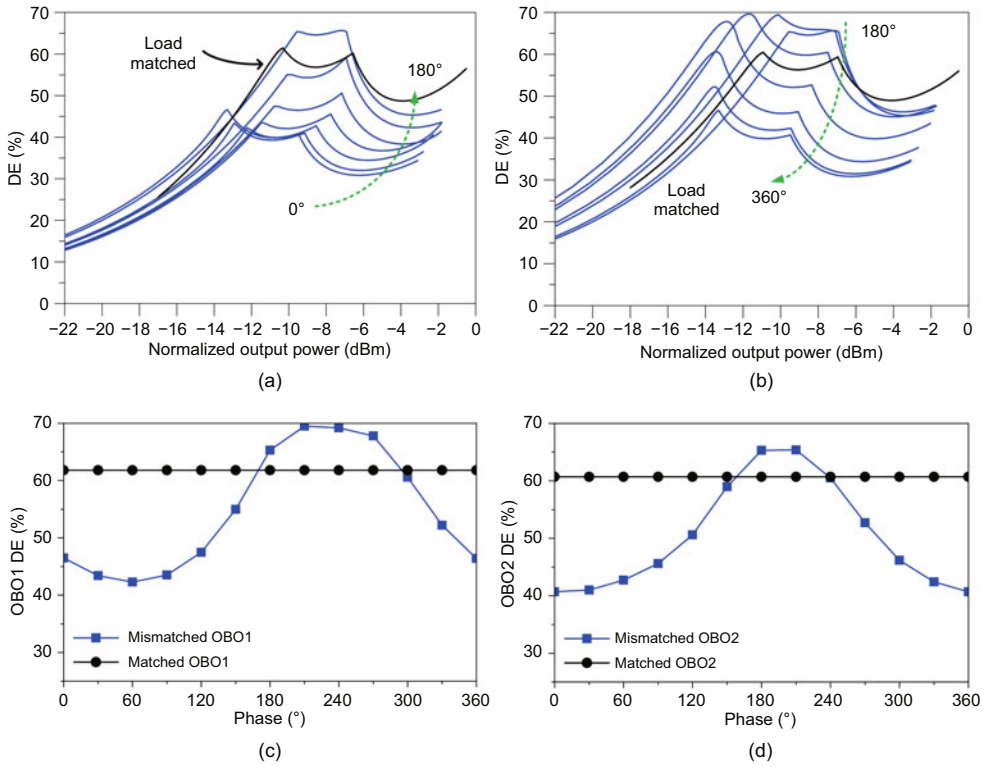

Fig. 7 Theoretical DE versus normalized output power within the ranges of [0°, 180°] (a) and [180°, 360°] (b), and DE at OBO1 (c) and OBO2 (d) versus phase at inductive reactance jX modulation

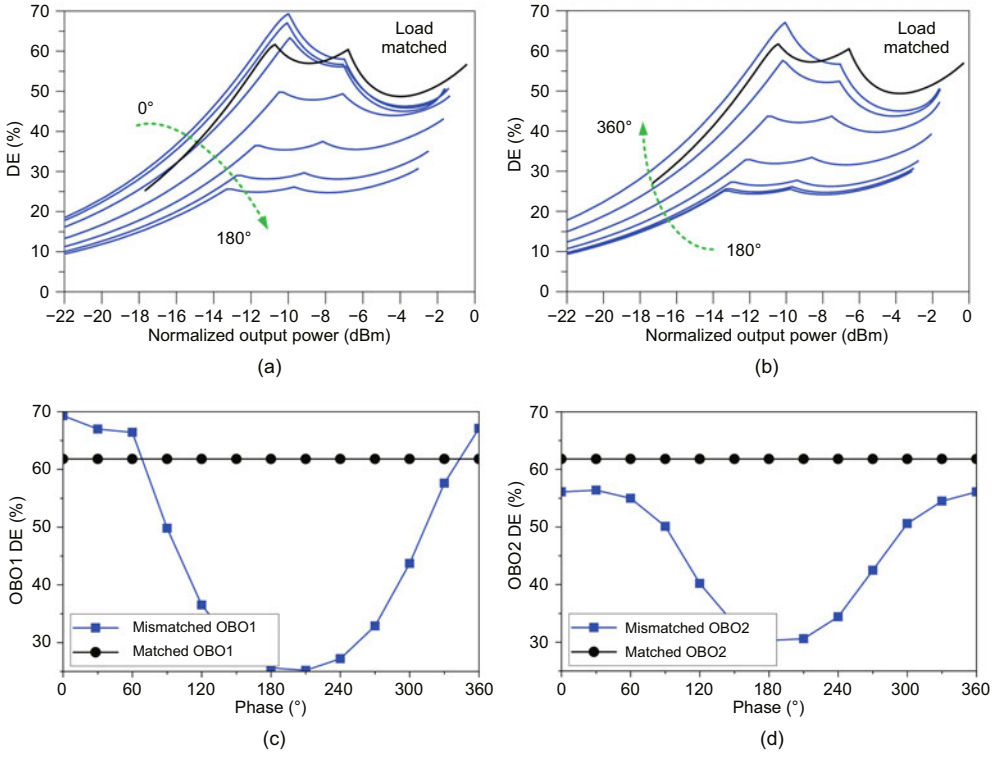

Fig. 8 Theoretical DE versus normalized output power within the ranges of [0°, 180°] (a) and [180°, 360°] (b), and DE at OBO1 (c) and OBO2 (d) versus phase at capacitive reactance jX modulation

3 Circuit design

In the previous section, the theoretical feasibility of the proposed 1D reconfigurable three-stage DPA architecture for resilience against load mismatch was established. This section aims to validate this theory by designing a three-stage DPA operating at 2 GHz, adhering to the aforementioned architecture. The target design specifications include a high-efficiency OBO range of 9.5 dB for matched loads, with an anticipated maintenance of a high-efficiency range of 8 dB under VSWR conditions of 2:1. For this design, we have chosen the gallium nitride (GaN) transistor CG2H40010F from Wolfspeed to serve as the carrier PA and peaking PAs. These transistors have a maximum output current $I_{\max}$ of 1.5 A, and all three sub-PAs operate with the same drain voltage of 28 V. When operating in class B, the optimal output impedance of the PA R_{opt} is 32 Ω. The actual substrate used for fabrication is Rogers 4350B, which boasts a dielectric constant ε_{r} of 3.66 and a thickness of 20 mil (that is 0.508 mm), ensuring high performance and reliability for the DPA design.

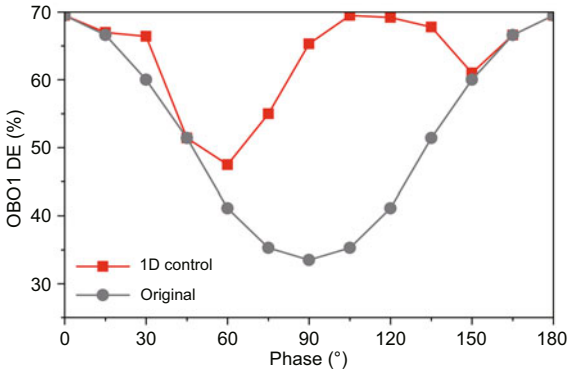

Fig. 9 Theoretical DE at OBO1 versus phase with and without 1D control

Fig. 10 provides a detailed insight into the designed DPA circuit, highlighting its specific dimensions. A two-stage three-way power divider serves as the initial component, effectively dividing the input signal's power into three equal parts. From Fig. 11, it can be seen from the simulation of passive and active models that the designed power divider has good performance at the operating frequency. However, due to the varying turn-on points of the three sub-PAs, which induce a phase difference in the currents, it is necessary to incorporate corresponding phase compensation lines before the input matching networks (IMNs).

The sizing of these compensation lines necessitates careful consideration of the subsequent layout, while ensuring that the carrier PA and peaking PA_2 maintain a 90° phase difference from peaking PA_1. The IMN design has been optimized with a T-shaped structure, and capacitors and resistors have been incorporated to guarantee circuit stability. For the sake of simplicity, an identical IMN has been employed for all three sub-PAs.

The OMN needs to match the optimal

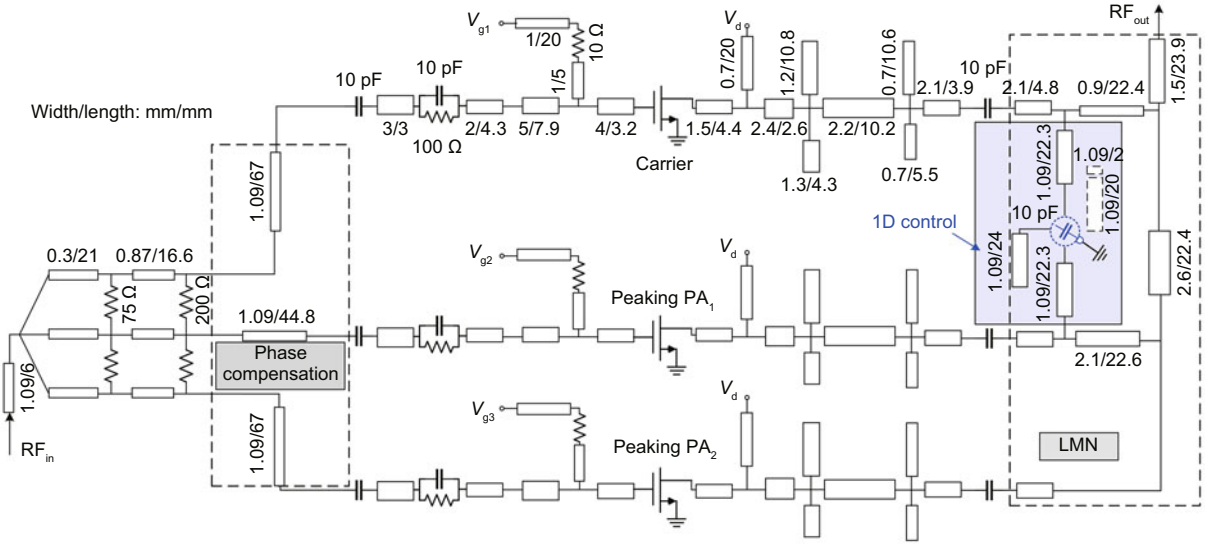

Fig. 10 Circuit details of the proposed three-stage DPA

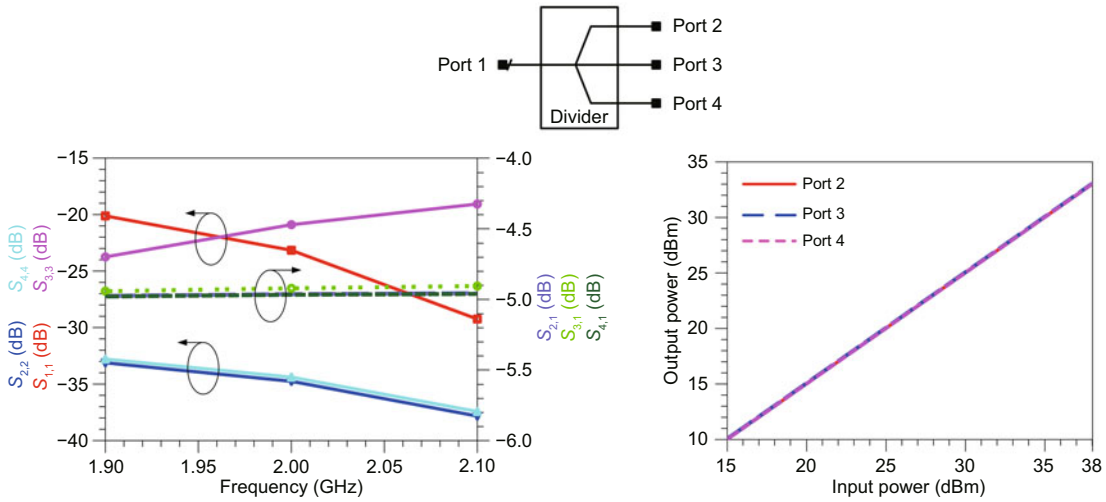

Fig. 11 Simulated *S*-parameters and output power versus input power of the three-way divider (References to color refer to the online version of this figure)

impedance of the transistor at the CG plane to the characteristic impedance of the LMN, while absorbing the parasitic and package parameters, as shown in Fig. 12. Since the impedance of the transistor output and the characteristic impedance of the LMN are both R_{opt}, OMN together with the package parameters is equivalent to a 180° network with an equivalent characteristic impedance $Z_{\mathrm{TL}} = R_{\mathrm{opt}}$. To enhance the efficiency of the designed DPA, four open transmission lines with varying electrical lengths have been integrated for harmonic suppression. All three sub-PAs employ identical OMNs. LMN is designed using the structure discussed in Section 2, comprising four 90° transmission lines. For realizing the proposed 1D control, additional 90° transmission lines are positioned between the carrier PA and peaking PA_1, which can be terminated to ground or control reactance. By connecting to different reactance values, distinct 1D tuning effects can be achieved. In the practical design, different reactance values are realized using open-circuit transmission lines with different electrical lengths. Considering that the potential effects of the coupling of lines in the fabricated DPA will lead to inaccuracy in the measurement, a number of transmission lines with slightly different lengths have been added for tuning in the 1D control section. Furthermore, leveraging the unique properties of 90° transmission lines, when the control port is grounded, the circuit reverts to an untuned state.

To measure the DPA performance with different phases when VSWR=2:1, it is necessary to design

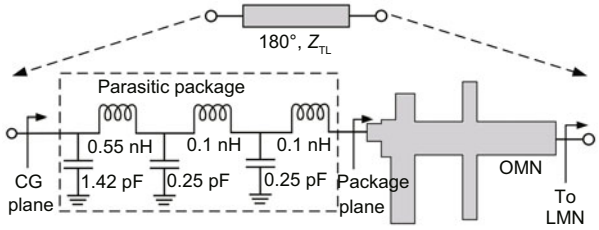

Fig. 12 Equivalent OMN containing package parameters

an external component for impedance change and phase adjustment. Therefore, a 90° transmission line with a characteristic impedance of 70.7 Ω is first used to transfer the load impedance to 100 Ω, and then several transmission lines with different lengths are used to change the VSWR phase for different mismatch conditions. The layout of this mismatch tuner is shown in Fig. 13. A small capacitor is used for switching, which does not affect the results.

After designing the circuit, we need to build an Ebers–Moll model of the entire circuit and observe the performance through harmonic balance simulation. Fig. 14 shows the variation of DE and gain with output power for the designed DPA when the load is matched. As can be seen from Fig. 14, when the 1D control port is grounded, the DPA has a saturated output power of 46.3 dBm and DE of 70.8% at saturation, and can achieve 59.4% DE at 9.5 dB OBO, with load matching to 50 Ω.

Next, the performance of the designed DPA under mismatch conditions is simulated. With 1D circuit reconstruction, the DPA can select the optimal

case at different phases. When VSWR=2:1, the DPA achieves a saturated output power of 45.2–45.8 dBm, saturated DE of 55.0%–74.6%, saturated gain of 7.2–7.8 dB, and DE of 49.6%–59.8% at 8 dB OBO, as shown in Fig. 15. It can be seen that the DPA maintains good performance under load mismatch conditions, in both output power and DE.

The difference between the saturated output power of the DPA in the matched and mismatched states is less than 1.5 dB. The DPA still exhibits good performance in the presence of load mismatch compared to that when it is matched, thus confirming its resilience under load mismatch conditions.

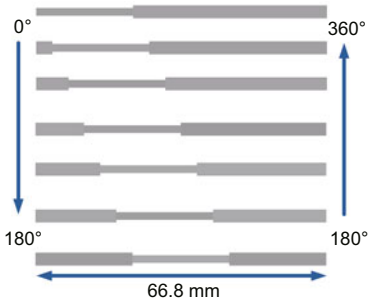

Fig. 13 Phase adjustment from 0° to 360° with VSWR=2:1

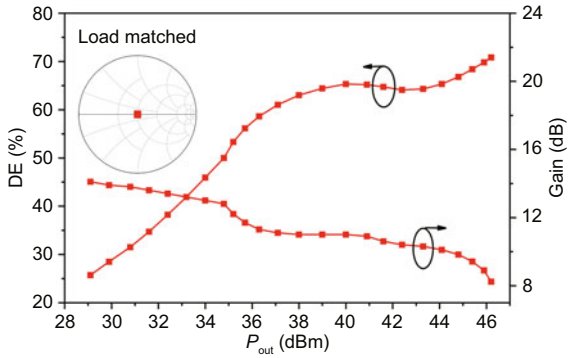

Fig. 14 Simulated DE and gain versus output power in the matched load condition

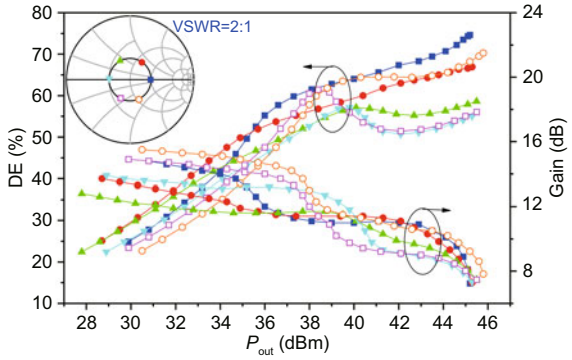

Fig. 15 Simulated DE and gain versus output power under different load mismatch conditions when VSWR=2:1

For a clearer comparison of DPA performance under worse conditions, we simulate the DE and gain when VSWR=3:1, as shown in Fig. 16. The mismatch resistant property is still demonstrated compared to the case without 1D control, but with more performance degradation. Based on the theory above, it is reasonable to think that taking more stages of DPA or more complex control parts may achieve greater load mismatch resilience under the worse conditions. Since power amplifiers with load mismatch resilience are designed under VSWR=2:1, we use VSWR=2:1 for comparison and the overall performance consideration. The DPA circuits will be fabricated and measured then.

4 Measurement results

The photo of the fabricated three-stage DPA is shown in Fig. 17. The three sub-PAs use the same drain supply voltage of 28 V. Depending on the turn-on sequence, the gate voltage is set to −2.8 V for the carrier PA, −4.5 V for the peaking PA_1, and −6 V for the peaking PA_2, with a quiescent current of 60 mA. Similar to the simulation, the fabricated DPA will be tested in both matched and mismatched states.

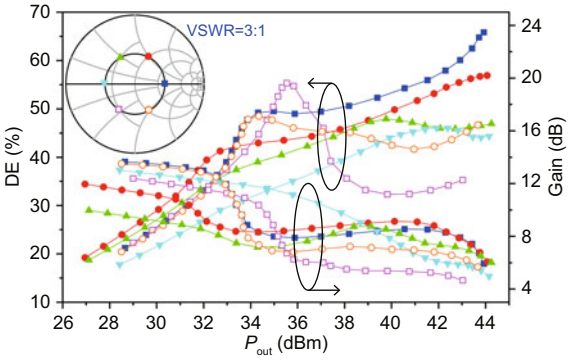

Fig. 16 Simulated DE and gain versus output power under different load mismatch conditions when VSWR=3:1

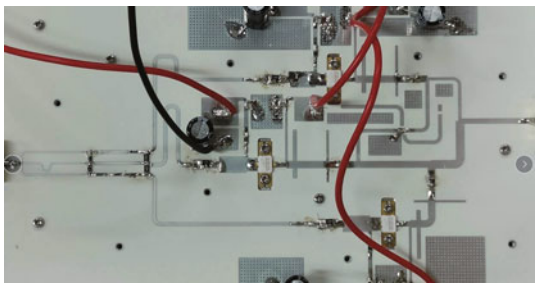

Fig. 17 Photograph of the fabricated three-stage DPA

Fig. 18 shows the platform used for measurement. The input signal is generated by a vector signal generator (VSG) and the signal is fed into DPA through a driver and an isolator. When the DPA is measured for a matched load, its output is connected to an attenuator and finally the results are displayed on the vector spectrum analyzer (VSA). When the DPA is measured under mismatch conditions, a designed VSWR tuner is used between the DPA output and the attenuator to adjust the impedance and VSWR phase to achieve different mismatch conditions. To better demonstrate the performance of the DPA, both continuous-wave (CW) and modulated measurements are performed.

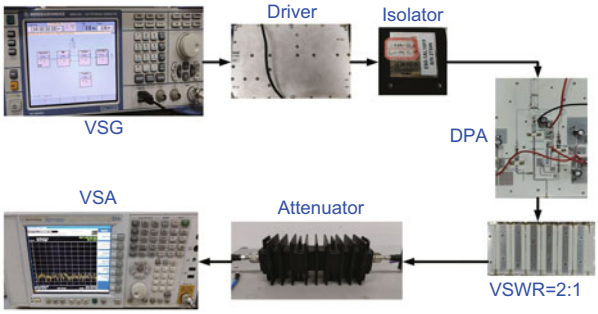

Fig. 18 Measurement setup for testing the proposed DPA

4.1 CW signal measurements

The three-stage DPA is initially assessed using CW signals. Under the matched load conditions, the output impedance is set to 50 Ω, and the 1D control port is grounded, indicating that the circuit is not actively regulated. Consequently, the DE and gain versus output power at this particular moment are depicted in Fig. 19. Upon reaching saturation, the DPA demonstrates an output power of 45.2 dBm, accompanied by DE of 73.1% and gain of 7.9 dB, and the DE maintains 51.0% at 9.5 dB back-off. However, when comparing these measurement results to the simulation ones, a certain degree of performance degradation is observed. This degradation could be attributed to the intricate complexity of the circuit design and the inevitable discrepancies in phase and harmonic behavior that arise due to the inherent gap between simulation and the actual physical conditions. Nevertheless, the fabricated DPA continues to exhibit a large efficiency range.

When assessing the performance of the DPA under load mismatch conditions, 1D control is then employed to optimize the circuit. By adjusting the reactance at 1D control port, the output power at saturation can be elevated to 43.4–45.3 dBm, with a DE ranging from 56.5% to 66.5%, a gain ranging from 6.2 to 7.8 dB, and a DE of 47%–55.1% at 8 dB OBO. Fig. 20 illustrates the variation in DE and gain of the DPA with respect to the output power under varying mismatch conditions. As shown in Fig. 20, the DPA responds differently to 1D control under diverse phase conditions during load mismatch. This overall trend aligns with the analysis presented in Section 2 and further validates the necessity of incorporating 1D control in the design of a three-stage DPA.

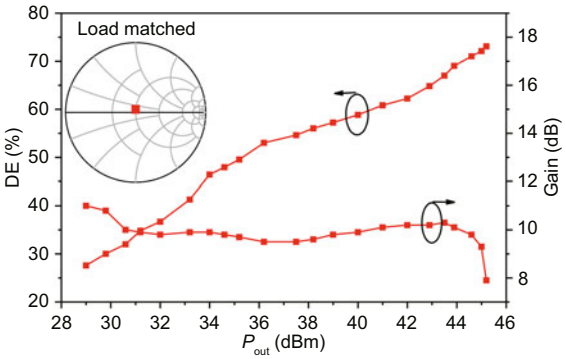

Fig. 19 Measured DE and gain versus output power of the fabricated DPA for the matched load condition

To further illustrate the performance of the DPA under mismatch conditions and better demonstrate the usefulness of 1D reconfigured circuits, test results using 1D reconfiguration are compared to those of the initial circuits. Fig. 21 is presented, highlighting the saturated output power, saturated DE, and the DE at 8 dB OBO for various VSWR phases. It also depicts the performance of the DPA across different modes of 1D control. By comparing these performances, the optimal mode of 1D control is identified and connected with a green solid line in the figure. The selection of the DPA's 1D control mode is based on its performance. Specifically, within the VSWR phase range of [120°, 240°], the DPA's DE is better in its original state with the 1D control port grounded. Additionally, for the VSWR phase ranges of [0°, 100°] and [260°, 360°], switching to the jX mode enables the DPA to achieve a superior operating state under mismatch conditions.

In summary, the introduction of the proposed 1D control reconfiguration has allowed the fabricated

DPA to achieve a saturated output power ranging from 43.4 to 45.3 dBm under load mismatch conditions, while maintaining a saturated DE of 56.5% to 66.5%. Notably, even at an output power back-off of 8 dB, the DE remains stable at 47% to 55.1%. The negligible difference in the saturated output power, $\leq$2 dB, between the matched and mismatched states of the DPA suggests that this three-stage design with 1D control exhibits good resilience against load mismatch.

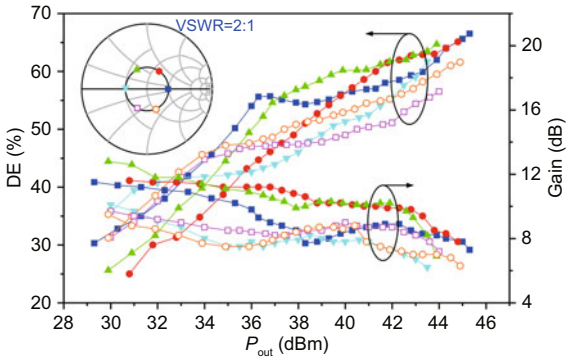

Fig. 20 Measured DE and gain versus output power under different load mismatch conditions

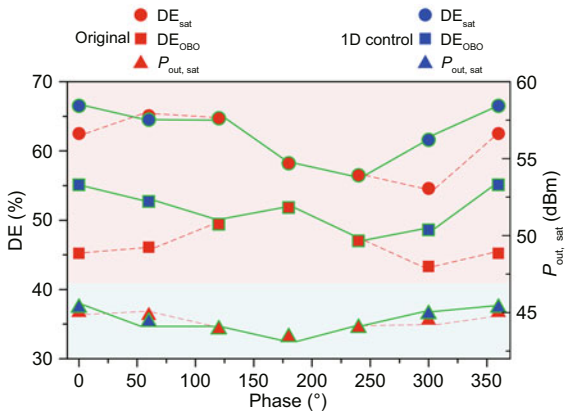

Fig. 21 Measured DE and saturated output power versus phase under different load mismatch conditions when VSWR=2:1 (References to color refer to the online version of this figure)

4.2 Modulated signal measurements

To demonstrate the performance of the fabricated three-stage DPA in practical wireless communication applications, the DE and adjacent channel power ratio (ACPR) of the DPA at the OBO point are measured using a modulated signal with a bandwidth of 20 MHz and a PAPR of 8 dB.

At an average output power of 35.2 dBm, the DPA exhibits an average DE of 46.7% and an ACPR better than −24.4 dBc. Subsequently, under the load mismatch condition with a VSWR of 2:1, the DPA's performance is measured across various VSWR phase points. For illustrative purposes, the output spectra corresponding to VSWR phase angles of 60° and 180° are shown in Fig. 22.

To comprehensively illustrate the resilience of the DPA to load mismatch at VSWR=2:1, Fig. 23 depicts the output power, average back-off DE, and ACPR as a function of the mismatch VSWR phase. Fig. 23 demonstrates that, upon switching the 1D control port, the fabricated DPA achieves an average output power of 35.5–37.3 dBm, coupled with an average DE of 46.9%–53.9% and an ACPR better

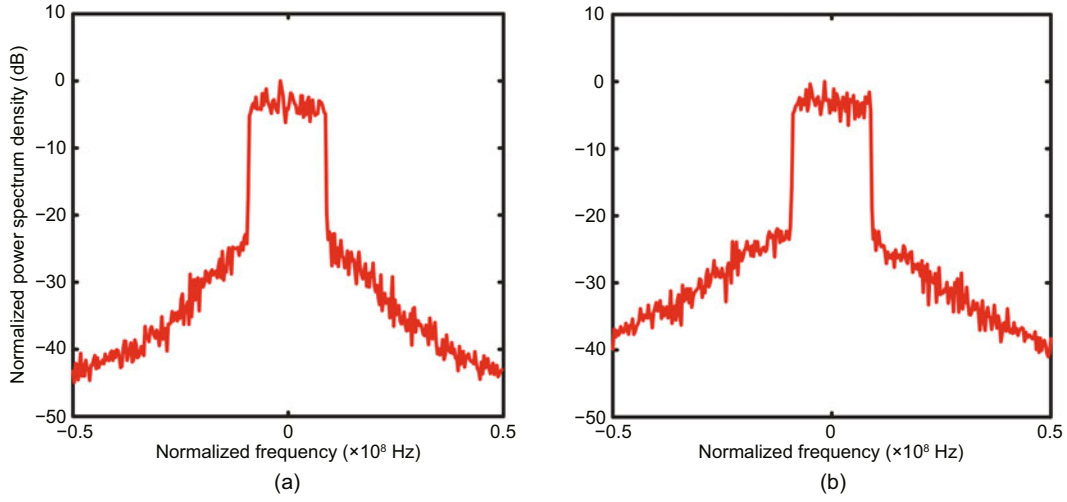

Fig. 22 Output spectrum of the proposed DPA with load mismatch at 60° (a) and 180° (b) with 1D control

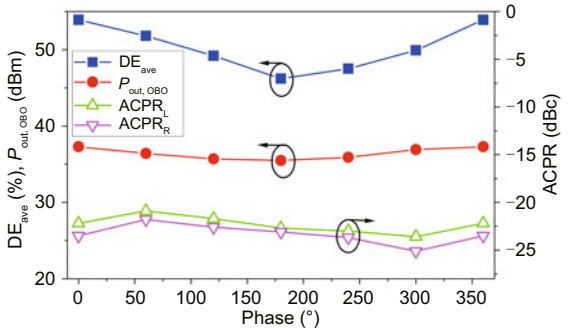

Fig. 23 Average DE, output power, and ACPR over 2:1 VSWR under modulated signal stimulations with 1D control

than −21 dBc.

4.3 Performance comparison

Table 1 provides a comparison of the proposed 1D reconfigurable three-stage DPA with load mismatch resilience, against similar types of PAs reported in recent years. Upon comparing key performance metrics such as saturated output power, high-efficiency range, DE, and control variables, it becomes evident that the proposed DPA achieves comparable performance under load mismatch conditions using a lower-dimensional circuit reconfiguration approach. This underscores the effectiveness and simplicity of the proposed design.

5 Conclusions

In this paper, the load mismatch resilience of three-stage DPA is analyzed based on nonlinear current models. To further improve the mismatch resilience, a novel three-stage DPA with a very simple 1D circuit control method is then proposed. A DPA operating at 2 GHz is designed to verify the proposed method and architecture. The designed DPA has a 9.5 dB OBO DE of 51% for matched load and maintains DE of 47%–55.1% at 8 dB OBO against load mismatch when VSWR=2:1. The proposed three-stage DPA architecture with 1D control offers a brand-new solution to provide load mismatch insensitivity with a very simple circuit configuration.

Contributors

Yi ZHANG and Jingzhou PANG designed the research. Yi ZHANG drafted the paper. Ruibin GAO, Shuang LIU, Yujie HAN, Meng REN, and Hanhui LIN helped organize the paper. Jingzhou PANG revised and finalized the paper.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Table 1 Performance comparison of recently published PAs with load mismatch adaptability

Reference	Frequency (GHz)	Control variable	Load Z_0=50 (Ω) P_{sat} (dBm)	Load Z_0=50 (Ω) DE_{sat} (%)	Load Z_0=50 (Ω) OBO (dB)	Load Z_0=50 (Ω) DE* (%)	VSWR=2:1 P_{sat} (dBm)	VSWR=2:1 DE_{sat} (%)	VSWR=2:1 OBO (dB)	VSWR=2:1 DE* (%)
This work	2	1D	45.2	73.1	9.5	51.0	43.4–45.3	56.5–66.5	8	47.0–55.1
Gonçalves et al. (2022)	3.6	2D	43.5	64	5	53	42.6–43.4	49–64	5	35–46
Shi et al. (2023)	2.4	3D	43.4/43.7	69.1/70.8	6	>60	41.5–43.3	52.8–60.7	6	50.1–62.5
Guo et al. (2023)	2.1	1D	42**	72**	10	64**	39.1–40.9	60.1–66.4	10	43.0–62.8
Pang et al. (2024)	2.0	3D	46.4/46.7	70.3/72.2	9	62.8/60.7	44.8–46.3	50.2–65.8	9	47.8–56.7

* At 8 dB OBO; ** graphically estimated. P_{sat}: saturation output power; DE_{sat}: saturation drain efficiency

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