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STUDY OF THE EFFECTIVENESS OF ANTI-PHASE TECHNIQUE FOR COMMON MODE NOISE SUPPRESSION*

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Abstract: This paper discusses the properties of a novel boost converter with auxiliary anti-phase winding approach resulting in low conducted common code noise level. A simplified equivalent circuit of the proposed boost converter is modeled to analyze its performance and to show the influence of the parasitic winding capacitance, as well as the stray capacitances of the switching waveform nodes into the earth plane. Simulation and experimental results are shown to verify the concept.

Key words: anti-phase technique, EMI(Electromagnetic Interference) model, boost converter
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INTRODUCTION

As switching mode power supply (SMPS) has become increasingly sophisticated, common mode suppression techniques involving low cost and compact packaging are called upon to perform a more important role in complying with regulatory limits. In a typical boost converter, common mode (CM) EMI is caused mainly by a transient voltage with high dv/dt through stray capacitance between the switching nodes (drain and gate) and the earth, or by a transient current with high di/dt through stray inductances. The total EMI generated in a converter can be suppressed significantly if common mode noise can be efficiently suppressed. An anti-phase technique was proposed to cancel common mode noise from the generation point (drain node) (Wu et al., 1999) To put this technique into practice, the influences of the parasitic capacitances have to be further investigated. Therefore a detailed verification of the effects of parasitic winding capacitances on the efficacy of the proposed technique are studied in this work.

COMMON MODE CIRCUIT MODEL ANALYSIS

For economic reasons, EMC should be considered in the earlier stages of equipment design. As the first step, the engineers should analyze the equipment's EMI generation characteristics so that it is possible to determine the required level of EMI suppression.

Generally speaking, EMI noise (Paul et al., 1992) is produced and conducted by a stray capacitance C_s through the earth (third terminal of LISN). It can couple the harmonics of the switching waveform into the earth plane as undesired current. Because of the thin insulating layer between the heatsink with large surface area and the power MOSFETs, this stray capacitance C_s toward the earth can reach up to approximately 100 pF.

This CM EMI measured from LISN can be very effectively controlled by reducing either the CM current or the stray capacitance C_s between the heatsink and the earth, C_s being responsible for conducting the CM noise current.

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To simplify the analysis for the circuit, the following assumptions are introduced.

1. Ignore the parasitic coupling capacitances C_P and C_N to two terminals P(Phase) and (N) Neutral of the LISN as shown in Fig. 1.

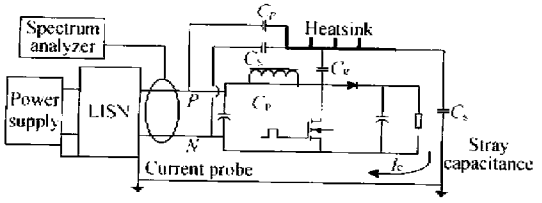

Fig. 1 Boost converter circuit configuration with general model of non-conductive path to the LISN terminals

2. The conductive CM emission is mainly due to the critical CM current through the stray capacitance C_s.

To illustrate the principle, a simple conventional boost converter configuration was set up as shown in Fig. 1. A CM current probe was clamped around the input cable of the converter to measure the CM current, displayed by a spectrum analyzer; and an LISN was inserted at the input stage of the circuit to present a constant impedance (50) between the phase conductor and the earth.

The conventional boost converter circuit is redrawn in Fig. 2a. Since the capacitance of C_s was so large that it could be approximately treated as shorted to the earth; the equivalent circuit can be shown in Fig. 2b.

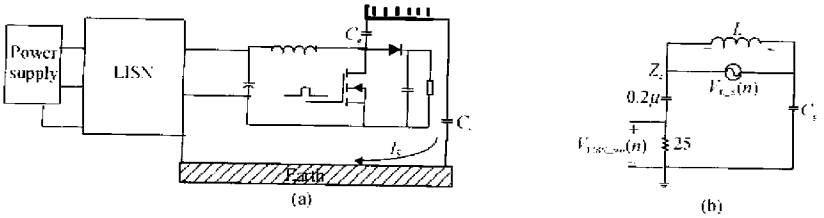

Fig. 2 A conventional boost converter and its CM EMI equivalent circuit
(a) circuit schematic; (b) equivalent circuit of CM noise

The voltage V_{LISN_wo} across the testing terminals of LISN can be deduced from Fig. 2. (Franki et al., 2000; William et al., 1994; Jefferey et al., 1993):

$$V_{\mathrm{LISN\_wo}}(n) = \left| \frac{r}{z_g(n) + Z_c(n) + r} \times V_{\mathrm{n\_s_1}}(n) \right| \quad (1)$$

$V_{\mathrm{LISN\text{-}wo}}(n)$: The CM voltage detected from LISN without anti-phase winding;

$V_{\mathrm{n\text{-}S1}}(n)$: The nth harmonic amplitude of the voltage across the main switch;

$Z_g(n) = 1/jn2\pi \times f_s \times C_g$: The corresponding impedance of the stray capacitance C_g;

$Z_C(n) = 1/jn\pi 2 \times f_s \times C$: The corresponding impedance of the LISN capacitance, $C = 0.2\ \mu$F;

r: The corresponding resistance of LISN ($r = 25\Omega$) $n = 1, 2, \cdots 30 \times 10^6/f_s$: The number of harmonics used as variable in conductive frequency range;

f_s: The switching frequency.

ANTI-PHASE WINDING APPROACH ANALYSIS

After inserting the anti-phase winding (Wu et al., 1999), the boost converter circuit configuration becomes as shown in Fig. 3a, where C_g is the stray capacitance between the power MOSFET drain node and heatsink, C_{cg} is the stray capacitance from the anti-phase winding to the heatsink, C_s is the stray capacitance from the heatsink to the earth, and C_w is the capacitive coupling between the opposite terminals of the transformer windings. These capacitances constitute common mode emission coupling paths in the proposed boost converter with an anti-phase winding (Wu et al., 1999; 2000). The equivalent circuit of the proposed boost converter is shown in Fig. 3b.

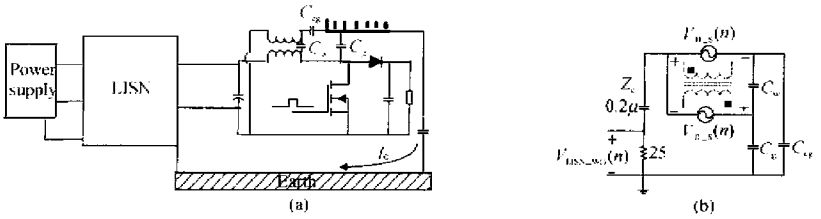

Fig.3 Proposed boost converter with an anti-phase winding
(a) circuit configuration; (b) common mode noise equivalent circuit

Referring to Fig.3b, the $V_{LISN\text{-}w}(n)$ can be deduced as following:

$$V_{LISN\_w}(n)=\left|\frac{[(Z_{c1}(n)+Z_{c2}(n))(Z_{c1}(n)+Z_{c3}(n)+r+Z_c(n))+Z_{c1}(n)+Z_{c2}(n)+2(Z_{c3}(n)+r+Z_c(n)]}{[(Z_{c1}(n)N+Z_{c2}(n))(Z_{c1}(n)+Z_{c3}(n))+r+Z_c(n))\times(Z_{c2}(n)+Z_{c3}(n)+r+Z_c(n))]}\right|\times$$
$$\left|\frac{\{(Z_{c2}(n)+Z_{c3}(n)+Z_c(n))[Z_{c1}(n)\times N+Z_{c2}(n)+2(Z_{c3}(n)+r+Z_c(n))]\}}{[(Z_{c1}(n)N+Z_{c2}(n))(Z_{c1}(n)+Z_{c3}(n)+r+Z_c(n))(Z_{c2}(n))+Z_{c3}(n)+r+Z_c(n))]}\times(rV_{n\_S1}(n))\right| \quad (2)$$

Where,

$Z_c = (j2n)^{-1} f_s C$

$Z_{cg} = (j2n)^{-1} f_S C_{cg}$

$Z_{c1}(n) = Z_{cw}(n)Z_g(n)/[Z_g(n) + Z_{cw}(n) + Z_{cg}(n)]$

$Z_{c2}(n) = Z_{cw}(n)Z_{cg}(n)/[Z_g(n) + Z_{cw}(n) + Z_{cg}(n)]$

$Z_{c3}(n) = Z_g(n)Z_{cg}(n)/[Z_g(n) + Z_{cw}(n) + Z_{cg}(n)]$

$V_{LISN\text{-}w}(n)$: The common mode voltage picked up by LISN with an anti-phase winding;

N: The transformer turn ratio;

Z_{cw}: The corresponding impedance of the winding parasitic capacitance C_w.

SIMULATION AND EXPERIMENTAL RESULTS

Based on the Eq. (1) the simulation result of conducted common mode noises generated in a conventional boost converter is shown in Fig.4.

While noises generated in a converter with an anti-phase winding with different values of C_w, 1 pF, 0.5 pF, and 0.1 pF, are shown in Fig.5.(a), Fig.5(b) and Fig.5(c) respectively based on Eq.(2). In the simulation other parameters used for calculation are: $n = 1$, $C_g = C_{cg} = 2.23$ pF, which can be calculated by using Finite Element Method (FEM).

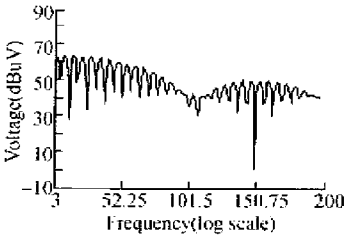

Fig.4 Simulated conducted common mode noise without anti-phase winding
($N = 1$, $C_g = C_{cg} = 2.23$ pF)

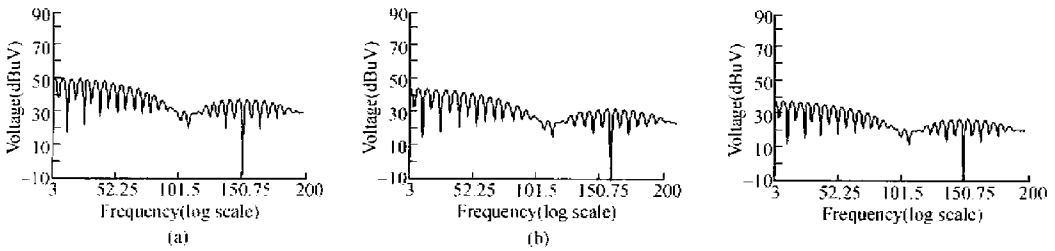

Fig.5. Simulation results of the conducted common mode noise with anti-phase winding ($n = 1$, $C_g = C_{cg} = 2.23$ pF)
(a) $C_w = 1$ pF; (b) $C_w = 0.5$ pF; (c) $C_w = 0.1$ pF

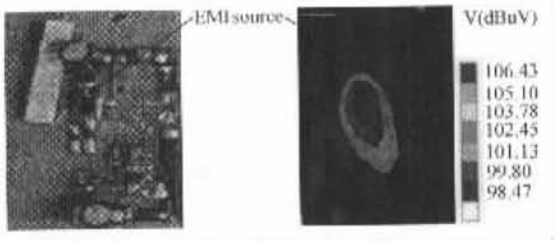

Fig.6 PCB of the boost converter
(a) photograph of the top side of PCB;
(b) electric field distribution on the PCB;
(frequency range: 0.45MHz-30MHz)

To verify the theoretical analysis and simulation results shown above, experimental evaluations were carried out in the lab. Firstly a typical boost converter was built up, then the printed circuit board (PCB) was scanned in a frequency range from 0.45 MHz to 30 MHz with an EMI scanner EPS3000, using a vertical electrical field probe. Fig.6(a) is a photograph of the top side of the PCB. The electric field distribution on the PCB plane of the converter is shown in Fig.6(b). From the photos shown in Fig.6, one can see that the strongest CM EMI emission comes from the drain node of the main switch. It travels through the stray capacitance of the heatsink to the earth. To evaluate the effectiveness of the anti-phase technique, the inductor L in the boost converter was replaced by an anti-phase transformer constructed on the same ferrite core with unity turns ratio ($n = 1$), as shown in Fig.3(a). In the experiments the parasitic capacitance C_w was changed by slightly altering the gap distance between the primary and secondary windings; and was measured by an impedance analyzer, HP4194. The spectrum of common mode noise current was measured with an HP8710 – 1744 RF current probe with bandwidth of 100 Hz – 50 MHz, and a spectrum analyzer, HP8591EM. An intermediate gain/phase amplifier with gain of 28 dB and frequency range 9 kHz – 1300 MHz and a transient limiter (– 10 dB/ 9 kHz – 200 MHz) were also used. The measured conducted common mode noise spectrum of the converter without anti-phase winding is shown in Fig.7(a), noise spectrum with anti-phase windings and with $C_w = 44$ pF, 26 pF, and 16 pF are shown in Fig.7(b), Fig.7(c), and Fig.7(d) respectively. The experimental results shown in Fig.7 show that the CM noise level decreases by almost 7dB in magnitude and envelope with decrease of the parasitic winding capacitance C_w.

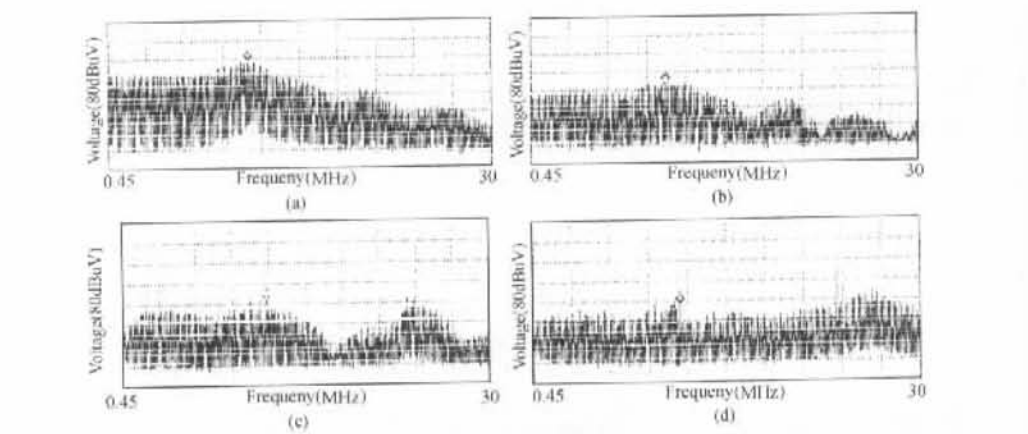

Fig.7 Experimental results of the conducted common mode noise spectrum
(a) without anti-phase winding; (b) with anti-phase winding $C_w = 44$ pF;
(c) with anti-phase winding $C_w = 26$ pF; (d) with anti-phase winding $C_w = 16$ pF

The parasitic capacitance C_w in the antiphase transformer can be effectively reduced by placing a shielding layer between the windings. Similar to the static shielding layer commonly applied in a normal transformer, the shielding layer consists of a thin copper sheet, properly

placed between the primary and secondary windings, to provide both good electrical isolation and connection to the ground plane (earth) as shown in Fig.8(a). The experimental results are shown in Fig.8(b) and Fig.8(c).

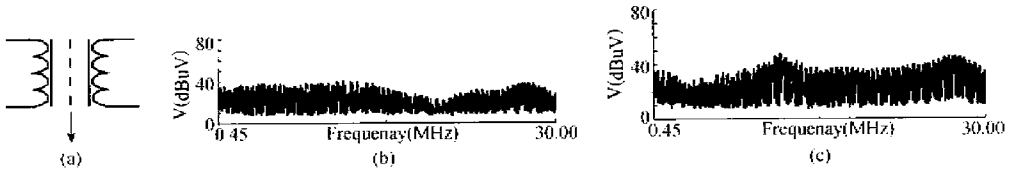

Fig.8 Experimental results of the shielding effect on the conducted common mode noise spectrum
(a) equivalent circuit of shielded transformer; (b) before shielding C_w = 20 pF; (c) after shielding C_w = 17 pF

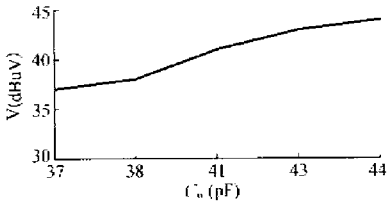

Fig.9 Experimental results of maximum conducted common mode noise versus the parasitic winding capacitance C_w.

The influence of the parasitic winding capacitances C_w on conducted CM noise is confirmed by the experimental results shown in Fig.7 and Fig.8, for frequency range of 0.45 MHz to 30 MHz. As shown in Fig.9, C_w should be smaller in order to achieve lower common mode EMI reduction level.

CONCLUSIONS

Anti-phase technique is an efficient solution for suppressing common mode current in a boost converter. However, the parasitic capacitance between the transformer windings C_w plays an important role. The stray capacitances C_g and C_{cg} from the switching waveform nodes of the anti-phase circuit into the earth have similar effect on common mode EMI reduction. Hence, an engineer should be aware of the above mentioned capacitive coupling effect and pay more attention to the layout and careful construction of the anti-phase transformer.

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