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Average modeling of Single Stage Flyback PFC + Flyback DC/DC converter*

SHEN Miao-sen(沈淼森), KANG Wan-ying(康婉莹), QIAN Zhao-ming(钱照明)†

(*Power Electronics Research Institute, Zhejiang University, Hangzhou 310027, China*)

† E-mail: qian@cee.zju.edu.cn

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Abstract: With the use of this novel average model for Single Stage Flyback PFC + Flyback DC/DC converter, voltage control mode, peak current control mode and average current control mode can be simulated easily by changing the model's parameters. It can be used to do various analysis not only for small signal and static behavior but also for large signal and dynamic behavior of the converter. By using this average model the simulation speed can be improved by 2 orders of magnitude above that obtained by using the conventional switched model. It can be applied to optimize the trade-off between high power factor, voltage stress, current stress and good output performance while designing this kind of single stage PFC converter. A 60W single stage power factor corrector was built to verify the proposed model. The modeling principle can be applied to other Single Stage PFC topologies.

Key words: average model, power factor correction, single stage
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INTRODUCTION

PFC circuitry simulation has some inherent difficulties, as two frequencies have to be considered during simulation: one is the switching frequency of about 50kHz, another is the mains frequency of 50 to 60 Hz. It causes an extremely large dynamic operation range. To surmount these difficulties, several models for large signal characterization (Sun et al., 1999) and small signal behavior (Zhu et al., 1998) were designed. It is well known that Single Stage PFC (SSPFC) combines a PFC circuit and a DC/DC converter into one circuit with only one switch, so it is less costly compared with two stage PFC (TSPFC). Because several important electrical characteristics, such as total harmonic distortion (THD), output voltage ripple, efficiency, current stress and voltage stress, involved, one has to consider certain compromises between these characteristics during designing (Qian et al., 1997). For example, to obtain good output performance, one has to reduce the requirement for power factor correction. It is true the other way round. To optimize the trade-off, a suitable average model for SSPFC becomes attractive. There were many SSPFC topologies proposed recently (Qian et al., 1997; Redl et al., 1995; Schenk et al., 1997), but few for modeling SSPFC average behavior, until now.

This novel average model for Flyback PFC + Flyback DC/DC converter (Qian, 1997) is based on the developed general average model for DC/DC converters (Ren, et al., 2000). It can be used for simulation not only of small signal and static behavior but also of large signal and dynamic behavior; and can also be used in voltage control mode, peak current control mode and average current control mode.

PRINCIPLE OF MODELING

The circuitry of the Single Stage Flyback PFC + Flyback DC/DC converter (SSFFPFC) is shown in Fig. 1. The power stage of the circuit consists of a rectifier, two transformers T_1 and T_2, a bulk capacitor C_b, a switch S and the load R_L.

To simplify the analysis, some assumptions for the circuit are given as follows:

1. The parasitic capacitance of the windings of T_1 and T_2 can be ignored.

2. The coupling coefficient between the primary winding and the secondary winding of the transformers equal unity. So the leakage inducta-

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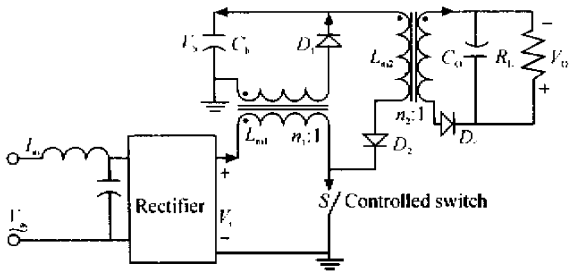

Fig.1 The scheme of the Single Stage Flyback PFC + Flyback DC/DC

nces of T_1 and T_2 are ignored.

3. The switch frequency is much higher than the mains frequency, so the voltage across C_b and the output voltage of the rectifier can be considered as constants during one switching cycle. Based on the assumptions above, the equivalent circuit can be shown by Fig. 2. L_{m1} and L_{m2} are the exciting inductances of the transformers, T_1 and T_2 indicate ideal transformers.

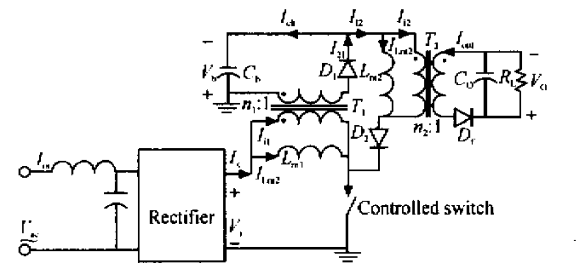

Fig.2 The equivalent circuit of the circuit in Fig.1

When the switch S is on, both of the magnetizing currents i_{Lm1} and i_{Lm2} increase linearly, and there is no current through both ideal transformers. When the switch is off, i_{Lm1} and i_{Lm2} decrease linearly and it is easy to see that: $i_{Lm1} = -i_{i1} = i_{21}/n_1$, $i_{Lm2} = -i_{i2} = i_{out}/n_2$. So the currents flowing in the transformers T_1 and T_2 can be regarded as converted currents i_{Lm1} and i_{Lm2}. Fig.3 (a) and (b) show the magnetizing currents (i_{Lm1} or i_{Lm2}) for the transformers in discontinuous conduction mode (DCM) and continuous conduction mode (CCM) respectively.

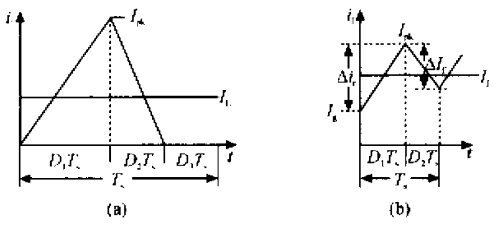

Fig.3 The magnetizing currents of the transformers during one cycle
(a) DCM mode operation (b) CCM mode operation

For switch being off at $D_1 T_s$, the magnetizing current decreases to zero at $(D_1 + D_2)T_s$ in DCM. In CCM operation, $D_2 T_s$ is the switch – off time in a cycle. From the developed general average model for DC/DC converters (Ren et al., 2000), we can directly obtain the following equations:

$$L_{m1}\frac{\Delta I_{Lm1}}{\Delta t} = V_i \times D_1 - V_b \times n_1 \times D_{2m1} + 0 \times D_{3m1} \quad (1)$$

$$D_1 + D_{2m1} = \left|\frac{2I_{Lm1}f_s L_{m1}}{V_i D_1}\right|_{D_1}^{1} \quad (2)$$

$$D_{3m1} = 1 - D_1 - D_{2m1} \quad (3)$$

$$L_{m2}\frac{\Delta I_{Lm2}}{\Delta t} = V_b \times D_1 - V_o * n_2 \times D_{2m2} + 0 \times D_{3m2} \quad (4)$$

$$D_1 + D_{2m2} = \left|\frac{2I_{Lm2}f_s L_{m2}}{V_b D_1}\right|_{D_1}^{1} \quad (5)$$

$$D_{3m2} = 1 - D_1 - D_{2m2} \quad (6)$$

Where f_s is the switching frequency, V_i is the input voltage and V_b is the voltage across C_b, V_o is the output voltage. n_1 and n_2 are the turns ratios of T_1 and T_2 respectively. D_{2m1} and D_{3m1} are the values of D_2 and D_3 (shown in Fig. 3) for L_{m1}. D_{2m2} and D_{3m2} are the values of D_2 and D_3 for L_{m2}.

V_i in (1) and (2) is given by input voltage source, and D_1 is determined by the modulator, so V_b and V_o are the most important values to be calculated. For the capacitor C_b:

$$V_b = \frac{1}{C_b}\int_{-}^{t} i_{cb}\,dt + V_{b0} \quad (7)$$

Where i_{cb} is the current through the capacitor, V_{b0} is the initial voltage across C_b. From Fig.2, we can see that $i_{cb} = i_{21} - i_{12}$. Here we will discuss the most complicated case: when both waveforms of I_{Lm1} and I_{Lm2} are in CCM as shown in Fig. 3(b). From Fig. 2 and Fig.3,

We can get the following equations:

$$I_{Lm1} = I_{gm1} + D_1 \times \Delta I_{rm1}/2 + D_{2m1} \times \Delta I_{rm1} - D_{2m1} \times \Delta I_{fm1}/2 \quad (8)$$

so: $$I_{gm1} = I_{Lm1} + D_{2m1} \times \Delta I_{fm1}/2 - D_1 \times \Delta I_{rm1}/2 - D_{2m1} \times \Delta I_{rm1}/2 \quad (9)$$

$$I_{pkm1} = I_{gm1} + \Delta I_{rm1} \quad (10)$$

$$I_{nm1} = I_{pkm1} - \Delta I_{fm1} \quad (11)$$

$$I_{Lm2} = I_{gm2} + D_1 \times \Delta I_{rm2}/2 + D_{2m2} \times \Delta I_{rm2} - D_{2m2} \times \Delta I_{fm2}/2 \quad (12)$$

so: $$I_{gm2} = I_{lm2} + D_{2m2} \times \Delta I_{fm2}/2 - D_1 \times \Delta I_{rm2}/2 - D_{2m2} \times \Delta I_{rm2}/2 \quad (13)$$

$$I_{pkm2} = I_{gm2} + \Delta I_{rm2} \quad (14)$$

$$I_{nm2} = I_{pkm2} - \Delta I_{fm2} \quad (15)$$

$$\Delta I_{rm1} = V_i \times T_s \times D_1/L_{m1} \quad (16)$$

$$\Delta I_{fm1} = V_b \times n_1 * T_s \times D_{2m1}/L_{m1} \quad (17)$$

$$\Delta I_{rm2} = V_b \times T_s \times D_1/L_{m2} \quad (18)$$

$$\Delta I_{fm2} = V_0 * n_2 \times T_s \times D_{2m2}/L_{m2} \quad (19)$$

$$I_{21} = (I_{pkm1} + I_{nm1}) \times D_{2m1} \times n_1/2 \quad (20)$$

$$I_{12} = (I_{gm2} + I_{pkm2}) \times D_1/2 \quad (21)$$

In which I_{nm1}, I_{pkm1}, I_{gm1}, ΔI_{rm1}, ΔI_{fm1} are the values of I_n, I_{pk}, I_g, ΔI_r, ΔI_f (shown in Fig. 3) for L_{m1}, I_{nm2}, I_{pkm2}, I_{gm2}, ΔI_{rm2}, ΔI_{fm2} are the values of I_n, I_{pk}, I_g, ΔI_r, ΔI_f for L_{m2}. T_s is the switching period. From Fig.2, we can get $I_{cb} = I_{21} - I_{12}$. From the above equations, we can calculate V_b in CCM + CCM (both exciting inductors operate in CCM). These equations are also applicable for other modes (DCM + CCM, CCM + DCM, DCM + DCM). For any inductor operating in DCM: $I_g = I_n = 0$, $\Delta I_f = \Delta I_r$, $I_L = \Delta I_r \times D_1/2 + \Delta I_f \times D_2/2$, these are exceptional case equivalents of Eqs. (8) and (12). In order to calculate V_o we can calculate the output current I_{out} first. It is easy to see that:

$$I_{out} = (I_{pkm2} + I_{nm2}) \times D_{2m2}/2 \quad (22)$$

The model given in this paper also integrates the power stage of the circuit with the PWM modulator. It is the same as discussed by Ren (2000), and shown in Fig. 4 (a). V_b is connected to the bulk capacitor, V_c is the port to the switching duty cycle control signal, the output of V_r is the rectified input voltage which is used to shape the input current in current control mode, I_{sense} is the input current sample.

APPLICATIONS AND COMPARISONS

Based on all these equations deduced above, we can establish a related template, then use SABER simulator to perform simulation. The average modeling circuit for SSFFPFC in voltage control is shown in Fig.4 (b). Considering the effect of the filter on the mains frequency current, the filter is still used in the circuit when using the average model.

In this circuit, $n_1 = 1$, $n_2 = 2$; the switch frequency is 50kHz, the input voltage frequency

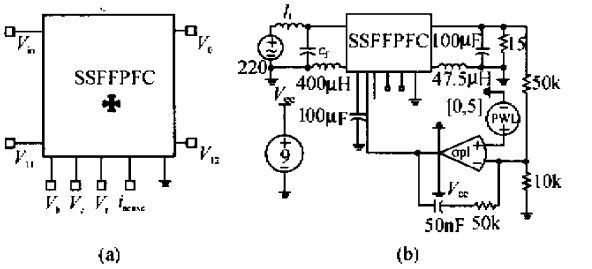

Fig.4 (a) the average model for SSFFPFC and (b) the simulation circuit using it in voltage control mode

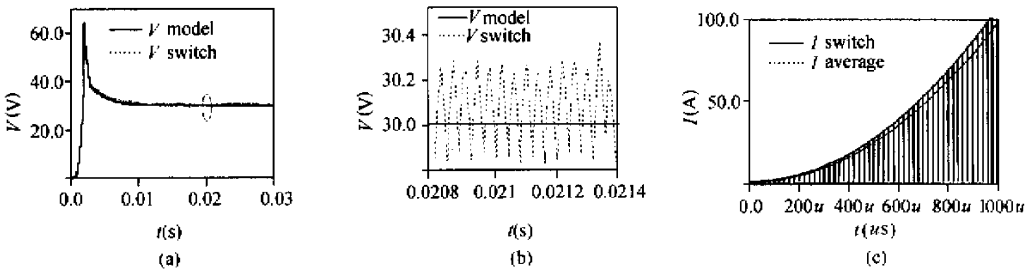

Fig.5 comparison of the simulation results of the circuit using average model and switched model
(a), (b)output voltage; (c)input current

is 50Hz, other parameters are shown in Fig.4 (b). Fig. 5 shows a comparison of the simulation results for the input current (c) and the output voltages at starting time between average model analysis (solid line) and conventional switched model analysis (dashed line) with the same parameters. To see more clearly, Fig. 5 (b) enlarges the curve section in the cycle region shown in Fig.5 (a). Table 1 shows a comparison of the time consumed in transient analysis (0 – 10ms) of use of the average model with use of the switched model while using ideal components in different control modes.

Table 1 Time consumed in simulation between average model and switched model in different control modes

Control modes	Time consumed using different model	
	Average model	Switched model
Voltage control mode	0.317	39.2
Peak current control mode	1.52	84.3
Average current control mode	1.78	71.8

To verify the validity of the proposed model, a 60W experimental circuit was built. Fig. 6 is the experimental circuit of the tested SSFFPFC in voltage control mode, where (a) is the PWM generator, (b) is the whole circuit with the same

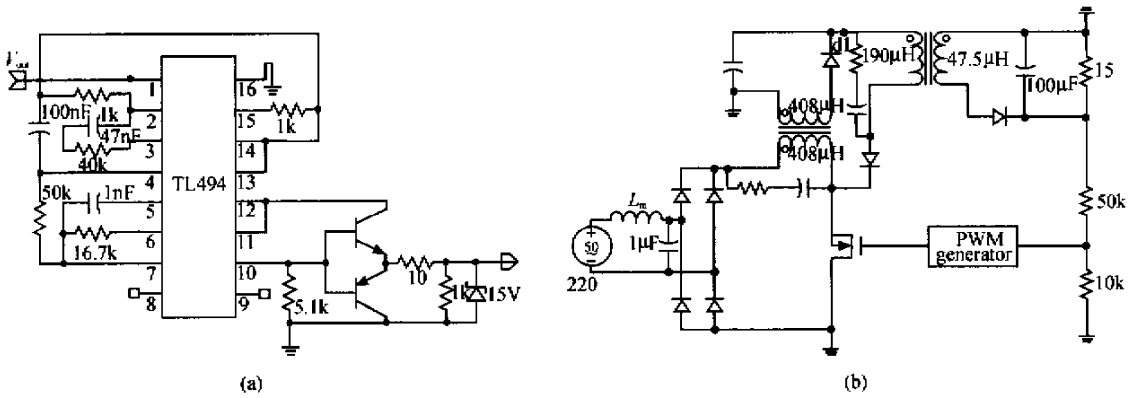

Fig.6 Experimental circuit of SSFFPFC
(a) PWM generator in(b); (b) the whole circuit

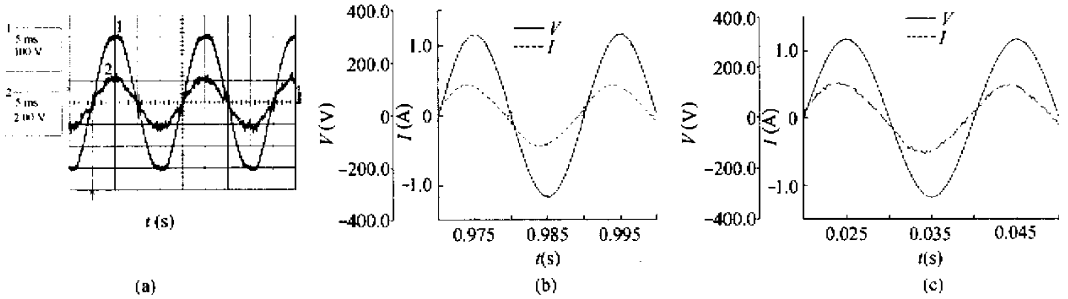

Fig.7 Input current and input voltage
(a) experimental result; (b) simulation result using average model; (c) simulation result using switched model

component parameters used in simulation. The experimental results for the input current and input voltage and the simulation result for the input current and input voltage using average model and switched model (also in voltage control mode) are shown in Figs.7 (a), (b) and (c) respectively.

The proposed average model can also be used in average current control mode and peak current control mode. Fig. 8 shows the simulation circuit using the model in average current control mode. Result of small signal analysis (V_o/V_c) in voltage control mode and average current control mode are shown in Fig. 9. The proposed model can be easily used to optimize the trade-off while designing a SSFFPFC

circuit. For example, Table 2 and Table 3 give some simulation results for the input current THD (THD), output voltage ripple (Ripple), and peak current (I_{peak}) through L_{m1} with various values of L_{m1} and different control modes respectively.

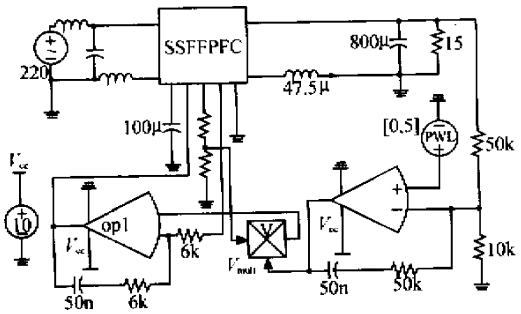

Fig.8 The circuit using the average model in average current control mode

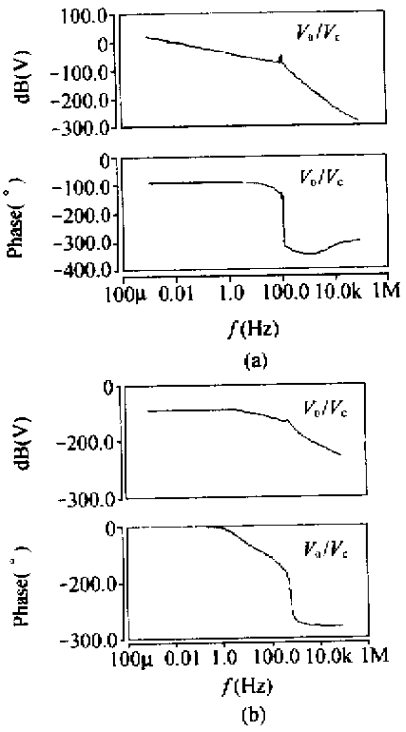

Fig.9 Simulation result (Vo/Vc) of small signal analysis
(a) Voltage control mode; (b) average current control mode

The operation principle of other SSPFC topologies, such as Boost PFC + Buck DC/DC converter are quite similar to the SSFFPFC converter, so the modeling principle proposed in this paper can be applied to them too.

Table 2 THD, Ripple and I_{peak} for different L_{m1} in voltage control (other parameters are the same as those in Fig.4)

Value of L_{m1} (μH)	Ripple(V)	THD(%)	I_{peak}(A)
400	0.15	3.75	3.49
500	0.21	4.68	3.12
680	0.32	17.6	3.22

Table 3 THD, ripple and I_{peak} for different L_{m1} in average current control (other parameters are shown in Fig.8)

Value of L_{m1} (μH)	Ripple(V)	THD(%)	I_{peak}(A)
400	1.15	7.81	3.52
500	1.13	10.7	2.81
680	1.10	10.9	2.85

CONCLUSIONS

The proposed average model for SSFFPFC can work very well in voltage control mode, average current control mode and peak current control mode. The simulation speed is much faster than that of the conventional switched model. So it is valuable to optimize the trade-off in designing a SSFFPFC circuit. Based on this model, it is easy to deduce the average model of other SSPFC topologies.

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