Analysis and design of DSP-based dual-loop controlled UPS inverters

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Received Aug.30, 2002; revision accepted Oct. 29, 2002

Abstract: This paper presents a novel digital dual-loop control scheme of the PWM(Pulse width modulate) inverter. Deadbeat control technique are employed to enhance the performance. Half switching period delayed sampling and control timing strategy is used to improve the system dynamic response. Simulation and experimental results presented in the paper verified the validity of the proposed control scheme.

Key words: Digital control, Inductor-current mode, Dual-loop
Document code: A **CLC number:** TN86

INTRODUCTION

With the rapid development of information technology and the internet, widespread applications of personal computers, the reliability of the power supply systems has become more important. Since UPS (uninterrupted power supplies), with a core part-the CVCF PWM inverter, play an important role in various application areas, more rigid quality specification is required for UPS. Traditional analog control strategies for PWM inverter contain many crucial components, whose temperature drift and aging parts will deteriorate the systems' long time stability. Since the programmability of the DSP chip offers flexibility in designing a control loop, it is much easier to incorporate an advanced control algorithm, which can hardly be implemented with its analog counterpart. Therefore, DSP(digital signals processor) based digital control techniques can greatly improve the uniformity of the products, and increase the stability and reliability of the UPS systems(Tzou *et al*., 1997).

This paper presents a digital dual-loop control scheme for regulation of UPS inverters. The proposed scheme can achieve satisfactory steady-state characteristics and fast dynamic response. The paper is organized as follows: Section II describes the structure of the proposed UPS inverter system. Section III discusses the designs of digital dual-loop controller which includes current and voltage loops. Section IV presents the simulation and experimental results of the UPS inverter. Section V contains the conclusion.

UPS INVERTER SYSTEM DESCRIPTION

Fig.1 shows the proposed digital controlled UPS inverter system with a resistive load. The

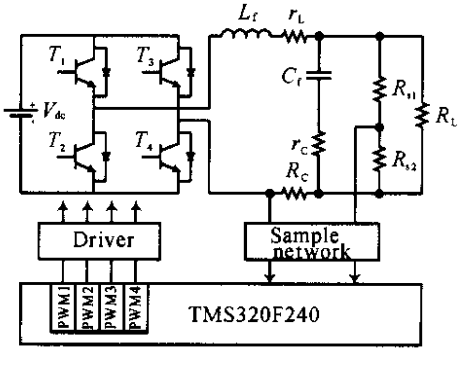


Fig.1 UPS inverter system with resistive load

UPS inverter system consists of a full bridge inverter, LC output filter and a single-chip DSP TMS320F240 from Texas Instruments (1997). The voltage source V_{dc}, which is often the output of the PFC power stage, delivers power to the load through the inverter. L_f is the filter inductor and C_f is the filter capacitor. The resistor r_c is

the equivalent series resistor(ESR) of the capacitor, while the resistor r_L is the ESR of the inductor. To lower the costs and ensure the control precision of the system, the resistor method for sensing inductor current and output voltage is employed. R_{s1} and R_{s2} are the output voltage sensing resistors and R_c is the inductor current sensing resistor. The sensed signals input to a dual 10-bit ADC module embedded in DSP through the sample network. Four PWM output channels generate PWM signals to control the power switches. Both the continuous model and discrete model of PWM inverter had been discussed in Jung *et al*. (1996). This paper focuses attention mainly on digital control techniques.

DIGITAL CONTROLLER OF UPS INVERTER

1. The structure of digital dual-loop controller

Many existing control approaches for PWM inverters are based on analog control techniques which are not as reliable as digital techniques (Wu *et al*., 2000). This paper presents an inductor-current mode dual-loop PI control scheme. Fig.2 is the block diagram of the proposed dual-loop controlled UPS inverter. Contents in dashed frame represent the LC filter and resistive load. The switch converter is modeled as an amplifier with constant gain K_{PWM}. Two signals are sensed as feedbacks: inductor current (i_L), output voltage(v_o). Inductor current is sensed to regulate the current inner loop. The output voltage is sensed to track the sinusoidal waveform. V_{ref} is a pure sinusoidal lookup table stored in the flash program memory embedded in the DSP chip. To suppress the high frequency noises and improve the sampling precision, low-pass filter made up of R_1R_2 and C_1C_2 is employed between the sensed signals and analog-to-digital converters. The proposed digital controlmer works as follows:

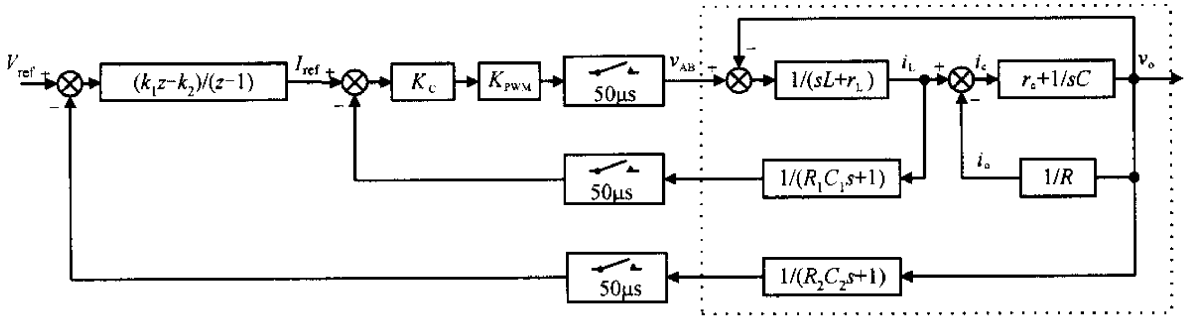


Fig.2 Block diagram of the proposed dual-loop controlled UPS inverter

The output voltage is compared with a sine reference V_{ref}, the error voltage is compensated by a digital PI regulator to produce the current reference I_{ref}. The sensed inductor current is compared with I_{ref} and compensated by a P-regulator; the output of the current loop is compared with a digital triangle waveform generated by a DSP built-in 16 bit timer and 4 channel PWM signals are accurately generated by the PWM module in the DSP chip.

2. The timing design of sampling and control

A novel sampling and control timing strategy is shown in Fig.3. One switching period is from t_0 to t_4. Doubled frequency unipolar sinusoidal pulse-width modulation is employed and the frequency of the ripple current of filter inductor twice that of the switching frequency. Because of the doubled frequency of the ripple current, the sizes of filter components can be greatly reduced. The timing strategy is as follows:

$t_1 - t_2$: Two channel ADCs are started to sample the output voltage and inductor current and at t_1 the timer period interrupt. ADCs ends the conversion at t_2.

$t_2 - t_3$: The digital control algorithms are implemented during this interval.

t_4: The calculated control register CMPRx is loaded at t_4, the timer underflow interrupt.

Obviously, in this sampling and control timing strategy, the newly calculated pulse width is applied with only half of the switch period delay

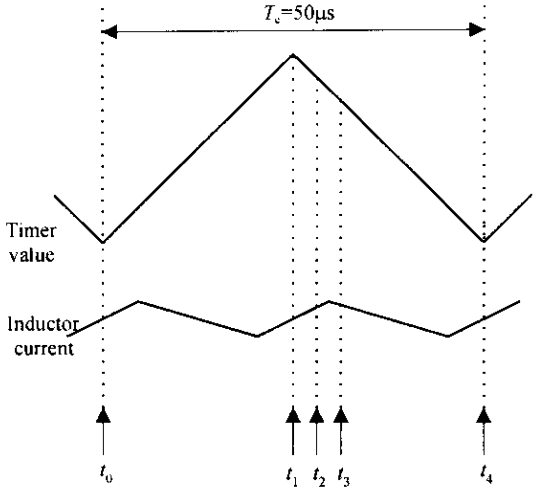


Fig.3 Timing diagram sampling and control

due to the AD conversion time and program implementation time. In fact, many digital control applications have one switch period delay (Zhang *et al.*, 2000; Jung *et al.*, 1997; Low, 1999). The proposed timing strategy shortens the time delay, and so, improves the dynamic response of control systems. Simulation and experimental results also confirm it.

3. Design of current loop and voltage loop

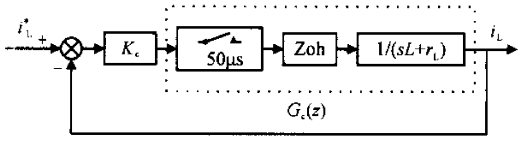


Fig.4 Block diagram of current inner loop

Fig.4 shows the simplified block diagram of the current inner loop, Zoh block represents a zero-order holder and its transfer function in s-plane is:

$$G_h(s)=\frac{1-e^{-T_s s}}{s} \tag{1}$$

where T_s is the sampling period. In this paper, the sampling periods of the current loop and voltage loop are both 50 μs. The open loop transfer function of current loop in z-plane is:

$$G_C(z)=Z\left(\frac{1-e^{-T_s s}}{s}\cdot\frac{1}{sL}\right)=\frac{T_s}{L}\cdot\frac{1}{z-1} \tag{2}$$

The inductor ESR r_L is omitted. The characteristic equation of the closed current loop is:

$$1+K_C\cdot\frac{T_s}{L}\cdot\frac{1}{z-1}=0 \tag{3}$$

To achieve deadbeat effect, let the root of Eq. (3) be located at zero, then we can get:

$$K_C=\frac{L}{T_s} \tag{4}$$

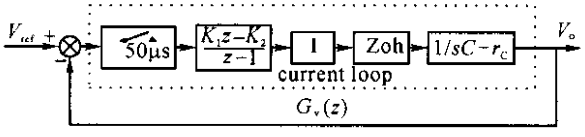


Fig.5 Block diagram of voltage outer loop

Fig.5 shows the simplified block diagram of the voltage outer loop, where

$$\frac{K_1z-K_2}{z-1}$$

is the general form of the digit PI regulator for the voltage outer loop. Since the tracking speed of the current inner loop is much higher than that of the voltage outer loop, a reasonable simplification is made as follows: Let inductor current track the current command while designing the voltage outer loop. Take the current inner loop as a constant gain 1, then the open loop transfer function of the voltage outer loop is:

$$G_V(z)=\frac{T_s}{C}\cdot\frac{K_1z-K_2}{z-1}\cdot\frac{1}{z-1} \tag{5}$$

The capacitor ESR r_C is omitted. The characteristic equation of the closed voltage loop is:

$$\frac{T_s}{C}\cdot\frac{K_1z-K_2}{z-1}\cdot\frac{1}{z-1}+1=0 \tag{6}$$

Also, we place the root of the closed-loop system at zero to achieve deadbeat effect:

$$K_2=\frac{C}{T_s} \tag{7}$$

In the simplified block diagrams, a unit feedback is employed for the control parameters design. The actual feedback path will be a proportion loop. Therefore, it is necessary to transform the illustrated block diagram to an actual one to get the parameters finally.

SIMULATION AND EXPERIMENTAL RESULTS

Some related parameters of the proposed

PWM inverter are given in Table 1:

Table 1 Parameters of the UPS inverter system

Item	Symbol	Nominal value(Unit)
Sampling rate	f_s	20 (kHz)
Filter inductor	L_f	0.93 (mH)
Filter capacitor	C_f	20 (μF)
Nominal load	R	16.2 (Ω)
Rail voltage	U_d	400 (V)
Output voltage	v_o	220 (V)
Switch frequency	f_c	20 (kHz)

Fig. 6 shows the presented inverter system frequency response. From the bode diagram, it can be seen that the phase margin is large enough whether on full load or no load conditions, so the control system is stable. And also, the frequency bandwidth is wide enough to ensure fast dynamic response.

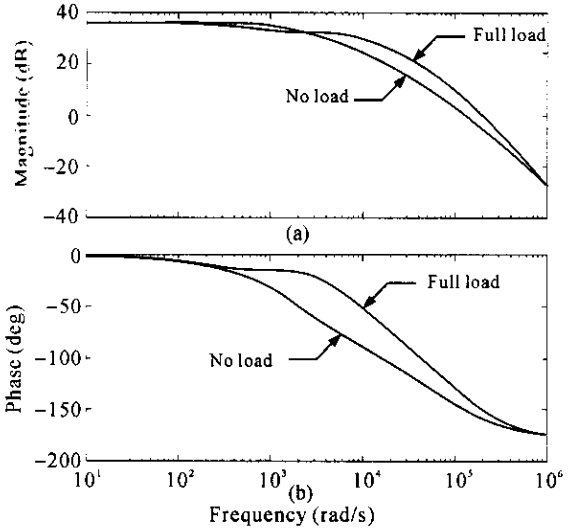


Fig. 6 Frequency response of presented inverter system (a) Magnitude and (b) phase response

In order to verify the control technique and its DSP implementation, a simulation was conducted with a MATLAB/SIMULINK model. Fig. 7 shows the simulation results of output voltage and load current. During the SIMULINK simulation, it was possible to change the load on the fly by using the manual switch (a switch model in SIMULINK library). As can be seen in Fig. 7, the first change is 1.5 KW to 3 KW, the second one is 3 KW to 1.5 KW.

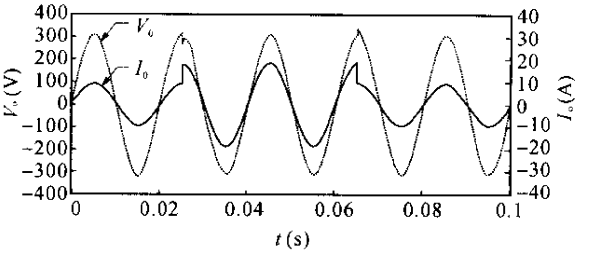
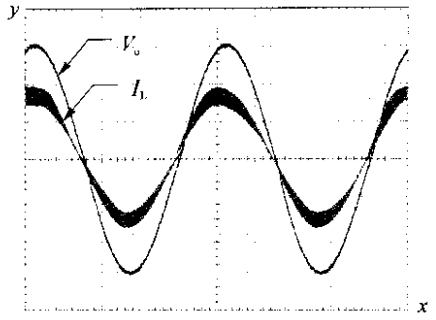


Fig. 7 Simulation results of output voltage and load current under load switch conditions

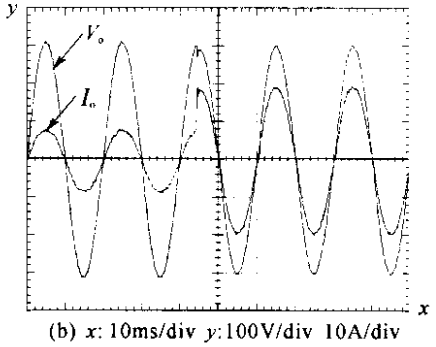
Based on the theoretical designs and MATLAB simulation, a 3 KVA prototype of the PWM inverter was constructed. Fig. 8a exhibits the output voltage and inductor current waveforms under 3 KVA resistive load. The total harmonic distortion (THD) of the output voltage is 1.4%. It shows that the control system has good steady-state characteristics. (THD of the output voltage is measured by LEM HEME ANALYST 2060) Fig. 8b and Fig. 8c illustrate the output voltage and load current under the step change of load from the half load (1.5 KVA) to full load (3 KVA) and full load to half load, respectively. The control system can quickly regulate the output voltage to steady state in 1 ms with rms 220 V at specified frequency 50 Hz. The results of load change demonstrated that the control system has fast dynamic response. (Fig. 8 in the next page).

CONCLUSIONS

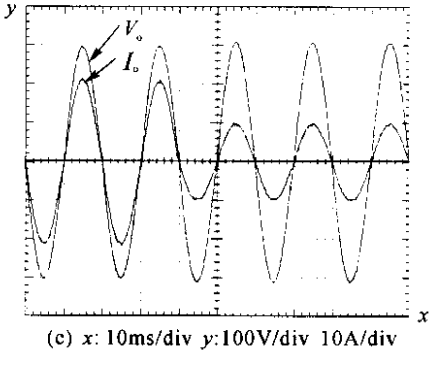
Compared with the analog control techniques, the DSP-based full digital control technique can dramatically simplify the design process of the control circuitry and increase the flexibility of the designs. This paper presents a novel digital dual-loop control scheme, digital deadbeat control technique has been used to enhance the performance of the PWM inverter. Half



(a) x: 4ms/div y:100V/div 10A/div



(b) x: 10ms/div y:100V/div 10A/div



(c) x: 10ms/div y:100V/div 10A/div

Fig.8 Experimental waveforms

(a) Output voltage and inductor current (x: 4ms/div y: 100V/div 10A/div); (b) output voltage and current, half to full load (x: 10ms/div y: 100V/div 10A/div); (c) output voltage and current, full to half load (x: 10ms/div y:100V/div 10A/div)

switching period delayed sampling and control timing strategy is employed to improve the dynamic response of the control systems. Simulation and experimental results verified the performance of the proposed control scheme.

ACKNOWLEDGEMENT

The authors thank Kong, J.H. and Yao, G. for their help in the experiments.

References

Jung, S.L., Huang, H.S., Chang, M.Y. and Tzou, Y.Y., 1997. DSP based multiple-loop control strategy for single-phase inverters used in AC power sources. IEEE PESC 97, St. Louis, Missouri, p.706 – 712.

Jung, S.L. and Tzou, Y.Y., 1996. Discrete sliding-mode control of a PWM inverter for sinusoidal output waveform synthesis with optimal sliding curve. *IEEE Trans. PE*, **11**(4):567 – 577.

Low, K.S., 1999. A DSP-based single-phase AC power source. *IEEE Trans. PE*, **46**(5): 936 – 941.

Texas Instruments, 1997. CPU, System, and Instruction Set. *In*: TMS320C24X DSP Controllers Reference Set.

Tzou, Y.Y., Ou, R.S., Jung, S.L. and Chang, M.Y., 1997. High-Performance programmable AC power source with low harmonic distortion using DSP-based repetitive control technique. *IEEE Trans. PE*, **12**(4): 715 – 725.

Wu, H.Y., Lin, D., Zhang, D.H., Yao, K.W. and Zhang, J.F., 1999. A current-mode control technique with instantaneous inductor current feedback for UPS inverters. IEEE APEC, Texas, USA, p.951 – 957.

Zhang, K., Kang, Y., Xiong, J., Zhang, H. and Chen, J., 2000. Repetitive waveform correction technique for CVCF-SPWM Inverter. IEEE PESC, Galway, Ireland, p.153 – 158.