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Noise and linearity optimization methods for a 1.9GHz low noise amplifier

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Abstract: Noise and linearity performances are critical characteristics for radio frequency integrated circuits (RFICs), especially for low noise amplifiers (LNAs). In this paper, a detailed analysis of noise and linearity for the cascode architecture, a widely used circuit structure in LNA designs, is presented. The noise and the linearity improvement techniques for cascode structures are also developed and have been proven by computer simulating experiments. Theoretical analysis and simulation results showed that, for cascode structure LNAs, the first metallic oxide semiconductor field effect transistor (MOSFET) dominates the noise performance of the LNA, while the second MOSFET contributes more to the linearity. A conclusion is thus obtained that the first and second MOSFET of the LNA can be designed to optimize the noise performance and the linearity performance separately, without trade-offs. The 1.9GHz Complementary Metal-Oxide-Semiconductor (CMOS) LNA simulation results are also given as an application of the developed theory.

Key words: RFIC, CMOS LNA, NF, noise, IP3, linearity
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INTRODUCTION

Recently, the high frequency performance of CMOS have been improved significantly in the low gigahertz frequency bands, making it a good candidate for the integration of both digital and analog chips. However, performances, such as noise and linearity characteristics, must be analyzed and designed carefully, so as to overcome the drawbacks of CMOS technologies in RFIC applications.

The cascode architecture shown in Fig. 1 is widely used in CMOS LNA circuits. With source degeneration, the input impedance of this structure is given by (Shaeffer *et al.*, 1997) as

$$Z_{\text{in}} = \omega_T L_s + j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} \approx \omega_T L_s \quad (\text{at resonance}) \qquad (1)$$

The noise performances of the first MOSFET M_1 in the cascode architecture (Fig.1) had been extensively studied (Shaeffer *et al.*, 1997; Lee, 1998). Eq.(1) shows that, with the degeneration inductor L_s at the source of M_1, the cascode structure can simultaneously achieve input impedance match and avoid thermal noise generated by a real input resistor at the gate of M_1. Many papers (Park *et al.*, 2001; Tinella *et al.*, 2001; Jin *et al.*, 2001) discussed qualitatively the noise and linearity performance of MOSFET M_2, but few papers focused on the relationships between the noise and linearity of MOSFETs M_1 and M_2, and give the choice of device sizes of M_2. In this work, a quantitative analysis of the cascode architecture was conducted and yielded exact expressions of the noise and linearity performances. It can be seen from these

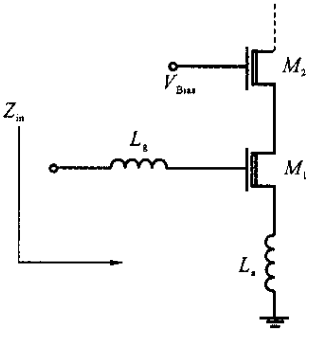

Fig.1 The cascode architecture

expressions that the MOSFET M_1 dominates the noise performance while M_2 contributes mainly to the linearity performance; and these two MOSFETs have little effects on each other. Thus the low noise and high linearity performances can be achieved by the optimization of M_1 and M_2 separately, with almost no trade-offs.

NOISE ANALYSIS

The noise contribution of the second MOSFET M_2 can be considered as a noise current at the output port of the first MOSFET M_1 (Van der Ziel, 1986), as shown in Fig.2. In order to accommodate possibilities of the correlation between the drain noise current i_{nd} and the gate noise current i_{ng}, we describe i_{ng} as a combination of two terms: the i_{nd} dependant term i'_{ng} and the i_{nd} independent term i''_{ng}:

$$\begin{aligned} i_{ng1} &= i'_{ng1} + i''_{ng1} \\ i_{ng2} &= i'_{ng2} + i''_{ng2} \end{aligned} \tag{2}$$

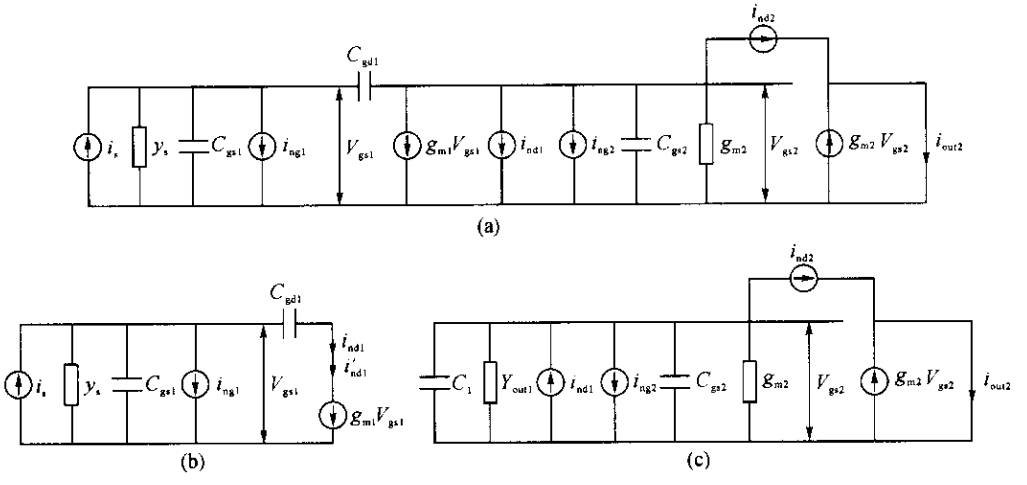

Fig.2 (a)The noise model of the cascode architecture; (b) The equivalent circuit for calculating the noise figure of the circuit; (c) The equivalent circuit for calculating the contribution of the second MOSFET

In Fig.2b, the noise contribution of M_2 is represented by an equivalent current source i'_{nd} at the output of M_1. The inter-stage network can then be short-circuited for the calculation of the noise figure for the whole circuit. Moreover, since the drain noise current and the gate noise current were given by Van der Ziel (1986) as

$$\begin{aligned} \overline{i_{nd}^2} &= 4kT\gamma g_{d0} \\ \overline{i_{ng}^2} &= 4kT\delta g_g \end{aligned} \tag{3}$$

the noise figure of the cascode architecture can be calculated from Fig.2b as follows:

$$NF = 1 + \frac{\delta_1 g_{g1}(1+|c|^2)}{g_s} + \frac{R_{n1}}{g_s}\left| y_s + j\omega C_{gs1} + j\omega C_{gd} - (g_{m1} - j\omega C_{gd1})c\sqrt{\frac{\gamma_1 g_{d01}}{\gamma_2 g_{d02}}}\right|^2 + \frac{R'_{n1}}{g_s}\left| y_s + j\omega C_{gs1} + j\omega C_{gd1}\right|^2 \tag{4}$$

Where y_s is the source admittance, g_s is the source conductance, c is the correlation coefficient for the drain noise current and the gate noise current, R_{n1} is the equivalent noise resistance generated by the drain noise current of M_1, and equals to

$$R_{n1} = \frac{\gamma_1 g_{d01}}{g_{m1}^2} \tag{5}$$

Representing the noise contribution of M2, R'_{n1} in Eq.(4) is the equivalent noise resistance generated by i'_{nd1}. Neglecting the gate noise current, it can be obtained, from Fig.2c, that

$$R'_{n1} = \frac{\gamma_2 g_{d02}}{g_{m1}^2}\left(\frac{\omega_0 C_1}{g_{m2}}\right)^2 \tag{6}$$

where C_1 represents the overall capacitance at M_1 drain, including the parasitic capacitance at M_1 drain and the gate-to-source capacitance of

M_2.

Substituting Eq.(6) and Eq.(5) into Eq.(4) and neglecting the gate noise current and the gate-to-drain capacitance of M_1 yields

$$NF = 1 + \gamma_1 g_{d01} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \left(1 + \left(\frac{\omega_0 C_1}{g_{m2}}\right)^2 \left(\frac{\gamma_2 g_{d02}}{\gamma_1 g_{d01}}\right)\right) \quad (7)$$

Eq.(7) represents the overall noise figure of the cascode architecture with the source degeneration structure of the first MOSFET M_1 neglected. Taking this source degeneration structure into account, the equivalent circuit for calculating the structure noise figure shown in Fig. 2b becomes the circuit shown in Fig.3.

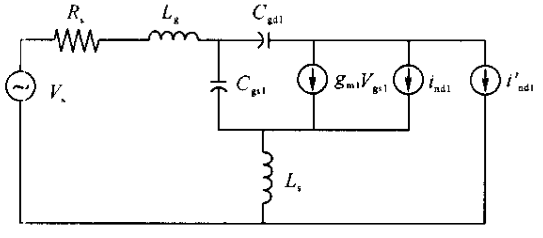

Fig.3 The equivalent circuit for calculating the noise figure of the cascode architecture taking the source degeneration into account

Comparing Fig.2(b) and 3, we find the only difference between them is the position of i_{nd1}, the drain noise current of M_1. Applying the same method as used above and considering the new position of i_{nd1}, the cascode architecture noise figure can be obtained as follows:

$$NF = 1 + \gamma_1 g_{d01} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \cdot \left(1 + \left(\frac{\omega_0 C_1}{g_{m2}}\right)^2 \left(\frac{\gamma_2 g_{d02}}{\gamma_1 g_{d01}}\right)\left(1 + \frac{\omega_T L_s}{R_s}\right)^2\right) \quad (8)$$

The result shown in Eq.(8) is analogous with that shown in (Floyd *et al.*, 1999). From Eq.(8), it can be seen that the noise contribution of the second MOSFET M_2 is

$$NF_{M2} = \gamma_2 g_{d02} R_s \left(\frac{\omega_0 C_1}{g_{m2}}\right)^2 \left(1 + \frac{\omega_T L_s}{R_s}\right)^2 \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (9)$$

Eq.(9) indicates that the noise contribution of M_2 decreases with C_1, the parasitic capacitance at M_1 drain, which, in turn, can be reduced by properly designed layout. In general, C_1 is in the same order of magnitude as that of the gate-to-source capacitor, thus

$$\left(\frac{\omega_0 C_1}{g_{m2}}\right)^2 \approx \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (10)$$

and the noise contribution of M_2 becomes

$$NF_{M2} \approx \gamma_2 g_{d02} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \left(1 + \frac{\omega_T L_s}{R_s}\right)^2 \left(\frac{\omega_0}{\omega_T}\right)^2 \approx NF_{M1} \left(1 + \frac{\omega_T L_s}{R_s}\right)^2 \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (11)$$

where NF_{M1} is the noise contribution of M_1. In practice, usually we have $\omega_0 << \omega_T$, so the noise contribution of M_2 is much less than that of M_1. Therefore the first MOSFET dominates the noise performance of the cascode structure LNA and it must be optimized for noise performance.

LINEARITY ANALYSIS

The cascode architecture shown in Fig. 1 can be considered as two cascaded nonlinear stages shown in Fig.4.

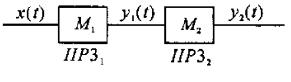

Fig.4 Equivalent cascaded nonlinear stages

Neglecting harmonic terms higher than the third-order and the DC term in the transfer function of these two nonlinear stages, we get the input-output characteristics of M_1 and M_2 in Taylor series

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \quad (12)$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^2(t) + \beta_3 y_1^3(t) \quad (13)$$

where α and β are the Taylor series coefficients. Substituting Eq.(13) into Eq.(12) yields

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_2\beta_1 + \alpha_1^2\beta_2)x^2(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3)x^3(t) \quad (14)$$

According to Lee (1998), the input-referred third-order intercept point ($IIP3$) of the cascode structure can be written as

$$IIP3^2 = \frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3}\right| \quad (15)$$

In Eq.(15), the three terms in the denominator may all be negative or positive. To estimate the worst-case, they are all set to positive. Thus

$$\frac{1}{IIP3^2} = \frac{3}{4}\left|\frac{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3}{\alpha_1\beta_1}\right| = \frac{3}{4}\left|\frac{\alpha_3}{\alpha_1} + \frac{2\alpha_2\beta_2}{\beta_1} + \frac{\alpha_1^2\beta_3}{\beta_1}\right| = \frac{1}{IIP3_1^2} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1^2}{IIP3_2^2} \quad (16)$$

where $IIP3_1$ and $IIP3_2$ are the input-referred third-order intercept points of the first and second stage respectively.

If the gain of the circuit, α_1, is greater then unity, it can be seen from Eq.(16), that the second stage plays a more important role than the first stage in $IIP3$. Therefore, in the cascode architecture, M_2 contributes more to the linearity of the circuit than M_1, and should be designed for linearity optimization.

Below, we will give a detailed analysis of the linearity behavior of M_2.

The transfer function, for a short channel MOSFET, can be expressed as (Van der Ziel, 1986)

$$i_d = \mu_{eff} C_{ox} \frac{W}{2L}(V_{GS} + v(t))^2 \quad (17)$$

where V_{GS}, the threshold voltage V_T subtracted from the gate-to-source DC voltage, is the net DC bias voltage between the gate and the source, $v(t)$ is the input voltage, and μ_{eff} is the effective mobility, which equals to

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} + v(t))} \quad (18)$$

where μ_0 is the low-field mobility, and the normal field mobility degradation factor θ has a typical value in the range of $0.1 - 1V^{-1}$. Substituting Eq.(18) into Eq.(17) and letting

$$K = \mu_0 C_{ox} W/2L,$$

we have

$$i_d = K\frac{(V_{GS} + v(t))^2}{1 + \theta(V_{GS} + v(t))} \quad (19)$$

Expanding Eq.(19) in Taylor series and neglecting the DC component and harmonics higher than the third-order, we get the coefficients of the transfer function expressed in Eq.(13),

$$\beta_1 = \frac{KV_{GS}(2 + \theta V_{GS})}{(1 + \theta V_{GS})^2},$$
$$\beta_2 = \frac{K}{(1 + \theta V_{GS})^3}$$
$$\beta_3 = \frac{-\theta K}{(1 + \theta V_{GS})^4} \quad (20)$$

The input-referred third-order intercept point of M_2 is, therefore, equal to

$$IIP3_2^2 = \frac{4}{3}\left|\frac{\beta_1}{\beta_3}\right| = \frac{4}{3}\left|\frac{V_{GS}(2 + \theta V_{GS})(1 + \theta V_{GS})^2}{\theta}\right| \quad (21)$$

As shown in Eq.(21), the input-referred third-order intercept point of M_2 increases with the DC bias. Increasing the supply voltage will increase the DC bias, but will lead a rise in the power consumption of the chip. Since the second MOSFET contributes more to the linearity than the first one, the DC bias voltage of the second MOSFET can be optimized in term of its gate width with a suitable bias voltage, while keeping the DC bias voltage of the first MOSFET as low as possible so as to reduce the power consumption of the chip.

In the section below, a 1.9GHz LNA simulation is given to validate the theory developed in the above sections.

LNA SIMULATION

In this section, the results of simulation of a 1.9GHz cascode architecture LNA are presented. It was conducted by the Agilent Advanced Design System (ADS) with 0.35μm CMOS process. The first MOSFET was designed to get the optimum noise performance, while the second MOSFET was designed to optimize the linearity. The key point here is to find the best gate width of these two MOSFETs.

As shown in Fig.5a, the minimum noise figure of the cascode architecture occurs when the gate width of the first MOSFET is equal to 250 μm. We can see from Fig.5b that the minimum noise figure changes significantly if the gate width of the second MOSFET is less then 100 μm, but changes little when the gate width is greater than 100 μm. When the gate width of M_2 is smaller than 100μm, its output resistance will

be much larger than that of M_1. Thus the bias voltage of M_2 will be much higher than the bias voltage of M_1, making M_1 unworkable in the saturation region. Since all MOSFETs must work in the saturation region in a practical LNA, this situation will not be discussed hereafter. If the gate width of M_2 is greater than 100 μm, both M_1 and M_2 will work in the saturation region. In this case, the gate width of M_2 has little effect on the minimum noise figure of the cascode architecture shown in Fig.5b, indicating that the noise contributions of M_2 are negligible. This conclusion agrees well with the theoretical analysis discussed in Section Two.

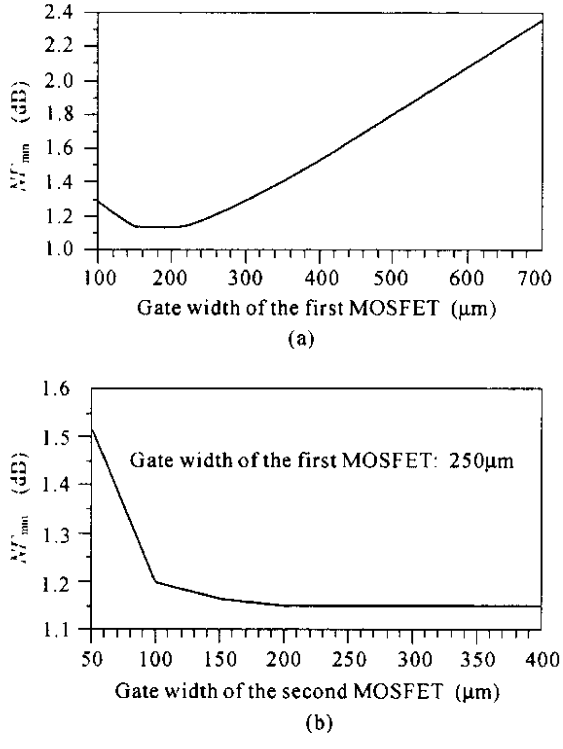

Fig.5 The minimum noise figure vs (a) gate width of M_1 and (b) gate width of M_2

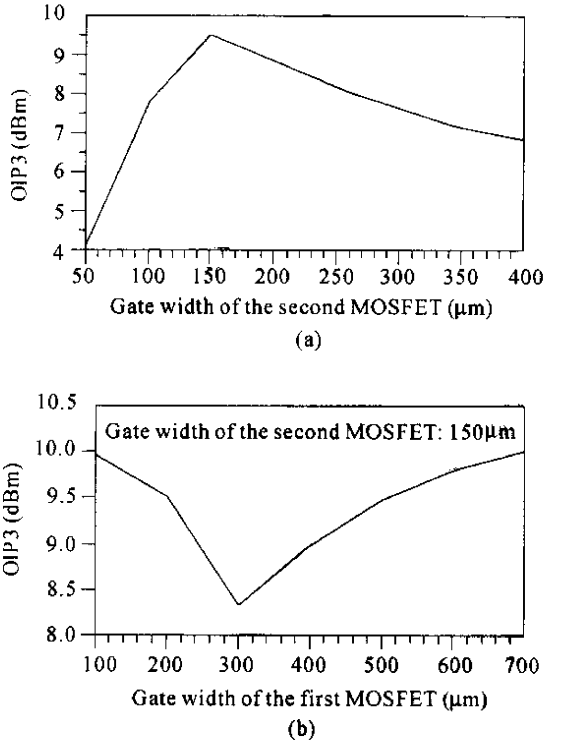

Fig. 6 The output-referred third-order intercept point vs (a) gate width of M_2 and (b) gate width of M_1

Fig.6a shows that the output-referred third-order intercept point (OIP3) peak occurs when the gate width of the second MOSFET is equal to 150 μm. In Fig.6b, the *OIP*3 changes within 8.5 dBm and 10 dBm along with the width of M_1, less than 8% of the central value of OIP3 and is negligible. A conclusion is thus obtained that the gate width of M_1 has little effect on the linearity performance of the cascode architecture, showing a good agreement with the analysis developed in Section Three.

According to the simulation results shown in Fig. 5 and Fig. 6, the optimum gate widths of M_1 and M_2 are chosen to be 250μm and 150 μm respectively. Thereby, the optimum noise and linearity performances of the LNA can be achieved simultaneously without any trade-offs between the device parameters of M_1 and M_2.

Finally, the simulation results of S-parameter and the optimized characteristics of this LNA are given in Fig.7 and Table 1. The noise figure we chose is 1.6 dB, slightly greater than the minimum noise figure NF_{min}, which is 1.13dB. This is because the optimum input impedance required by the minimum noise figure is different from 50 Ω. In order to satisfy the 50 Ω input impedance match, the noise figure has to be increased. It should be pointed out that the 1.6 dB noise figure is still a very low value for CMOS processes.

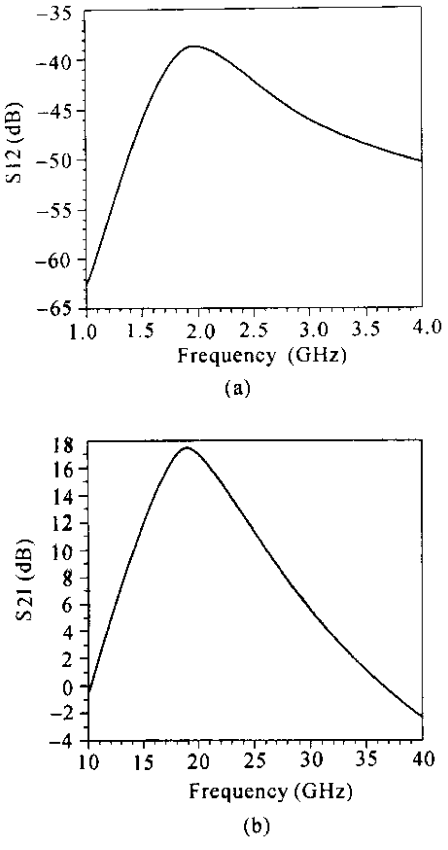

Fig.7 Simulation results of S-parameters
(a) Reverse transmission S12; (b) Forward transinission S21

Table 1 LNA perffformance summary

Parameter	Value
Frequency	1.9 GHz
Noise Figure	1.6 dB
S21	17.5 dB
OIP3	9.5 dBm
Supply Voltage	1.5V
Power dissipation	9 mW
Technology	0.35 μm CMOS

CONCLUSIONS

In this paper, the quantitative expressions of the noise contribution of the first MOSFET and the linearity contribution of the second MOSFET in a cascode structure LNA are presented. As an application of the results, the noise and linearity optimization methods are developed for a 1.9GHz CMOS LNA. According to our expressions, Eq. (8) and Eq. (16), in the cascode architecture, the first MOSFET is the dominant contributor to the noise while the second MOSFET contributes mainly to the linearity. Furthermore, these two MOSFETs have little effects on each other. Therefore, the device parameters of these two MOSFETs can be designed separately, with almost no trade-offs, so that low noise and high linearity performances can be obtained simultaneously. These optimization methods and the analysis results were implemented in a 1.9GHz CMOS LNA design yielding very good circuit characteristics. The simulating experimental results have proved the validity of the theoretical analysis.

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