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DPLL implementation in carrier acquisition and tracking for burst DS-CDMA receivers*

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Abstract: This paper presents the architectures, algorithms, and implementation considerations of the digital phase locked loop (DPLL) used for burst-mode packet DS-CDMA receivers. As we know, carrier offset is a rather challenging problem in CDMA system. According to different applications, different DPLL forms should be adopted to correct different maximum carrier offset in CDMA systems. One classical DPLL and two novel DPLL forms are discussed in the paper. The acquisition range of carrier offset can be widened by using the two novel DPLL forms without any performance degradation such as longer acquisition time or larger variance of the phase error. The maximum acquisition range is $1/(4T)$, where T is the symbol period. The design can be implemented by FPGA directly.

Key words: CDMA, Digital phase locked loop(DPLL), Carrier frequency offset
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INTRODUCTION

DS-CDMA techniques play an important role in current HFC networks and wireless communication systems (Chung *et al.*, 1993; Gaudenzi *et al.*, 1996; Viterbi, 1997). Crucial to the DS-CDMA system is proper code and carrier synchronization. Literature on code synchronization is abundant but on carrier acquisition are rare because carrier recovery after de-spreading process in DS-CDMA receiver seems similar to traditional demodulators. In 3G systems, the existing continues pilot waveform facilitates carrier recovery, but in some burst multi-users DS-CDMA systems such as HFC network and Low Earth Orbiting (LEO) satellite systems, the designer must take special consideration of the following characteristics. First, burst systems have no continues waveform, and the preamble should be as short as possible. Second, as multi-users CDMA receiver, carrier recovery cannot take place prior to signal de-spreading (De Dong *et al.*, 1997). Third, carrier frequency offsets can be large compared to CDMA systems symbol rate due to Doppler shifts or frequency uncertainties in the receiver and transmitter frequency mixing stages. Fourth, although code synchronization usually takes place prior to the carrier recovery process, the large carrier offset will worsen the code synchronization, which means there is strong coupling between the carrier and the symbol synchronization. So although DPLLs have been widely used, there are many problems in the specific application.

Gardner (1996) and Huang *et al.* (1998) analyzed the performance of digital phase-locked loops in different systems including DS-CDMA systems. But they all put emphasis on nonlinear and quantify the influence of the DPLL. The main aim of this work is to try to provide the DPLL design based on FPGA reference according to various degrees of carrier offset in different DS-CDMA systems.

CLASSICAL SECOND-ORDER-DPLL ARCHITECTURE IN DS-CDMA SYSTEM

In DS-CDMA systems, carrier synchronization is performed after the de-spreading process

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as depicted in Fig.1.

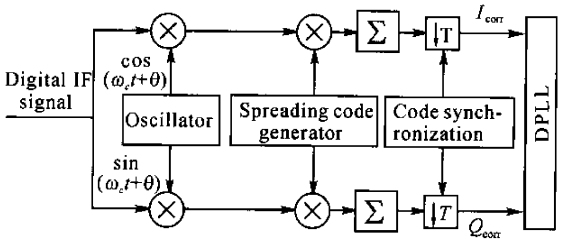

Fig.1 CDMA receiver

The local oscillator (implemented by NCO) in Fig.1 is not controlled by a carrier recovery circuit, but has a frequency close to the received carrier. Thus, removal of the residual carrier offset and data recovery are realized by Digital Phase Locked Loop. The linear DPLL module in Z-domain is depicted in Fig.2.

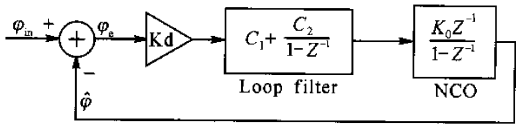

Fig.2 DPLL module

Corresponding to analog PLL, C_1 and C_2 can be described in the following forms:

$$C_1 = 2\xi\omega_n T/K,\ C_2 = (\omega_n T)^2/K \qquad (1)$$

Where ξ is the second-order damping factor, ω_n is the loop natural frequency. We can also introduce another important parameter B_L (loop bandwidths) to describe C_1 and C_2:

$$C_1 = \frac{2\xi}{K}\frac{2B_L T}{\xi+\frac{1}{4\xi}},\quad C_2 = \left(\frac{2B_L T}{\xi+\frac{1}{4\xi}}\right)^2 \Big/ K \qquad (2)$$

and $$B_L = \frac{\omega_n}{8\xi}(1+4\xi^2) \qquad (3)$$

In QPSK-CDMA mode, the acquisition time for a second-order loop can be approximated by the method of Nezami (2001).

$$t_{acq} = \frac{1.2}{B_L T} \qquad (4)$$

It should be pointed out that Eq.(4) is correct only if the carrier frequency offset is less than 1/2 B_L, and that larger offset results in longer acquisition time or phase lock failure.

According to Eq. (7.27) and Eq.(7.30) in Meyr (1989) and Eq. (21) in Nezami (2001), the BER degradation caused by random tracking phase errors is approximated by

$$D = \frac{10}{\ln(10)}\left(\frac{1}{SNR_{in}}+1\right)B_L T \qquad (5)$$

It should also be pointed out that Eq.(5) is correct at high SNR or small B_L value. Usually B_L is set less than 23 percent of the symbol rate so that the BER degradation is approximately less than 1dB.

It is clear there is a tradeoff between Eq.(4) and Eq.(5). Large loop bandwidths results in large capture range and fast acquisition speed but degrade BER performance.

The typical Costas loop used in QPSK systems is depicted in Fig.3:

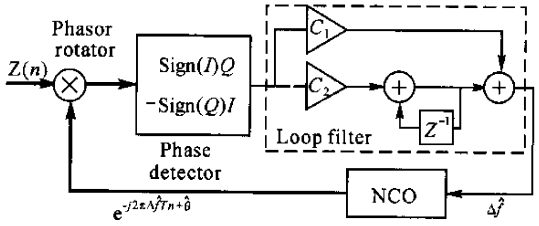

Fig.3 Basic costas loop

The thick black line in Fig.3 represents the complex signal. $Z(n)$ is the de-spreaded signal and sampled by symbol rate. The basic Costas Loop is widely used in HFC network where the carrier frequency offset can usually be controlled in limited range (De Dong *et al.*, 1997).

The trouble with mobile CDMA systems is that the frequency offset is often larger than the symbol rate. To capture the offset in the limited preamble stage, large B_L should be chosen. But on the other hand, the large B_L is not acceptable from the view of BER degradation, or even the loop cannot be locked at all with the large B_L. So the equivalent problem is how to capture the largest possible carrier frequency offset with a given B_L that satisfies the needs of loop stability and phase noise resistance. In the next Section, utilizing the all "1" preamble words, two novel PLL forms are discussed to solve the problem.

One is direct estimation aided, and the other is interpolation-used.

TWO NOVEL DPLLs

Assuming $B_L T = 0.2$, $\xi = 0.7$ is almost an upper limit in view of the noise influence in practice, the DPLL has an approximate capture range of $0.1/T$. In mobile systems, carrier frequency offset is often larger than $1/10T$ due to the Doppler frequency offset and long PN code spreading, especially in LEO systems. Two DPLLs are presented below for enlarging the acquisition range with a given B_L. It should be mentioned that when carrier frequency offset is larger than $1/4T$, the code synchronization would be influenced; and the code acquisition becomes a 2-D time/frequency acquisition problem.

1. Direct estimation aided DPLL

It is suggested that feed-forward carrier offset estimation should be employed when larger offset exists (Gaudenzi *et al*., 1980; 1996). But frequency estimation via spectrum (Meyr, 1989) is too complex to realize based on FPGA. Another frequency estimation (via phase increment estimation) is presented below. Assume the preamble words are set to all "1", $Z(n)$ in Fig.4 is given by

$$Z(n) = \alpha \sqrt{E_c} \sum_{m=1}^{N} \exp(j(2\pi m \Delta f T_c + \theta_n)) + V = I_{corr}(n) + jQ_{corr}(n) \quad (6)$$

Where $\sqrt{E_c}$ is the chip energy, α is the propagation quotiety, N is de-spreading length (spreading gain), T_c is the chip period, θ_n is the initial phase at the nth symbol. V is the noise including MAI (Viterbi 1997), and I_{corr}, Q_{corr} are depicted in Fig.1. Then the frequency estimation below can be obtained

$$\sin(2\pi \Delta \hat{f} T_c) = \frac{I_{corr}(n-1)Q_{corr}(n) - I_{corr}(n)Q_{corr}(n-1)}{I_{corr}(n-1)^2 + Q_{corr}(n-1)^2} \quad (7)$$

The numerator of Eq.(7) can be realized, and the value is proportional to Δf when Δf is far smaller than chip rate. But it is difficult to get the real value of Δf by using FPGA because of the division in Eq.(7). The numerator is not only related to Δf but is also involved in propagation degree and timing synchronization error. But we can judge the sign of Δf by the numerator of Eq.(7). Thus Fig.4 shows a DPLL architecture, which extends the acquisition range to $1/10T$ with the given B_L that is designed to track the carrier frequency offset maximum to $1/20T$.

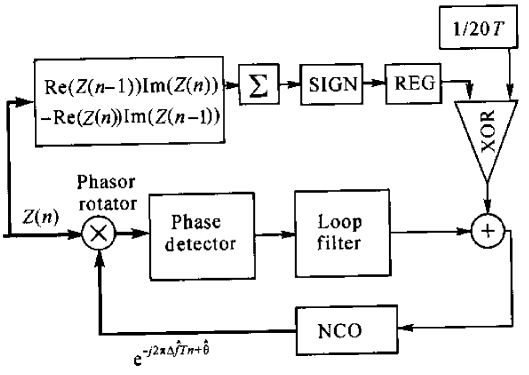

Fig.4 Direct estimation aided DPLL

In Fig.4, the value of $1/20T$ can be accurately known when NCO has been designed. Direct estimation is performed and registered during the preamble stage.

2. Interpolation-used DPLL

Eq.(6) can also be written in another form in the preamble time:

$$Z(n) = \alpha \sqrt{E_c} e^{j\varphi_0} e^{j2\pi\Delta fnT} \frac{1 - q^N}{1 - q} + V \quad (8)$$

Where $q = \exp(j2\pi\Delta f T_c)$

So $Z(n)$ in the preamble time is just a single carrier signal whose frequency is Δf and sampled by symbol rate:

$$Z(n) = B\exp(j2\pi\Delta fnT) + V \quad (9)$$

In mobile CDMA systems, the frequency offset is often larger than the symbol rate but smaller than the chip rate. If we can obtain $Z(m)$ as Eq.(10) ($Z(n)$ sampled by chip rate), we can easily acquire the carrier offset Δf in the preamble time because the phasor of every sample has the carrier offset information. And the CDMA receiver must recover both the symbol clock and chip clock, so that Eq.(10) can be realized.

$$Z(m) = B\exp(j2\pi\Delta fmT_c) + V \quad (10)$$

The direct way to obtain $Z(m)$ is to interpolate the signal $Z(n)$ by chip rate in the preamble time. Through an interpolator, symbol rate signal $Z(n)$ turns into chip rate signal $Z(m)$. Then one chip rate DPLL is used to acquire carrier frequency offset by tracking the signal $Z(m)$, and the DPLL only works in the preamble time(the upper block of Fig.5). When the frequency offset is locked by the chip rate DPLL, another classical DPLL continues to work at the symbol rate to track the signal $Z(n)$ and finish data recovery. The architecture is depicted in Fig.5.

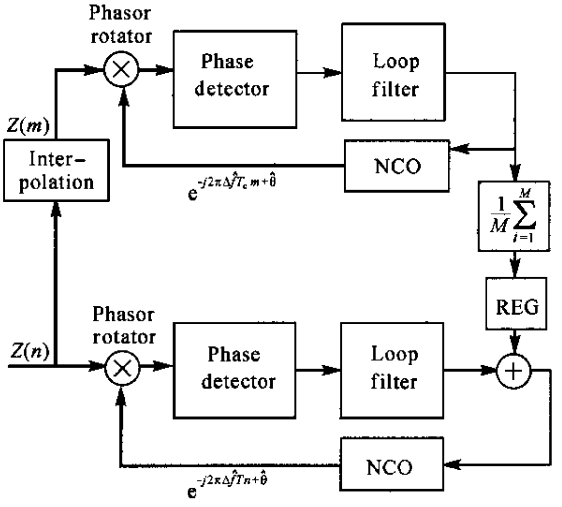

Fig.5 Interpolation used DPLL

Now the problem is how to implement the interpolator. A three-order CIC (Cascaded Integrator Comb) filter is chosen because of its simpler digital implementation and better performance. Fig.6 shows the block of interpolation in Fig.5.

Fig.6 only recovers the real part of $Z(n)$, another uniform interpolator is also employed to recover the imaginary part of $Z(n)$. The Comb block runs at symbol rate, while the Integrator runs at chip rate.

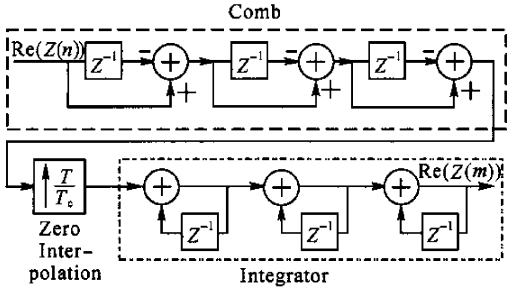

Fig.6 Interpolator using CIC filter

The advantage of the Interpolation-used DPLL is obvious. After interpolation, the carrier offset Δf is small compared to the update rate of the upper loop in Fig.5 so that the frequency offset can be easily tracked. And after preamble time, the residue frequency offset also becomes small comparing to the update rate of the other loop in Fig.5 so that the residue frequency offset can be easily tracked. Thus both normalized loop bandwidths of the two loops in Fig.5 can be chosen to be smaller, so the design of the DPLL becomes easier.

SIMULATION RESULTS

1. Basic Costas DPLL

The basic DPLL architecture is depicted in Fig.3. We define the SNR (signal-to-noise ratio) as:

$$SNR = \frac{N^2 E_c}{V} \tag{11}$$

Where $V/2$ is the variance of I_{corr} and Q_{corr}. The phase error variance obtained in (Nezami, 2001) at high SNR is

$$\sigma_\theta^2 = \frac{B_L T}{SNR} \tag{12}$$

Fig.7 shows plots of the tracking phase error variance against SNR for normalized loop bandwidths of $B_L T = 0.26$, 0.15, 0.01 by simulation (real line) and calculation using Eq.(12) (dashed line). The damping factor $\xi = 0.7$ in Fig.7.

From Fig.7, we notice that Eq.(12) only

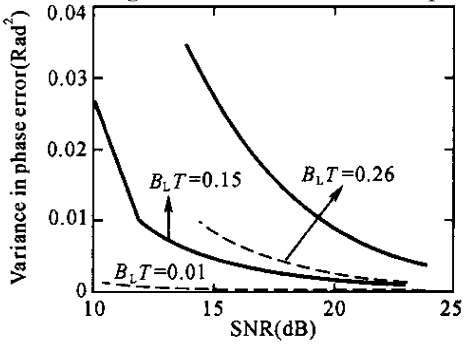

Fig.7 Variance of tracking phase error

matches simulation results at high SNR or with small normalized loop bandwidths. When $B_L T = 0.26$, the loop cannot even be locked when SNR is less than 12dB. So we chose $B_L T = 0.1$ for the flowing simulation.

Fig.8 to Fig.10 show the carrier acquisition and tracking process in typical Costas loop depicted in Fig.3 where the Y-coordinate is the input of NCO ($\Delta\hat{f}$).

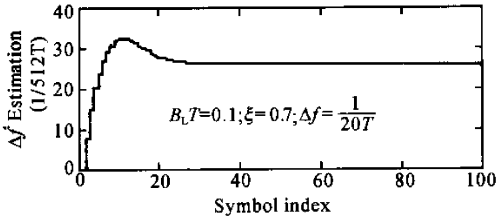

Fig.8 Carrier offset acquisition process with $\Delta f = \frac{1}{20T}$

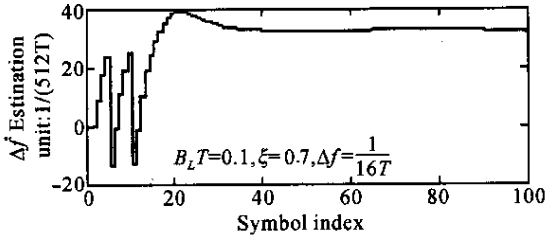

Fig.9 Carrier offset acquisition process with $\Delta f = \frac{1}{16T}$

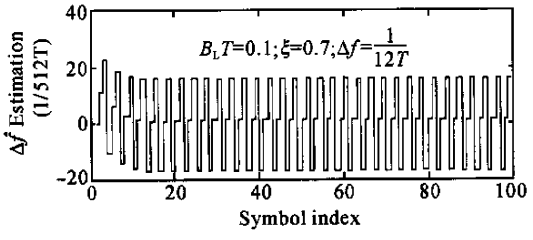

Fig.10 Carrier offset acquisition process with $\Delta f = \frac{1}{12T}$

In Fig.8, when $\Delta f = \frac{1}{20T}$, the frequency acquisition process is perfect. When $\Delta f = \frac{1}{20T}$, although the loop can also be locked as shown in Fig.9, the acquisition time extends to more than 20 symbols. And in Fig.10 the carrier offset acquisition process fails when $\Delta f = \frac{1}{12T}$.

2. Direct estimation aided DPLL

Using the form of Fig.4, the carrier acquisition process returns to perfect as shown in Fig. 11 with the same frequency offset and loop bandwidths as those in Fig.10.

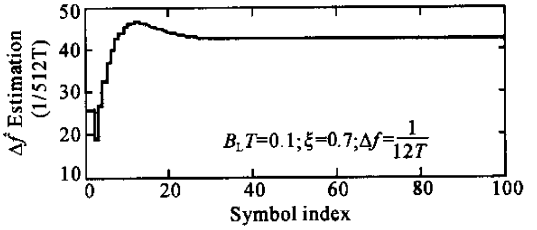

Fig.11 Carrier offset acquisition process with DE-Aided DPLL

Considering the noise influence, Fig. 12 shows the direct estimation, accumulation and registering process in the direct estimation aided DPLL. It shows the accumulator in Fig. 4 can reduce the noise influence.

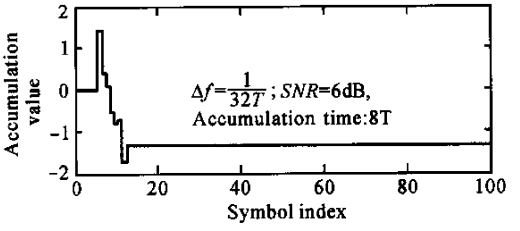

Fig.12 Direct estimation process

3. Interpolation used DPLL

Interpolation used DPLL consists of 2 loops as shown in Fig. 5. The simulation focuses on the frequency acquisition loop (the upper loop in Fig.5). Assuming $N = 64$, $\Delta f = \frac{1}{4T}$, Fig. 13 and Fig.14 show the interpolation process; Fig.15 shows the carrier offset acquisition process after interpolation; the Y-coordinate of Fig. 15 is the

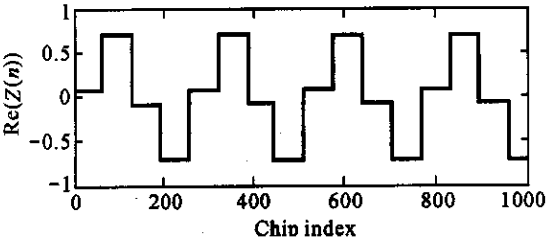

Fig.13 Input of interpolator

input of NCO in the upper loop of Fig. 5. We can observe the cycle libration caused by the simple CIC filter used in the interpolator. The cycle libration and the noise influence can be effectively reduced by the accumulating, averaging and registering process shown in Fig. 16; where the accumulation starts at 200 chips, and ends at 520 chips (totally 4 symbols time), and then the frequency estimation value is obtained by averaging and registering.

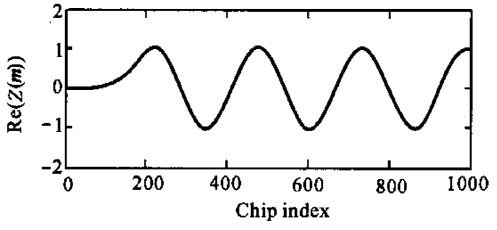

Fig. 14 Output of interpolator

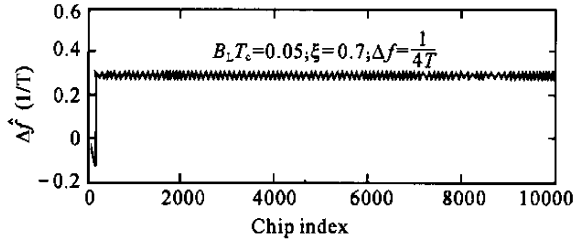

Fig. 15 Carrier offset acquisition process

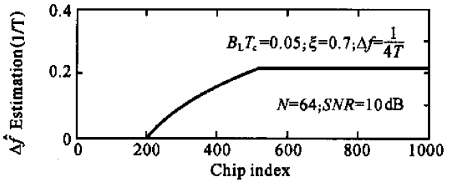

Fig. 16 Accumulating, averaging and registering process

Since the loop is running at chip rate, the frequency offset is much smaller than the update rate in the frequency acquisition loop; the loop parameter $B_L T_c$ can be changed to 0.05. T_c is the chip period.

CONCLUSIONS

In this paper, three DPLL forms are presented to realize carrier frequency offset acquisition in CDMA receiver of burst mode. Specific applications are recommended below:

1. When $\Delta f < \frac{1}{20T}$, the typical Costas loop can be adopted;

2. When $\frac{1}{20T} < \Delta f < \frac{1}{10T}$, the Direct Estimation DPLL is recommended;

3. When $\frac{1}{10T} < \Delta f < \frac{1}{4T}$, the Interpolation-used DPLL can be adopted.

4. When $\frac{1}{4T} < \Delta f$, frequency-sweeping module must be added to acquire the initial carrier offset, but DPLL can still be employed to do fine frequency tracking. The Interpolation used DPLL is also recommended to reduce the initial acquisition time.

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