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Clock generator and OOK modulator for RFID application*

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Abstract: The clock generator and OOK modulator for RFID (Radio Frequency Identification) presented in this paper consist of a current source and delay elements. The simple constant-gm structure is adopted in the current source design and the current consumption of the current source is only about 2 μA. The delay elements, the clock generator and OOK modulator are introduced in detail in the paper. The designed circuits are fabricated by 0.6 μm CMOS process. The area of the core circuit is only about 400 μm×80 μm. The delay time of all three samples is in the range of 9 μs to 21 μs when the supply voltage varies from 2 V to 4 V. As the measured results satisfy the system requirements, these circuit structures are suitable for RFID application.

Key words: RFID, OOK, CMOS, Current source, Delay elements
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INTRODUCTION

In the past few years, the RFID technique has become more and more popular (Kaiser and Steinhagen, 1995; Karthaus and Fischer, 2003; Usami, 2004). An RFID system is contactless, very efficient, can be used in many hostile environments, and has been used in many applications such as tracing animals, automated vehicle identification, carrier transport, and so on. The RFID tags can be divided into active RFID and passive RFID. The passive RFID tags have advantages in term of low cost, small size, long operation lifetime, etc.

Many techniques are used in RFID design. The ultra-small RFID chip (0.3 mm×0.3 mm×0.06 mm) is designed through the embedded antenna technique and special semiconductor technology (Usami, 2004). Reasonable circuit design technique for making RFID chip with very low required receive power is reported in (Karthaus and Fischer, 2003). Liu *et al*.(2003) presented a provided with OOK modulator passive RFID tag for automatic toll-gate at the entrance of a freeway. With the simple OOK modulation otherwise called PSK in (Karthaus and Fischer, 2003), FSK in (Kaiser and Steinhagen, 1995), the more simple circuit can be adopted to reduce the area and power consumption of the chip. The system structure in Liu *et al*.(2003) is shown in Fig.1. The clock generator and OOK modulator are required to generate two clock signals (clk1 and clk2) applied for digital part's clocks and the modulation signal to change the load of the tag's antenna.

The clock generator and OOK modulator are realized by delay circuit consisting of a current source and several delay elements. The designed delay circuits are fabricated by a 0.6 μm CMOS technology. The measured results satisfy the system requirements when the supply voltage varies from 2 V to 4 V. To the authors' knowledge, application of delay circuit in RFID design has never been reported in published literature.

This paper is organized as follows: Section 2

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introduces the circuit structure of the current source, the delay elements, the clock generator and the OOK modulator. In Section 3, some results are presented. Section 4 presents the conclusion.

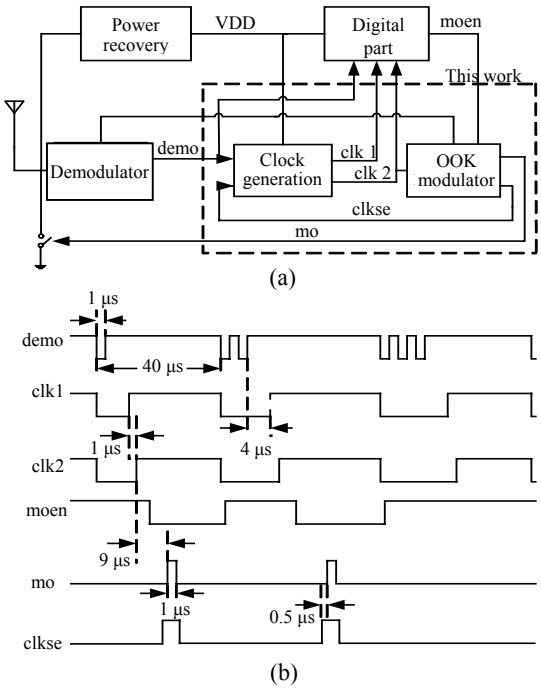

Fig.1 RFID tag structure (a) and several signal's wave (b)

CIRCUIT STRUCTURE

The structure of the tag is shown in Fig.1. The OOK's modulated signal is demodulated at a data rate of 25 kb/s by the demodulator. Then the clock generator provides the clock signals, 'clk1' and 'clk2' for the digital circuit. If the digital part controls the signal 'moen' to be low, the OOK modulator outputs a 1 μs modulated signal which changes the load of the antenna through the switch. At the same time, a signal 'clkse' is generated to prevent the clock generator from generating a false clock signal after the antenna is modulated. The timing relation of these signals is depicted in Fig.1b.

The clock generator and OOK modulator are operated using a current source and delay elements as described below.

Current source

The schematic of the current source is shown in Fig.2. A simple constant-gm structure is adopted to reduce power consumption. The PMOS transistors M1 and M2, the NMOS transistors M3 and M4, the resistor R1 constitute the core of the current source. M5, M6, M7 and M8 make up the current mirror, with the transistors in the latter circuit. M9 starts up the current source to the normal working situation by the signal RST coming from the reset generator circuit (Liu *et al*., 2003).

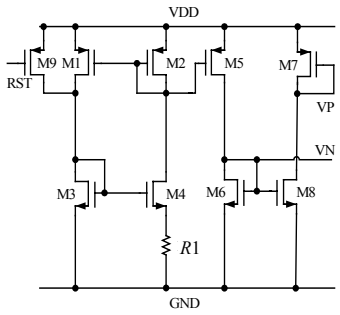

Fig.2 Schematic of the current source

M3 and M4 operate in the weak inversion region. According to Vittoz and Fellrath (1977), the drain current in M3 and M4 can be expressed as:

$$I_{\mathrm{D}} = U_T \ln\left(\frac{S_1}{S_2}\cdot\frac{S_4}{S_3}\right)\Big/R1, \tag{1}$$

where S is the ratio of the effective width to the effective length of the transistor, I_{D} is the drain current of the transistor and U_T is expressed by Eq.(2)

$$U_T=kT/q, \tag{2}$$

where k is Boltzmann's constant, T is the absolute temperature and q is electron charge.

The dimensions of M1 and M2 are identical, so Eq.(1) can be expressed as:

$$I_D=U_T\ln(S_4/S_3)/R1. \tag{3}$$

The drain current is independent of the variation of the supply voltage, and is proportional to the absolute temperature. $R1$ is an N-well resistor whose temperature coefficient has a little compensating effect.

To reduce power, the drain current of M4 is controlled to about 400 nA. $R1$ is 80 kΩ. The total current drained from the current source is only about 2 μA.

Delay elements

Fig.3 shows the schematics of the delay elements. The terminals VN and VP are connected to the corresponding terminals of the circuit in Fig.2. Thus the currents in the transistors M1 and M2 are constant. All the capacitors used poly capacitors.

At the start of the rising edge, node *A* discharges charges via capacitors *C*1, *C*2 and a constant current provided by M1 in Fig.3a. When the voltage of node *A* reaches the threshold voltage of the subsequent inverter, the delay process is finished. The delay time can be roughly calculated by Eq.(4):

$$t=(C1+C2)U_{TH}/I_D, \quad (4)$$

where U_{TH} is the threshold voltage of the inverter and I_D is the drain current in the transistor M1 or M2.

Fig.3b is the delay element for the falling edge of the signal. Its working principle is the same as that described for Fig.3a. The only difference is that it affects the falling edge of the incoming signal.

Clock generator and OOK modulator

The block diagram of the clock generator and OOK modulator are shown in Fig.4. Through the simple logic circuits, the signal 'clk1' is obtained from the signal 'demo' which is delayed by about 4 μs. Another clock signal 'clk2' that is delayed 1 μs from 'clk1' may be obtained by the same circuit with some

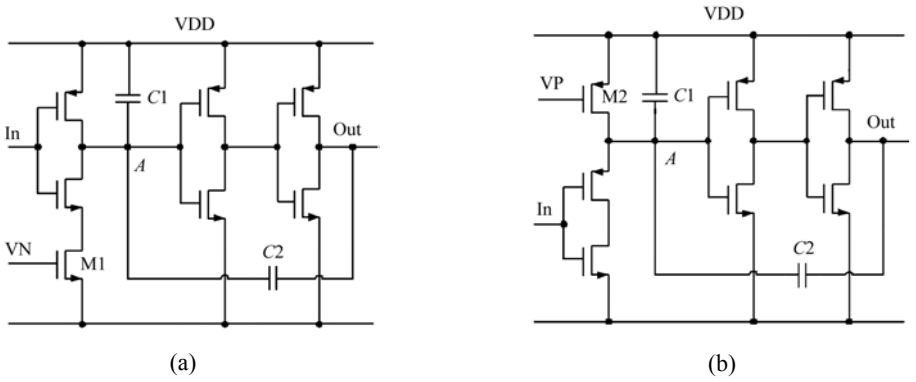

Fig.3 Schematics of the delay elements for the rising edge (a) and for the falling edge (b)

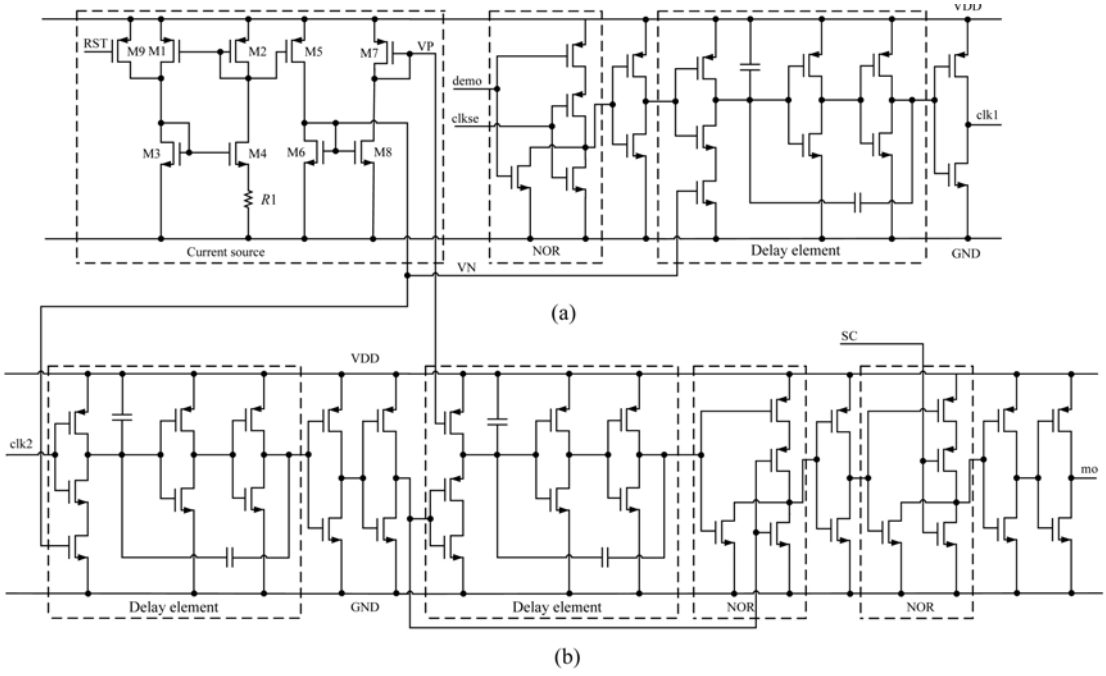

Fig.4 The schematic of clock generator (a) and OOK modulator (b)

different component parameters. The signal 'clkse' controls the on and off operation of the clock generator.

The OOK modulator is composed of two delay elements. The first delay element completes the delaying function of 'clk2' by about 9 μs. The second delay element and the NOR gate generate a modulation signal with a pulse width of 1 μs. The terminal SC controls whether outputting the modulation signal. Generating the signal 'clkse' is not described as it is similar to generating the signal 'mo'.

These two circuits provide the two clock signals for the digital circuit generating the modulation signal. As shown in Fig.1b, the typical delay of the 'mo' signal with respect to the signal 'clk1' is about 14 μs. The system requirements are satisfied if this delay time falls in the range of 9 μs to 21 μs.

EXPERIMENTAL RESULTS

The clock generator and OOK modulator described above are fabricated by a 0.6 μm CMOS process. Fig.5 shows the die microphotograph of these two circuits.

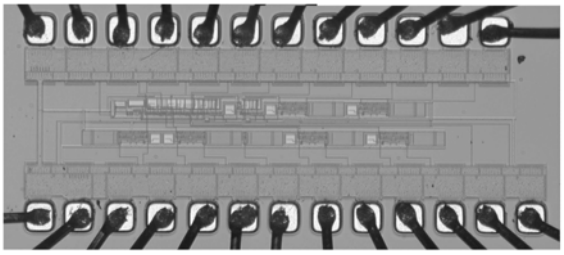

Fig.5 The die microphotograph

The area of the core circuit is only about 400 μm×80 μm.

Three samples for the same circuit were tested. The total delay time and the simulation results of these three samples are summarized in Fig.6.

Fig.6 shows that when the supply voltage varies from 2 V to 4 V, all three samples satisfy the requirement (The delay time is in the range of 9 μs to 21 μs). More accurate current source may be used to achieve more accurate delay time.

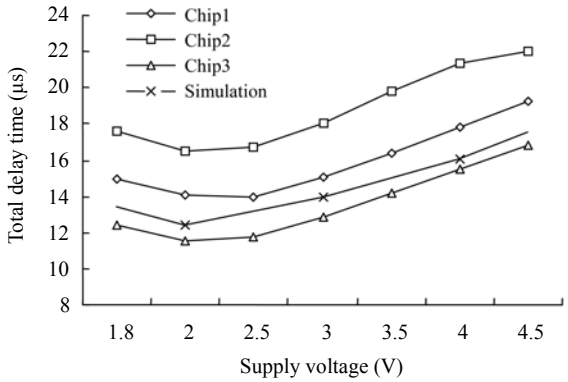

Fig.6 The measured total delay time

CONCLUSION

The clock generator and OOK modulator for RFID application are presented in this paper. These two circuits are composed of a current source and delay elements described in the paper. The designed delay circuit was fabricated by 0.6 μm CMOS technology. The experimental results showed that the delay time satisfies the system requirement and thus these circuit structures are suitable for RFID application. If more accurate delay time is required, more accurate current source should be used.

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