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A 6-switch single-phase 5-level current-source inverter*

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Abstract: The new 6-switch single-phase 5-level current-source inverter proposed in this paper was developed by properly simplifying the traditional 8-switch single-phase 5-level current-source inverter, and its operational principle was analyzed. Just like the problem of voltage-unbalance between different levels existing in voltage-source multilevel inverters, a similar problem of current-unbalance between different levels whether for the 8-switch single-phase 5-level current-source inverter, or for the new 6-switch 5-level current-source inverter also exists. A simple current-balance control method via DC current feedback is presented here to implement the current-balance control between different levels. And to reduce the output current harmonics, PWM control technique was used. Simulation and experimental results showed that this new 6-switch topology operates correctly and that the balance-inductor can almost equally distribute the total DC current.

Key words: Single-phase, Current-source inverter (CSI), Multilevel, Topology
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INTRODUCTION

Up to now, multilevel voltage-source inverters (VSIs) (Fang, 2001) have been paid more attention than multilevel current-source inverters (CSIs) in the high-power fields. One of the most important reasons is that inductors, as energy storage elements, have the disadvantages of higher conducting losses and lower energy storage efficiency than capacitors. However, with the development of superconducting magnetic energy storage (SMES) technology (Luongo, 1996), superconducting inductors can be used as higher efficiency energy storage elements. Compared with VSI, CSI has many advantages, such as more stable working conditions, more direct control of output current, faster dynamic response, etc. So use of superconducting inductors as the current sources of multilevel CSIs in high-power systems is a good choice, so that researches on multilevel CSIs technology will become more and more attractive.

As for single-phase 5-level CSIs, mainly two kinds of topologies have been proposed. The 8-switch 5-level CSI topology and its generic *n*-level CSI structure were presented in (Antunes *et al*., 1999). Low-frequency modulation was used, and current balance was achieved by choosing proper switching combinations without closed-loop control. In (Xiong *et al*., 2004), another kind of 8-switch 5-level CSI topology was analyzed, and PWM strategy was used, but the problem of DC current balance was not considered.

½-level current balance is important for 5-level CSI, without current feedback control, the DC current of the balancing-inductor is hardly kept at ½-level when the load impedance is changed much. In this paper, based on the topology proposed in (Antunes *et al*., 1999), a simpler 5-level CSI topology is proposed and the problem of ½-level current balance is also analyzed and discussed.

NEW SINGLE-PHASE 5-LEVEL CSI

As shown in Fig.1, the traditional 5-level CSI (Antunes *et al*., 1999) is made up of 8 switches,

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namely 4 pairs of parallel complementary switches (S_5S_6, S_7S_8, S_1S_2 and S_3S_4), and two balancing-inductors. To generate the 5-level output current of this 8-switch topology, one possible switching combination can be obtained as shown in Table 1.

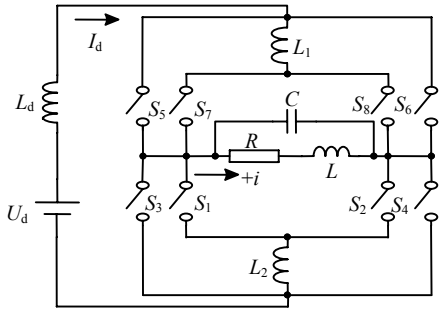


Fig.1 Traditional single-phase 5-level CSI

Table 1 One possible switching combination of single-phase 5-level CSI

Switching combinations	Output current
(S_2 S_4) S_6 S_8	0
(S_2 S_4) S_5 S_8	$+½I_d$
(S_2 S_4) S_6 S_7	$+½I_d$
(S_2 S_4) S_5 S_7	$+I_d$
(S_1 S_3) S_5 S_7	0
(S_1 S_3) S_6 S_7	$-½I_d$
(S_1 S_3) S_5 S_8	$-½I_d$
(S_1 S_3) S_6 S_8	$-I_d$

We can easily find that the switching pair S_2S_4 is always on at the positive half cycle, and another pair S_1S_3 is always on at the negative half cycle. One can conclude that the series connection of L_2, S_2 in parallel with S_4 is just equivalent to L_2 shorted by S_4, and thus there is no current flow through the series connection of L_2, S_2, which is not used and can be removed with such control method; it is the same for the series connection of L_2, S_1. After such simplification, a new single-phase 5-level CSI topology is achieved as shown in Fig.2, where there are only 6 active switches and one balancing-inductor and another balancing-inductor can be removed.

IMPLEMENTATION OF CONTROL METHOD

Substituting S_4 for S_2S_4, and S_3 for S_1S_3 in Table 1 yields switching combinations for this new 6-switch 5-level CSI. It is evident that there are only two switching combinations for generating +½-level current and –½-level current respectively, so the control strategy is greatly simplified. As an example, the equivalent circuit for generating +½-level current is shown in Fig.3, where Z_L is the load impedance.

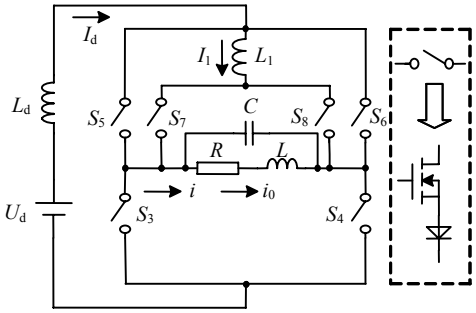


Fig.2 The new single-phase 5-level CSI

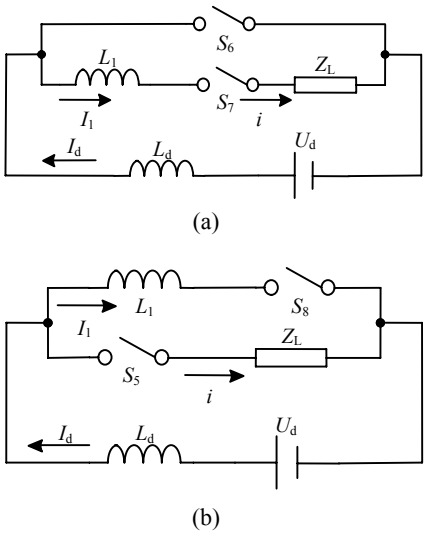


Fig.3 Equivalent circuits. (a) $S_4S_6S_7$ on; (b) $S_4S_5S_8$ on

In Fig.3a, the load impedance Z_L is in series with the balancing-inductor L_1, which makes the steady-state balancing-inductor current I_1 smaller than the one of that in the branch of S_6. While in Fig.3b, L_1 is not in series with Z_L, which makes the steady-state balancing-inductor current I_1 larger than the current in the series connection of S_5, Z_L. Therefore, any of the two combinations alone cannot keep current balance between these two parallel branches. However, if the switching combination in Fig.3a is selected when

$I_1>½I_d$, while for $I_1<½I_d$, the switching combination in Fig.3b is selected. Namely, the switching combination can be changed automatically according to the current in inductor L_1, then the current in balancing-inductor L_1 will be approximately $½I_d$ at the steady state.

In order to automatically change the switching combination, DC current feedback control is introduced. To reduce the load current harmonics, the POD-PWM (McGrath and Holmes, 2002) technique is used. So the POD-PWM technique plus the current closed-loop control constitute the whole control system, whose implementation scheme is shown in Fig.4. The sinusoidal modulating signal W_m and the four triangular carriers are delivered to comparators COMP1~COMP4 respectively, and the PWM signals corresponding to different levels are generated (Xiong *et al*., 2005). The measured DC currents I_1 and I_d are delivered to comparator COMP5, whose output is a pulse signal, if $I_1>½I_d$, output level "1" to select ½-level combinations of $S_4S_6S_7$ and $S_3S_5S_8$, if $I_1<½I_d$, output level "0" to select ½-level combinations of $S_4S_5S_8$ and $S_3S_6S_7$, thus automatically changing of the switching combination can be implemented. This pulse signal together with the PWM signals are sent to LOGIC UNIT to produce gate driving signals for the corresponding active switches S_3~S_8.

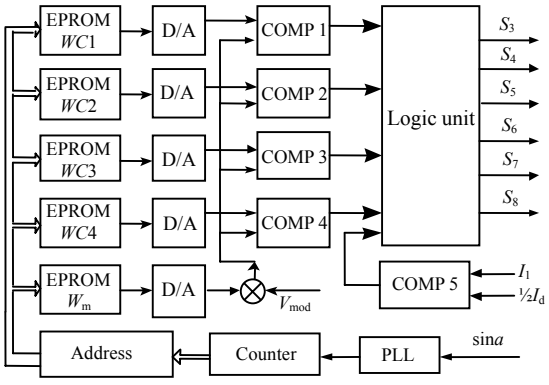


Fig.4 System control diagram

SIMULATION RESULTS

The main simulation parameters are as follows: U_d is the output voltage of 3-phase uncontrolled rectifier and the input phase voltage is 70 V, L_d=200 mH, L_1=100 mH, R=15 Ω, L=10 mH, C=50 μF, the magnitude modulation ratio is 0.9, the frequency modulation ratio is 32, the output frequency is 50 Hz.

Fig.5 shows the simulated waveforms of the balancing-inductor current I_1 and the total DC current I_d, with I_1 clearly almost equal to $½I_d$. Fig.6a shows the load current waveforms: the top is the unfiltered PWM waveforms, and the bottom is the filtered load

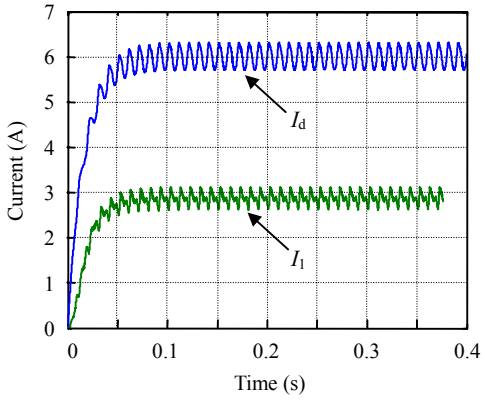
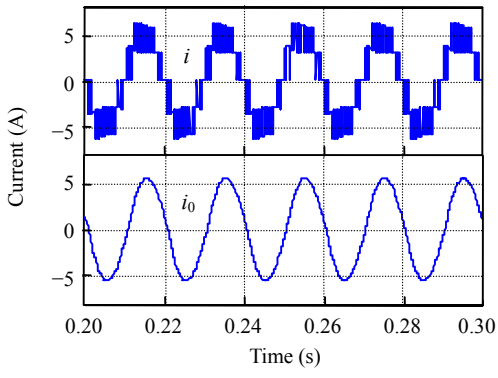
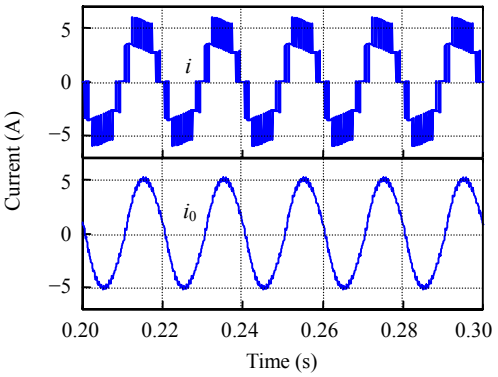


Fig.5 DC current waves (L=10 mH)



(a)



(b)

Fig.6 Output current waves. (a) L=10 mH; (b) L=0 mH

current waveform which is almost sinusoidal and with very low distortion.

However, if a resistive inductive load (L=0 mH) is used, output current waves are as shown in Fig.6b, where the PWM current is almost unchanged, and the load current just becomes a little worse compared with that in Fig.6a. So this inverter is fit for resistive or resistive-inductive loads. But if the resistance R becomes too large, I_d will become too small, the time-constant L_d/R simultaneously decreases and the current ripple of I_d increases much. When the current ripple approximates the value of I_d, the ½-level current cannot keep balance, so that the inverter cannot perform well. Therefore, the DC voltage U_d should also be increased to keep the inverter operate normally, which can be done by using a 3-phase controlled rectifier.

EXPERIMENTAL RESULTS

Based on the operating principle described above, an experimental prototype of a single-phase 5-level CSI was built to demonstrate the validity of the new topology. The schematic of the experimental setup is shown in Fig.2. The circuit parameters are as follows: U_d is the output voltage of 3-phase uncontrolled rectifier and the input phase voltage is 70 V, L_d=200 mH, L_1=100 mH, R=15 Ω, L=10 mH, C=50 μF, magnitude modulation ratio is 0.9, frequency modulation ratio is 32, output frequency is 50 Hz, active switches are composed of MOSFET IRFP450 in series with fast recovery diode HFA25TB60.

Fig.7a shows the total DC current I_d, Fig.7b shows the waveforms of the balancing-inductor current I_1. By comparing I_1 with I_d, one can find that I_1 is very close to ½I_d. Fig.8a shows the unfiltered PWM load current waveforms, Fig.8b shows the filtered load current waveform which is approximately sinusoidal.

CONCLUSION

The traditional 8-switch single-phase 5-level CSI is discussed, a new 6-switch single-phase 5-level CSI is proposed and analyzed. The mechanism for ½-level current balance of balancing-inductor is described. POD-PWM signal generating technique, together with the current-balancing control strategy is developed. An experimental system was built to validate this new topology and its PWM control strategy.

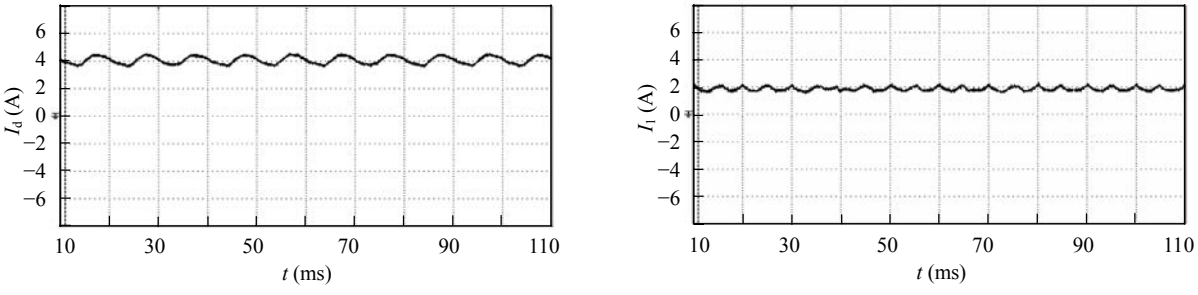


Fig.7 DC current waves. (a) Total DC current; (b) Current in L_1

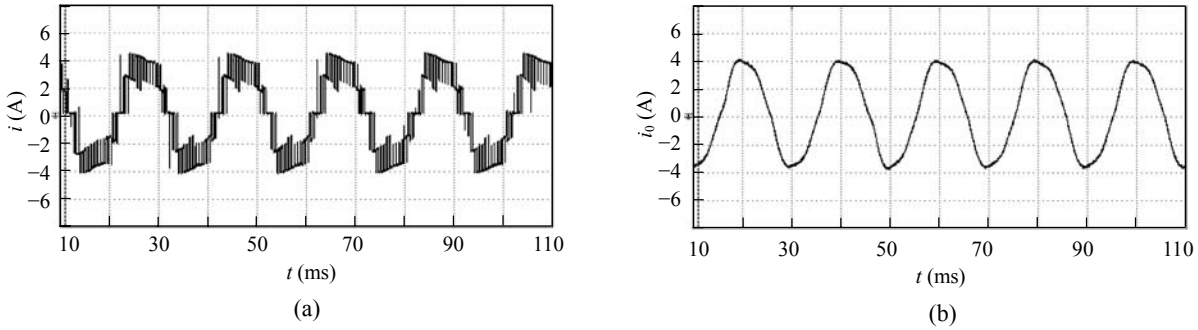


Fig.8 Load current waves. (a) Unfiltered PWM load current; (b) Filtered load current

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