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CdS/SiO_2 nanowire arrays and CdS nanobelt synthesized by thermal evaporation*

YU Ling-min†[1,2], ZHU Chang-chun[2], FAN Xin-hui[1], QI Li-jun[1], YAN Wen[1]
([1]*School of Materials and Chemical Engineering, Xi'an Institute of Technology, Xi'an 710032, China*)
([2]*School of Electronic and Information Engineering, Xi'an Jiaotong University, Xi'an 710049, China*)
†E-mail: ylmyl@163.com

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Abstract: CdS/SiO_2 nanowire arrays and CdS nanobelts were synthesized by thermal evaporation of CdS and CdO mixture powders, with highly selective etching occurring on the silicon substrate surfaces. Study of the growth mechanism of CdS/SiO_2 nanowire arrays and the growth process of CdS nanobelts showed that the growth of CdS dendrites plays an important role in the formation of CdS/SiO_2 nanowire arrays, and that the mechanism of CdS/SiO_2 nanowire arrays growth was in good agreement with "self-assembling nanoelectrochemistry". In the thermal evaporation process, an interaction between Si from silicon substrate and Cd took place.

Key words: CdS/SiO_2 nanowire arrays, CdS nanobelts, CdS dendrites, Self-assembling nanoelectrochemistry
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INTRODUCTION

The richness of fundamental phenomena and the potential applications in nano-technologies has aroused rapidly growing interest in nano-dimensional materials. Quasi-one-dimensional (1D) nano-semiconductors in the form of nanowires and nanoribbons have recently been successfully fabricated in many laboratories and by many methods (Wu *et al*., 2004; Yang *et al*., 2005; Gan *et al*., 2004; Soumitra *et al*., 2006). To synthesize CdS nanowires, people have developed a series of synthetic methods, such as atmosphere pressure chemical vapor deposition (Ge and Li, 2004), solvothermal synthesis CdS nanowires in high yield (Jin *et al*., 2005), sacrificial template growth of CdS nanotubes from $Cd(OH)_2$ nanowires (Li *et al*., 2006), CdS nanowires synthesized in microemulsion system (Fu *et al*., 2004), CdS/Si coaxial CdS/Si coaxial nanowires fabricated via a simple one-step thermal evaporation of CdS powder (Fu *et al*., 2006). The most popular method is using anodic porous alumina template (Wang *et al*., 2005; Xu *et al*., 2000; Yang *et al*., 2002), with the growth mechanism being usually understood as space-limited nucleation followed by growth along the template channels. However, the process of preparing anodic porous alumina template is very complex and controlling the size of pores is difficult. Therefore, the synthesis of aligned nanowires is an important topic worthy of exploration. Recently Tsinghua University Zhu Jing group found that large-area silicon nanowire arrays could be formed on silicon substrates when they are immersed into aqueous HF solution containing silver nitrate (Peng and Zhu, 2003). To explore the possible general use of this method and also the origin of the silicon nanowire arrays formation in HF-based etching solution, one new mechanism—the so called "self-assembling nanoelectrochemistry", which is based on the local passivation of the Si dissolution induced by the growth of metal nuclei—was proposed

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for the formation of Si nanowire arrays. It was suggested that numerous nanometer-sized electrolytic cell arrays could be spontaneously assembled on the surface of silicon substrates in ionic metal HF solution. So that it is believed that highly selective etching could occur on the silicon substrate surface due to the presence of the nanometer-sized electrolytic cell arrays.

In this paper, we demonstrate that CdS/SiO_2 nanowire arrays could also be created on silicon substrate, which is not immersed in HF etching solution. On the surface of Si substrate compact CdS dendrite film and large areas CdS/SiO_2 nanowire arrays are always found.

EXPERIMENTAL PROCESS

Sample preparation

The equipment used for the present work is similar to that described previously. An alumina tube was mounted inside a tube furnace. Three grams CdS (99.999%) and CdO (99%) mixture powders (mass ratio=1:1) were placed near the middle of the high-temperature zone of the furnace. Ten polished silicon substrates about 5 mm wide and 10 mm long were ultrasonically cleaned in acetone, ethanol, deionized water for 20 min each, dipped in 20% HF for 20 min. And then, all the substrates were placed abreast at the alumina tube. The right side of the first Si substrate is apart from the left side of the source material 9.5 cm. The tube had previously been evacuated to a base pressure of 10^{-2} torr by a mechanical pump before the starting materials were heated. The carrier gas of Ar admitted at the other end of the alumina tube flowed at 50 sccm (standard cubic centimeters per minute) at 300 torr after that, The temperature of the furnace was increased to 1150 °C and kept at the temperature for 1 h.

Characterization methods

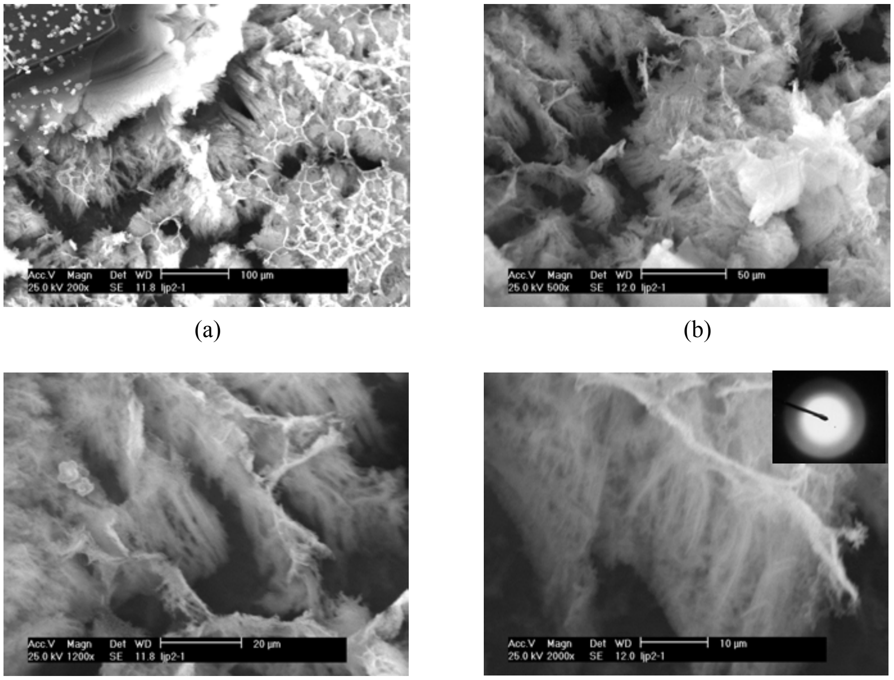
The as-prepared product was first directly examined by scanning electron microscopy (SEM). Micro-structural characterization was carried out in a transmission electron microscopy (TEM) at accelerating voltage of 200 kV. The chemical compositions of the samples were determined by an energy dispersive X-ray (EDX) spectrometer attached to the SEM.

RESULTS AND DISCUSSION

The deposit CdS/SiO_2 nanowire arrays product includes two colors with yellow upside and white underside. The chemical composition of deposition is determined by X-ray energy dispersion (EDX) attached to SEM. The results showed that the white is SiO_2 and the yellow is CdS. SEM showed that continuous CdS dendrites and porous structure are on the silicon substrate (Fig.1a). From Fig.1a it also could be found that there are many yellow particles with the same color as the CdS powders. Dense oriented CdS/SiO_2 arrays could be observed in areas where continuous CdS dendrites are formed. Most of these oriented CdS/SiO_2 nanowire arrays grow normally on the silicon substrate surface and band together in bundles (Fig.1b). Fig.1c shows a high-magnification SEM image of nanowire arrays. Continuous CdS dendrites could be found at the CdS/SiO_2 nanowires end. Fig.1d is a porous structure cross section, showing that uniform diameter SiO_2 nanowire arrays aggregated together are quite clean, with very few particles attached to its surfaces. Further sample characterization was carried out by TEM. The selected-area electron diffraction (SAED) pattern of these CdS/SiO_2 nanowire arrays is given in the inset of Fig.1d, showing that the nanowire arrays' microstructure is amorphous. Fig.2a is a high-magnification of the yellow particle in Fig.1a, showing many CdS nanobelts, some of which are curved to an angle without being broken, which suggests that the nanobelts are very flexible. For a typical nanobelt, the width decreases along the growth direction. Fig.2b shows an SEM image of single nanobelt with width of 2.6~33.3 μm. The SAED pattern of the nanobelts is shown in the inset of Fig.2a showing that the nanowire arrays' microstructure is a single-crystal.

Our experimental results revealed that the HF solution concentration plays an important role in determining the morphology of CdS dendrites and silicon substrate. When the HF solution concentration is less than 10%, pure CdS nanowires could be obtained. The silicon substrate begins to dissolve absolutely when the HF solution concentration is higher than 40%.

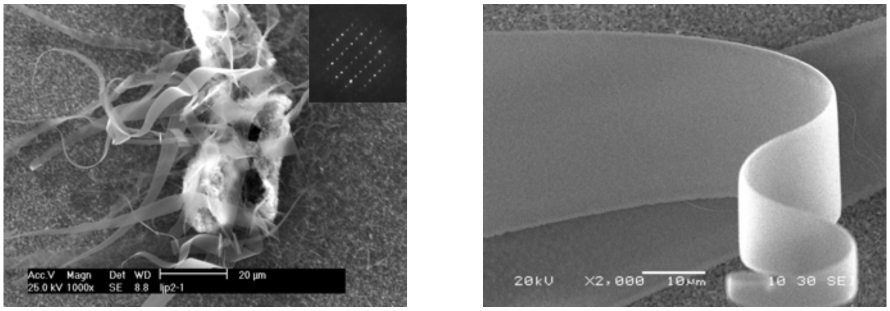
To investigate the source composition on silicon substrate, CdS powders are used instead of CdS and



(a) (b)

(c) (d)

Fig.1 (a) SEM micrograph of CdS dendrites grown on silicon substrates; (b) Porous structure formed under the compact CdS dendrites; (c) Low magnified SEM images of the oriented CdS/SiO_2 nanowire arrays; (d) High magnified SEM images of the oriented CdS/SiO_2 nanowire arrays, the inset is the selected-area electron diffraction pattern



(a) (b)

Fig.2 (a) SEM image of CdS nanobelts, the inset is the selected-area electron diffraction pattern; (b) SEM image of a single CdS nanobelt

CdO mixture powders. The results showed that silicon is also etched. This means that there is interaction between CdS and silicon substrate.

Densely oriented CdS/SiO_2 arrays are always produced during CdS dendrites deposition. In other words, a continuous CdS dendrite greatly hinders the formation of CdS/SiO_2 arrays because CdS dendrites generally cause uniform etching of silicon substrate. In our experiment, it was obvious that CdS dendrites precipitate on the silicon substrate during evaporation of CdS and CdS powder. Silicon substrates are not treated with metallic ion contained in HF solution, but are dipped in 20% HF for 20 min for cleaning. Consequently, there is a small quantity of HF remaining on the silicon substrate surface. When CdS and CdO mixture powders are during the course of thermal evaporation, decomposition and ionization would take place:

$$CdS\ (g) \rightarrow Cd^{2+}\ (g) + S^{2-}\ (g), \quad (1)$$
$$CdS\ (s) \rightarrow Cd\ (g) + S\ (g), \quad (2)$$
$$CdO\ (g) \rightarrow Cd^{2+}\ (g) + O^{2-}\ (g), \quad (3)$$
$$CdO\ (g) \rightarrow Cd\ (g) + \tfrac{1}{2}O_2\ (g). \quad (4)$$

Therefore, both HF and Cd^{2+} are on the silicon substrate surface.

In order to interpret the above phenomena, one needs to look carefully into the etching process of a silicon wafer. It is well known that metal deposition on silicon is initiated by electrochemical reduction of metal ions, a process driven by the difference between the electron quasi Fermi energy in the silicon and the redox energy level of Cd^{2+}. The mechanism for Cd^{2+} reduction is elucidated by aligning the silicon bands with the redox levels of Cd^{2+}, which requires nucleation of nanometer-sized Cd precipitates on the silicon substrate. At the first stage of deposition, deposition begins through the formation of randomly distributed Cd nuclei on the silicon substrate surface, showing exclusion areas around preferential nucleation at kink sites. At long deposition times, these metal nuclei have a strong tendency to coalesce and form continuous compact metal films. With the assistance of HF, nanometer-sized Cd nuclei are distributed on the silicon substrate surface in the early stage and possibly form Cd nuclei arrays. According to the mechanism of “self-assembling nanoelectrochemistry”, these Cd nuclei and the surrounding areas will spontaneously form free-standing microscopic electrolytic cell arrays on the silicon surface if no coalescence occurs. These free-standing microscopic electrolytic cell arrays will not coalesce if abundant CdS dendrites could be produced. At high temperature, Cd nuclei react with S to form CdS. Finally, these microscopic electrolytic cell arrays will lead to highly selective etching of silicon substrates to form CdS/SiO_2 nanowires.

Our method is based on the physical evaporation of CdS and CdO mixture powders, it was surprising that CdS/SiO_2 nanowire arrays were synthesized, which suggests that CdS reacts with silicon substrate. Using a simple thermal evaporation method, CdS nanobelts and nanowires were synthesized on tungsten substrates by Dong and Jiao (2003). In order to study the effects of substrate composition on CdS nanostructure growth, silicon and porous Si were used instead of tungsten. The results showed that substrates do affect the growth of CdS nanobelts and nanowires. When Si and porous Si were used as the substrates and the other growth conditions were kept the same as before, SiO_2 and CdS/SiO_2 composite nanobelts and nanowires were formed. They believed that it is Si from substrate that affects the formation of CdS nanostructures and results in the formation of SiO_2 and CdS/SiO_2 nanobelts and nanowires. In our experiment, we deduced that it is the formation of CdS dendrites that accelerate the selective etching of silicon substrate, which is caused by the formation of the metal-silicide coming from the interaction between Si from silicon substrate and Cd. There is relatively strong chemical bond present in this metal-silicide, which suggests that Cd is always present in the form of metal-silicide. According to observations of Auger electron kinetic energy, we believe that Cd gets some charge from Si in the process of metal-silide formation, which can be interpreted by electron arrangement structure and electronegativity of Cd and Si. The electronegativity of Cd and Si are 1.69 and 1.90 respectively, which indicates that their ability to gain electron is close. The outer space electron structure of Cd and Si are $4d^{10}5s^2$ and $3s^23p^2$. Electron at 3p of Si could transfer to 5p of Cd when there is interaction between Cd and Si so as to produce steady electron structure. As a result, Si from silicon substrate must be reacted with Cd.

CONCLUSION

(1) CdS/SiO_2 nanowire arrays have been synthesized by thermal evaporation of CdS and CdO mixture powders.

(2) Experimental results indicated that the simultaneous growth of CdS dendrites plays an important role in the formation of CdS/SiO_2 nanowire arrays.

(3) The mechanism for CdS/SiO_2 nanowire arrays growth was in good agreement with “self-assembling nanoelectrochemistry”.

(4) In the thermal evaporation process, interaction between Si from silicon substrate and Cd occurs.

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