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A new three-phase 5-level current-source inverter*

BAO Jian-yu†, BAI Zhi-hong, WANG Qing-song, ZHANG Zhong-chao†
(*School of Electrical Engineering, Zhejiang University, Hangzhou 310027, China*)
†E-mail: jianyu_bao@126.com; zhangzc@public1.zju.edu.cn
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Abstract: The new three-phase 5-level current-source inverter (CSI) proposed in this paper was developed by connecting three separate single-phase 5-level CSIs in series, and its operational principle was analyzed. There are two major problems existing in current-source multilevel inverters, one is the complex PWM control method (2-logic to 3-logic conversion), and the other is the problem of current-unbalance between different levels. A simple current-balance control method via DC current feedback is applied in each single-phase 5-level CSI cell to implement the current-balance control between different levels. And to reduce the output current harmonics, POD PWM control technique was used. Simulation and experimental results showed that this new three-phase 5-level CSI topology operates correctly.

Key words: Three-phase, Current-source inverter (CSI), 5-level, Harmonics, POD PWM
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INTRODUCTION

Multilevel converters can offer substantial benefits for higher power applications compared to two level inverters, including reduced harmonics, and increased power ratings because of reduced switching device voltage and current stresses. However, until recently, multilevel voltage source inverters (Peng, 2001) have been the dominant multilevel topology, despite the fact that current-source inverters (CSIs) have many advantages for higher power applications. These include more stable operating conditions, direct control of the output current, faster dynamic response in some circumstances, easier fault management, etc. One primary reason for the limited interest in CSIs to date is that inductors as storage elements have the disadvantages of higher conduction losses and lower energy storage efficiency compared to DC-link capacitors. However, with the development of superconducting magnetic energy storage (SMES) technologies (Karasik and Dixon, 1999), many of the disadvantages of conventional inductors can now be overcome, and hence their use is becoming a more attractive proposition, particularly for higher power applications. Thus there is an emerging interest in research to explore how multilevel CSIs can be topologically arranged and operated.

So far, only a few three-phase multilevel CSI topologies have been proposed. A new three-phase direct type multilevel CSI topology was presented in (Xiong *et al*., 2004), where low-frequency modulation is used, and current balance is achieved by choosing preset switching combinations without closed-loop control. In (Xiong *et al*., 2005), another kind of three-phase five-level CSI topology was analyzed, and PWM strategy was used, but the issue of controlling the intermediate DC link current was not considered.

This paper begins by presenting two kinds of three-phase 5-level CSI topologies, chooses one of them as the new topology suitable for use with three-phase applications, and analyzes its operational principle. Then the multicarrier PWM technique is implemented in each single-phase CSI cell by shifting the phases of the three modulation signals 120 degree

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apart from each other, and a practicable way to maintain the intermediate DC-link current at 1/2 the level of the total DC-link current is also described. Lastly, experimental prototype results are presented to verify this new topology.

NEW THREE-PHASE 5-LEVEL CSI

Antunes *et al*.(1999) presented a generic *n*-level CSI topology, and analyzed its operation in more detail as an 8-switch 5-level CSI system. On the basis of this 8-switch CSI topology, Bao *et al*.(2006) proposed the 6-switch single-phase 5-level CSI topology shown in Fig.1, which is made up of 6 switches, namely 3 pairs of parallel complementary switches (S_5S_6, S_7S_8 and S_3S_4), and one balancing-inductor. To generate the 5-level output current of this 6-switch topology, the switching combination is shown in Table 1.

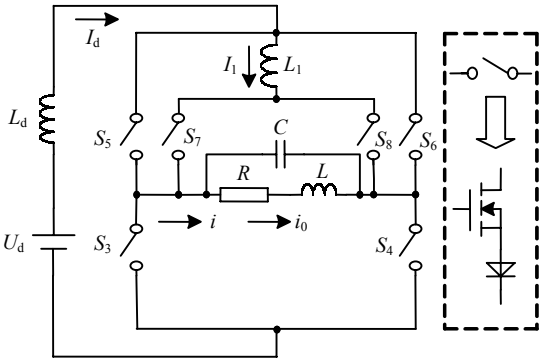

Fig.1 The 6-switch single-phase 5-level CSI

Table 1 Switching combination of the single-phase 5-level CSI

Switching combinations	Output current
$S_4S_6S_8$	0
$S_4S_5S_8$	$+1/2I_d$
$S_4S_6S_7$	$+1/2I_d$
$S_4S_5S_7$	$+I_d$
$S_3S_5S_7$	0
$S_3S_6S_7$	$-1/2I_d$
$S_3S_5S_8$	$-1/2I_d$
$S_3S_6S_8$	$-I_d$

On the basis of this 6-switch single-phase topology, two kinds of three-phase 5-level CSI topologies can be obtained (Fig.2).

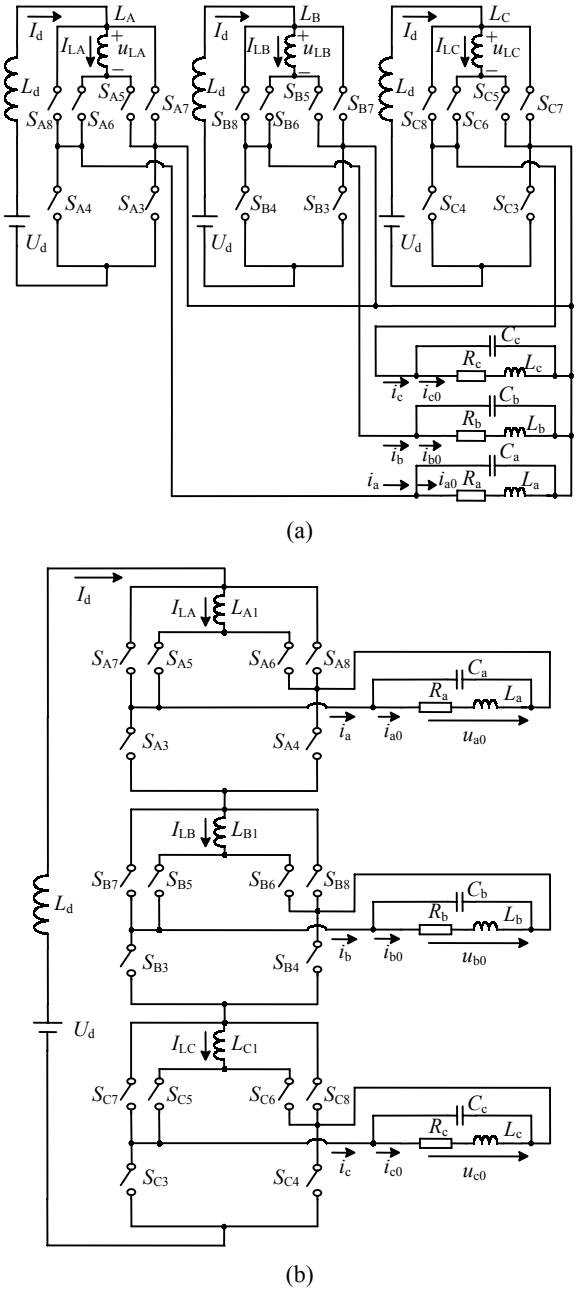

Fig.2 Two kinds of three-phase 5-level CSIs. (a) With the neutral line; (b) Without the neutral line

In Fig.2a, the three-phase 5-level CSI is composed of three single-phase 5-level CSIs, which are decoupled by the neutral line of the loads. Each phase of the inverter can operate independently of the other two phases, but the full load current of each phase must flow through this neutral line. Also, the whole circuit needs three independent DC current-sources, namely three large smoothing-inductors.

In Fig.2b, the three-phase 5-level CSI is also composed of three single-phase 5-level CSIs, which are connected in series with each other. Because the three single-phase CSIs share the same DC current-source, they can operate independently without the need of the neutral line. Comparing to the topology shown in Fig.2a, this topology needs only one DC current-source, namely one large smoothing-inductor. From the viewpoint of circuit structure, the topology in Fig.2b is simpler than that in Fig.2a and can be constructed more easily. Therefore, the topology shown in Fig.2b will be discussed in detail in this paper.

In Fig.2b, the valve switch is composed of such devices as GTO or IGBT in series with a diode. L_x (x=a,b,c) and C_x (x=a,b,c) compose the low-pass filter to filter out switching frequency harmonics on the ac side. R_a, R_b, and R_c represent the ac load. We can extend this topology to higher level structure when we change each CSI cell to the corresponding higher level structure.

PWM CONTROL STRATEGY

The most appropriate strategy to control this CSI is POD-PWM, since it gives the optimum single-phase harmonic cancellation (McGrath and Holmes, 2002) for each single-phase 5-level CSI cell. Fig.3 shows the principle of this scheme for one phase, where the modulation reference signal (W_m) is compared against 4 triangular carriers (WC_1~WC_4).

Each carrier is continuously compared with the modulating signal, and the outputs of these comparisons are used to determine the required switching combination. Table 2 shows how the four comparator outputs define the CSI switching combinations that produce the required output current levels.

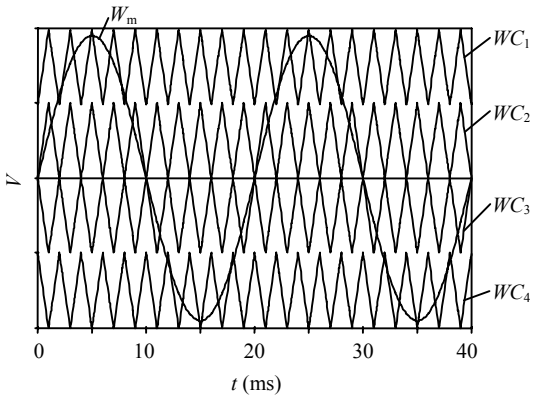

Fig.3 POD-PWM technique

Table 2 CSI switch state decoding for POD-PWM

W_m	Comparator state	Switching combinations	Output current
$W_m>0$	$W_m>WC_1$	$S_4S_5S_7$	$+I_d$
	$WC_2<W_m<WC_1$	$S_4S_5S_8$, $S_4S_6S_7$	$+1/2I_d$
	$W_m<WC_2$	$S_4S_6S_8$	0
$W_m<0$	$\|W_m\|<\|WC_3\|$	$S_3S_5S_7$	0
	$\|WC_3\|<\|W_m\|<\|WC_4\|$	$S_3S_6S_7$, $S_3S_5S_8$	$-1/2I_d$
	$\|W_m\|>\|WC_4\|$	$S_3S_6S_8$	$-I_d$

The comparator outputs are processed using a simple logic coding translation to create the switch gate signals throughout the fundamental cycle. The approach is similar to that used in two-level VSI modulator to decode the outputs to control the switching states of two-level CSI, which allows a CSI modulator to be easily developed from a VSI modulator with the same harmonic performance as the VSI modulator. Hence this proposed scheme will achieve the same harmonic performance as POD-PWM of a five-level VSI system.

IMPLEMENTATION OF CURRENT-BALANCE CONTROL

The principle of balancing-inductor current control proposed in this paper is to detect the polarity relationship between i_{x0} (x=a,b,c) and u_{x0} (x=a,b,c) at each switching period, and to select the appropriate redundant 1/2-level switching state whenever a current of $\pm1/2I_d$ is required in the load, so as to maintain the balancing-inductor current at exactly $1/2I_d$.

If a $+1/2I_d$ output current is required in Fig.1, this is done by arranging the switching decoding logic by the PWM comparator outputs, switching combination $S_4S_6S_7$ will be used if $I_1>1/2I_d$ and the polarities of u_0 and i_0 are the same. Conversely, if the polarities of u_0 and i_0 are different, switching combination $S_4S_5S_8$ will be used. Alternatively, if $I_1<1/2I_d$, switching combination $S_4S_5S_8$ will be used if the polarities of u_0 and i_0 are the same, and switching combination $S_4S_6S_7$ will be used if the polarities of u_0 and i_0 are different. It is

the same for all three single-phase CSI cells. More detailed analysis results are shown in (Bao *et al*., 2006).

Fig.4 shows the system control diagram for one phase cell, which describes how this controller is implemented in practice, with five EPROMs and DACs used to generate the four POD carriers (WC_1~WC_4) and the sinusoidal reference waveform (W_m). The comparator outputs from these signals ($COMP_1$~$COMP_4$) feed into a GAL logic array that is programmed with the logical rules defined above. A fifth comparator ($COMP_5$) determines whether the balancing inductor current is above or below $1/2I_d$, the output is logic "1" if $I_{LX}>1/2I_d$, and the output is logic "0" if $I_{LX}<1/2I_d$. The phase detector logic determines the relative polarity of u_{x0} and i_{x0}, the output is logic "1" if u_{x0} and i_{x0} have the same polarity, while the output is logic "0" if u_{x0} and i_{x0} have different polarity. Therefore, there are altogether four logic combinations: (1,0), (0,1), (1,1), (0,0), which will be fed into the GAL logic array to select the corresponding switching combinations used for the balance control of 1/2-level intermediate DC-link current.

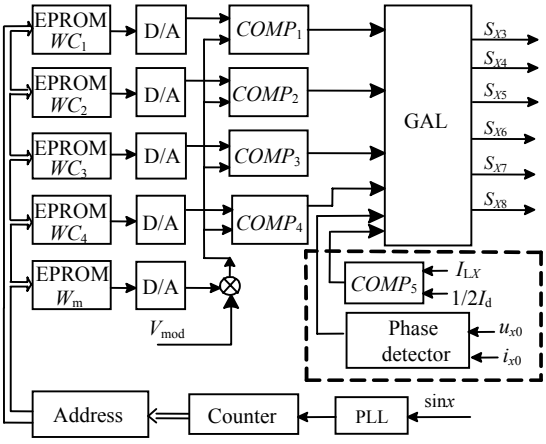

Fig.4 System control diagram for one phase cell

SIMULATION RESULTS

Simulation results based on the new three-phase 5-level CSI are presented to validate the proposition mentioned above. The POD-PWM technique and the intermediate DC-link current-balancing control strategy are applied to each single-phase CSI cell. The simulation parameters of the system are as follows:

The DC supply voltage U_d was provided by a 3-phase uncontrolled rectifier with an input phase voltage of 70 V; the smoothing-inductor L_d=100 mH; the circuit parameters of each cell were L_{x1}=100 mH, R_x=6 Ω, L_x=10 mH, C_x=50 μF; the CSI was operated with a modulation index of 0.9, an output frequency of 50 Hz, and a PWM switching frequency of 1600 Hz (pulse ratio=32).

Fig.5 shows the simulated waveforms of the total DC current I_d, the balancing-inductor current I_{LA}, I_{LB}, I_{LC}, and obviously these three balancing-inductor currents are almost equal to $1/2I_d$. Fig.6a shows the unfiltered load current waveforms, Fig.6b shows the filtered load current waveform which is almost sinusoidal and with very low distortion. Fig.7 shows the harmonic spectrum of one phase output PWM current and its filtered load current. One can see that harmonic contents of the filtered load current are very small.

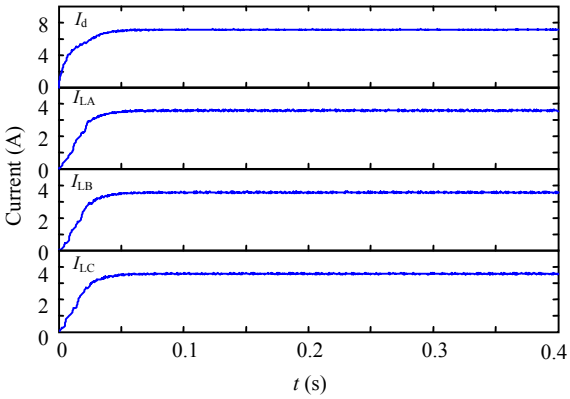

Fig.5 DC current waves

EXPERIMENTAL RESULTS

Based on the operating principle described above, an experimental prototype of a three-phase 5-level CSI was built to demonstrate the validity of this new topology. The schematic of the experimental setup is shown in Fig.2b, the circuit parameters are the same as the simulation parameters listed in "SIMULATION RESULTS", active switches are composed of MOSFET IRFP450 in series with fast recovery diode HFA25TB60.

Fig.8a shows the total DC current I_d, Fig.8b shows the waveforms of the balancing-inductor current I_{LA}. By comparing I_{LA} with I_d, one can find that

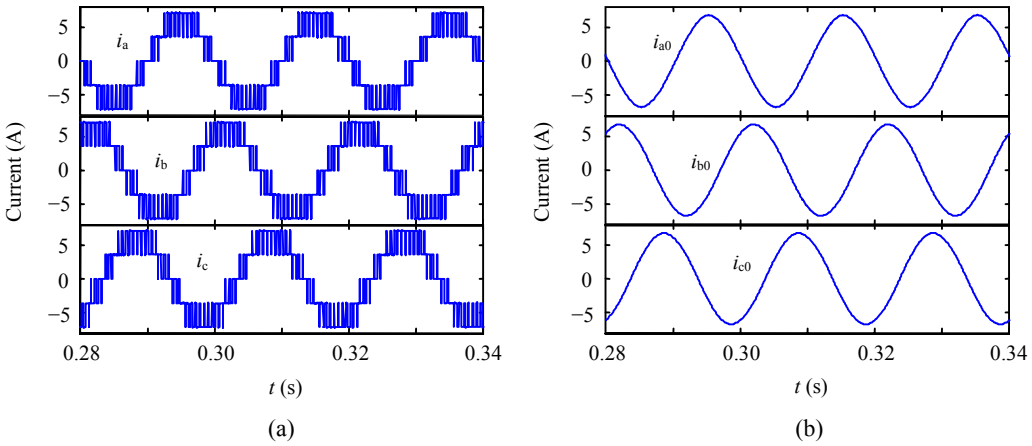

Fig.6 Output current waves. (a) Unfiltered; (b) Filtered

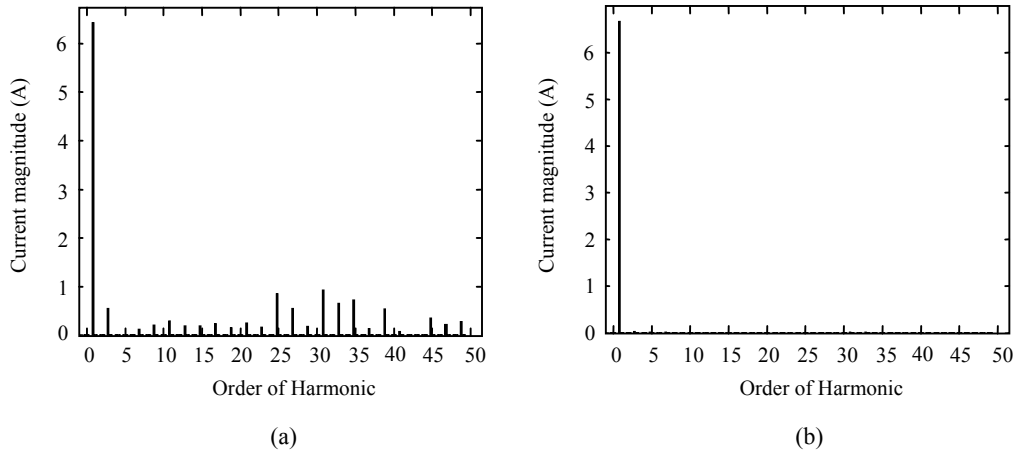

Fig.7 Harmonic spectrum of one phase current. (a) Unfiltered load current i_a; (b) Filtered load current i_{a0}

I_{LA} is very close to $1/2I_d$. Fig.9 shows the unfiltered PWM load current waveforms, Fig.10 shows the filtered load current waveforms which are approximately sinusoidal except for i_{a0}, because the filter elements used in different phase are not very symmetrical.

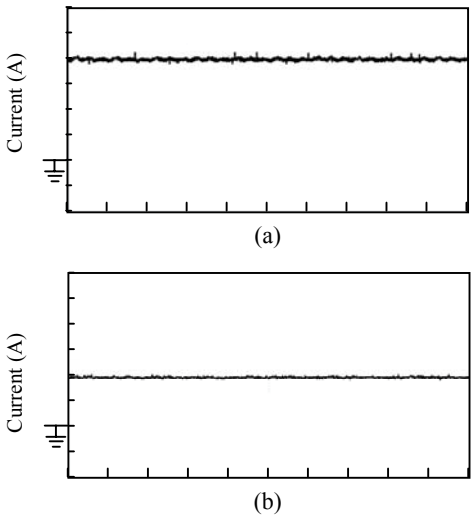

Fig.8 DC current waves. (a) I_d (1 A/div, 10 ms/div); (b) I_{LA} (1 A/div, 10 ms/div)

CONCLUSION

This paper presents a new three-phase 5-level CSI, analyzes and simulates its operational principle. By the implementation of the POD-PWM technique and the intermediate DC-link current-balancing control strategy in each single-phase CSI cell respectively, the three-phase 5-level CSI with balance controlled intermediate DC-link current is POD-PWM con-

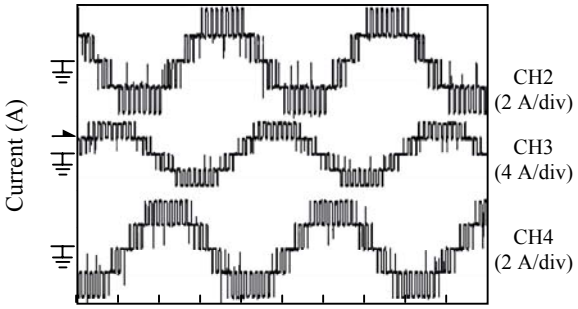

Fig.9 Unfiltered PWM load current (5 ms/div)

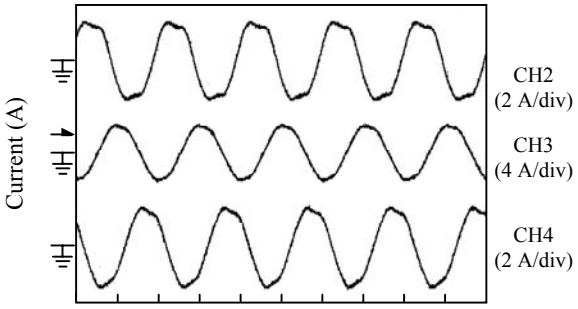

Fig.10 Filtered load current (10 ms/div)

trolled to achieve a sinusoidal output with minimal harmonic distortion. Simulation and experimental results are included in the paper to validate this new topology.

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