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Physical design method of MPSoC*

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Abstract: Floorplan, clock network and power plan are crucial steps in deep sub-micron system-on-chip design. A novel diagonal floorplan is integrated to enhance the data sharing between different cores in system-on-chip. Custom clock network containing hand-adjusted buffers and variable routing rules is constructed to realize balanced synchronization. Effective power plan considering both IR drop and electromigration achieves high utilization and maintains power integrity in our MediaSoC. Using such methods, deep sub-micron design challenges are managed under a fast prototyping methodology, which greatly shortens the design cycle.

Key words: Physical design, Fast prototyping, Floorplan, Clock tree synthesis (CTS), Power plan, Multiprocessor system-on-chip (MPSoC)

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INTRODUCTION

The methodology of multiprocessor system-on-chip (MPSoC) is employed commonly by logic designers today for the sake of flexibility and reusability while process technology continues its revolution represented by characteristic size's scaling down, but the reasons drive gate count growing rapidly. Huge number of transistors, serious signal integrity, large wire delay, and power supply crisis, etc. give greater challenges to back-end designers than ever before.

In order to shorten the design cycle, silicon virtual prototyping method (SVP) is quickly accepted by back-end designers (Dai *et al*., 2003; Mehrotra *et al*., 2003). It is a fast implementation of the physical design to evaluate design trade-off and create a realistic implementation plan, but SVP mainly depends on new advanced tools. Traditionally chips are divided into rectangular blocks and symmetry is maintained to favour later placement and routing (Ito *et al*., 2003; Khan, 2004; Kalla *et al*., 2004). To minimize skew and decrease phase delay between source and sinks, custom clock circuits used in clock tree synthesis (CTS) step become popular for high frequency requirement (Zhu and Chan, 2001; Warnock *et al*., 2002; Lo *et al*., 2003). Unfortunately using this method may greatly increase complexity and design cycle.

The MediaSoC322xA (MediaSoC for short) chip is aimed at multimedia application (Liu, 2006). It integrates a 32-bit RISC general processor (Xiao *et al*., 2006) and a 32-bit MediaDSP (Liu *et al*., 2004). The general processor performs control of the whole system in conjunction with audio decoding, while the MediaDSP acts as a video decoder. Other application specific integrated circuit (ASIC) modules are also integrated into MediaSoC, including TV-encoder, synchronous or asynchronous RAM controllers and direct memory access (DMA) modules.

Dual cores, huge number of gates, many clock domains and related timing goals pose great physical design difficulty. Based on SVP methodology and our experimental work, a fast prototyping method is proposed to cope with the uncertainties of deep sub-

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micron problems. Instead of rectangular symmetry floorplan, we used a diagonal floorplan to decrease path delay. An interactive CTS makes rapid and effective clock design possible. Early power estimation is also integrated into our design to guide power network distribution. In the following sections of this paper, the design methodology of coping with dual cores, implementations with floorplan, clock network, and power distribution for MediaSoC are described, with results also presented.

FAST PROTOTYPING METHODOLOGY

Integration and interconnection make the old design methodology obsolete. Tools are ineffective and even collapse when the number of gate count exceeds a certain boundary. Deep sub-micron (DSM) technology decreases gate delay but increases the wire delay dramatically, which increases the timing uncertainty of a project. Designers have to use pessimistic models to preserve sufficient budget to ensure that later steps do not fail.

To overcome uncertainties of design and in proper time give a concrete feedback during the design process to help logic designers find the effective way, fast prototyping method is proposed based on our experiments. It is a practical approach for dealing with increased complexity and the challenges of timing closure with DSM silicon. Fast prototyping is the first stage of back-end design and plays an important role in deciding the final results.

Fast prototyping is characterized by simplicity, rapidity, and compatibility. It is simple because there is no big difference between its flow and earlier ones. It includes careful floorplan, fast placement, and trial routing, much like traditional flow, but it uses simple models and a little looser constraints. This leads to short execution time of tools and makes several iterations of prototyping in a day possible. Its rapidity shines as it exploits the design cycle slot, so design of a project may seem like pipelining. Given a partially accomplished net-list, we can use black box model correspondingly, and build a full chip model to validate the physical feasibility of the net-list and check whether timing specification can be reached. Compatibility exists because carrying out this methodology does not mean you have to change or upgrade your tools thoroughly. This means decreased expenditure and shorter time of acclimation to new tools.

In this way, back-end designers are more active than before. They can give suggestions based on the practice of layout. When any fallacy or pitfall is confirmed, feedback is sent to front-end designers in time. This means designers can work in parallel. Reasonable timing budget and area pre-plan greatly favour flexibility and correctness.

As a case study, our design flow is shown in Fig.1. It is divided into two major stages, i.e. fast prototyping and real implementation. In fast prototyping, floorplan iterations are done to generate different plans and solutions although some modules have not been optimized yet. After each floorplan, fast placement and trial routing are also carried out to help construct a physical silicon model. Power analysis is done based on net-list extracted from trial route, the result of which gives preliminary consumption information that can be used for optimization of power design. When the full net-list is

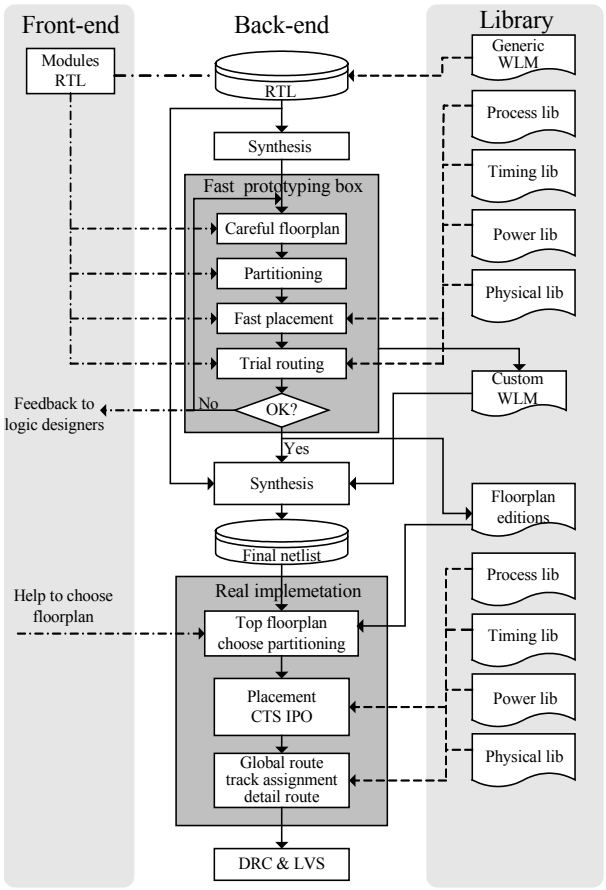


Fig.1 Design flow overview

finalized, the black box modules are substituted with the editions started. The best one from the comparison is chosen for succeeding processes. In real implementation, partition, placement, CTS, routing, etc. are done in sequential order.

NEW IMPLEMENTATION METHODS

Diagonal floorplan

Physical design starts from floorplan, which is a crucial step of the project. It was reported that radically symmetric floorplan is used frequently to maintain regularity and physical engineers labour efforts. For instance, layout designers keep rigid symmetry among the whole chip, as two or more processor cores are equal functional ones. Modules and sub-modules inside the cores keep the same characteristics derivatively as data-path of cores are equal. Designers can just concentrate their efforts on one of them and afterward only duplicate it to construct the whole system.

MediaSoC (Fig.2) contains two main processors designed by SoC R&D group of ISEE department of Zhejiang University: a 32-bit RISC general processor, and a 32-bit MediaDSP. The two processors are designed as master-slave architecture. The master processor RISC performs control of audio decoding along with the whole system. The slave processor MediaDSP works as a video decoder. Besides the two main cores, there are some ASIC components, including TV-encoder, synchronous or asynchronous RAM controllers and DMA modules, which are auxiliary components for audio and video decoding work. Real-time playback requires perfect synchronization between audio and video decoding process, so that synchronization controller which acts as a bridge connecting two cores needs special attention to ensure data sharing as fast as possible.

Fig.3 shows the floorplan block diagram of MediaSoC chip, and main cores/modules. The hard macros, including the on-chip memory of two cores and the ASIC components, are located around the whole chip. The soft macros are located in the middle. The most impressive point is that we do not use traditional rectangular block floorplan method. The two cores are both media functional units so lots of data have to be shared promptly. Based on study of the merits of X architecture (Choi *et al*., 2004; Ho *et al*., 2005) and our experimental work (Lai, 2005; Teng *et al*., 2005; Teng, 2006), we raised a diagonal floorplan for dual core (DFFDC) method. The two cores are intentionally placed on both sides of the diagonal line symmetrically, and configuration and communication registers are set in the centre of the chip. Child modules of each core recede from the division line according to their communicational weight. This method ensures inter-core data sharing. The change from traditional rectangular floorplan to diagonal

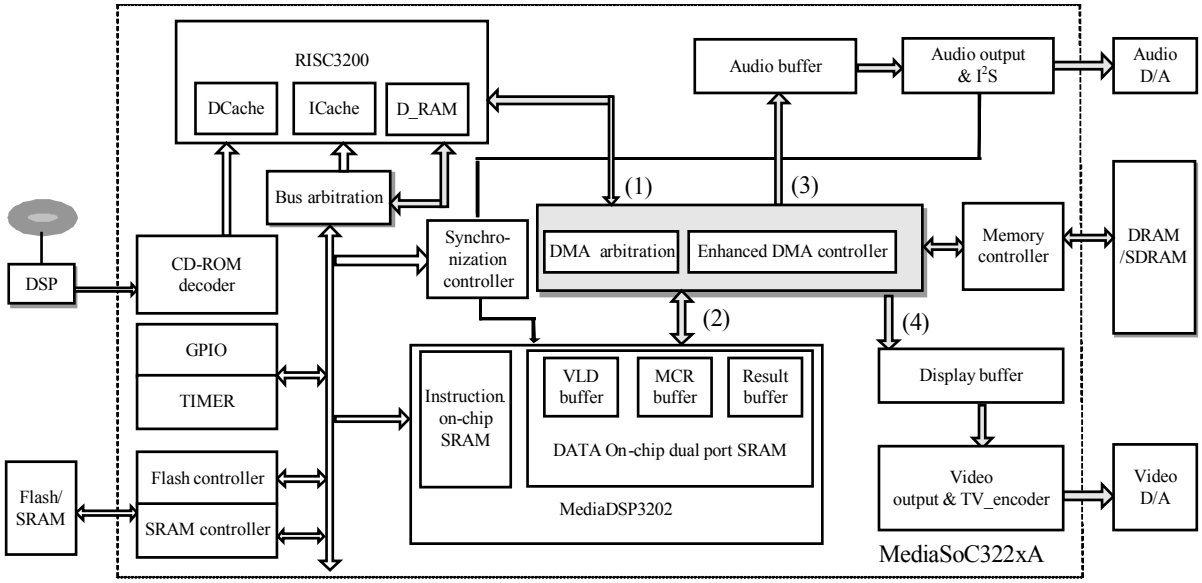
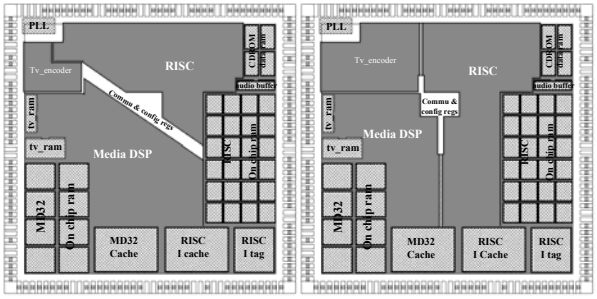


Fig.2 Audio and video decoder multiprocessor system-on-chip structure



(a) (b)

Fig.3 (a) Diagonal floorplan of MediaSoC; (b) Traditional rectangular floorplan

floorplan method is not complex, since all the hard macro locations do not need to be changed. What we do is to adjust the soft macros, especially the location of configuration and communication registers.

The diagonal placement greatly extends the boundary and decreases the access time delay of sharing data. Table 1 shows results comparing the diagonal floorplan and the rectangular floorplan in the worst case. Table 2 provides some physical information on MediaSoC.

Table 1 Results of comparison between the traditional method and the diagonal floorplan method

Parameters	Methods		Improvement (%)
	Traditional	DFFDC	
Timing (ns)	6.8	6.4	5.8
Power (mW)	430	390	9.3
Wire length (nm)	20 143 356	19 532 995	3.0

Table 2 Characteristics of the MediaSoC chip fabricated in SMIC 0.18 μm CMOS process technology

Parameters	Value
Power	<2 mW/MHz
Transistors (million)	5.7
Timing (ns)	6.4
Power supply (V)	3.3 (I/O); 1.8 (core)
Die size	4.7 mm×4.7 mm
Clock frequency*	200 MHz

* Testing condition: V_{dd}=1.8 V, room temperature is 25 °C

Clock network

For the sake of flexibility, MediaSoC is designed to run at several configurable frequencies. Table 3 lists the clocks used in MediaSoC. The coordination of multi-clock domains is another challenging work for modern back-end designers. Synchronous and asynchronous signals are both heavily used in our design. The timing information for CTS is obtained from the design constraint file. Some timing information can be changed and set upon tool's analysis and reports dynamically.

Our CTS is logically divided into two steps, i.e. inter-module level and intra-module level, with respect to hierarchy methodology. At inter-module level, wires are permitted to cross macros or other modules. The two cores use relatively high frequency and need special attention. Equal length channels are preserved for certain area to help build global clock networks. Inside module, symmetric H-trees (Tutuianu *et al*., 1996) are constructed mainly by tools to achieve minimum skew.

In layout design, clock buffers and inverters which constitute the whole clock network draw much attention from designers. In order to increase drive capability and improve cell intrinsic delay, special clock buffer circuit or custom buffer cells are used. This does improve timing performance but requires a long design cycle. We use an interactive CTS methodology for effective clock network. Buffer cells used in level 1 or 2 are big ones in standard cell library due to the large number of their successors, and their positions are adjusted by hand when tools are unable to tackle them gracefully. For example, there are redundant ones placed too closely, which may lead to congestion in later detailed routing step. Little adjustment may yield surprising improvement in timing performance since buffers are very sensitive to positions. As a matter of fact, not only tools auto placement is employed, but hand

Table 3 Clock domains and comparison of traditional and interactive CTS results show of MediaSoC

Clocks	Frequency (MHz)	Number of sink pins	Number of buffers		Skew (ps)	
			Traditional CTS	Interactive CTS	Traditional CTS	Interactive CTS
clk-core	202.5	15 847	495	480	120	95
clk-biu	81	1189	44	42	187	142
clk-81m-out	81	425	17	16	150	120
clk-27m-out	27	733	18	18	155	140
DMA	81	N/A	N/A	N/A	N/A	N/A

adjusting of buffer cell locations is integrated during clock tree construction. This interactive adjustment of clock tree buffers becomes an important step in our design process. Inter-module signals, e.g. buses need big buffers too due to the excessive capacitive load of such wires. Delay cells are strictly prohibited in CTS as they greatly disturb the path timing. Blockages and route guides are employed in this step to force the tree's even distribution.

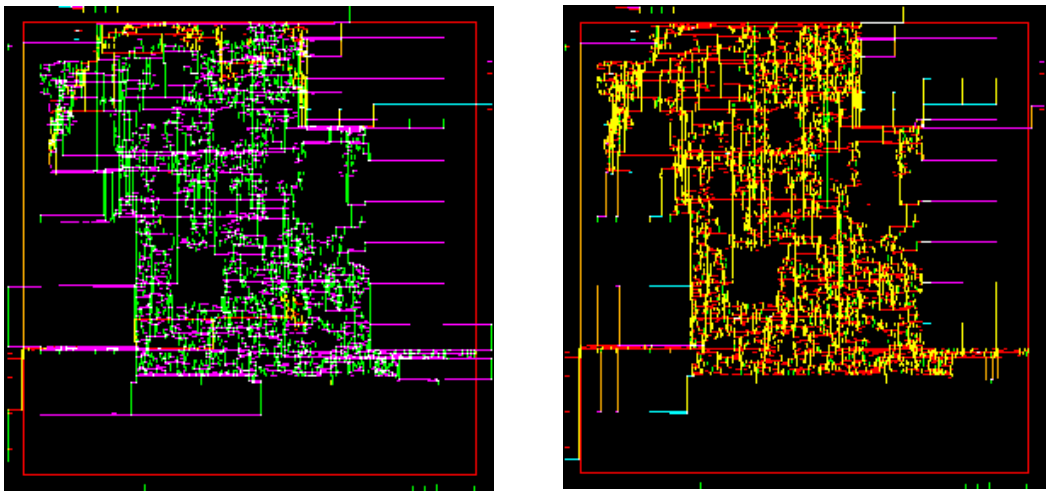
To minimize the length and phase delay, higher metal layers are devoted to connect clock signals, relieving other signals from their high toggle rate. Besides, user-defined width is set to decrease resistance. Results showed that this method works well because it is flexible and easy to implement.

Buffer cells in clock network are carefully handled and wire connections are revised. Metal 2 and Metal 3 are heavily used during normal route procedure; the final utilizations reach 18% and 25% respectively. Metal 5 and Metal 6 each has a utilization of 19.7% and 17.8%. This is attributed to the route blockages above on-chip SRAMs which make routing resources below Metal 5 unavailable, so the effective density of Metal 2 and Metal 3 is much higher than those of Metal 4 and Metal 5 within standard cell logic area. As congestion map is a key factor in coupling capacitance computation (Lou and Chen, 2004), high metal density will definitely lead to worse coupling map. Moreover, high toggle rate of clock network may decrease adjacent signal propagation speed and even cause timing failure by capacitive noise.

In order to wire the clock network efficiently, a custom routing rule for clock is employed to achieve the goal of even distribution of metal wires and minimizing noise coupling effects. First, wires for clock routing are constrained to Metal 4 and Metal 5, then the spacing between these wires are doubled. Full clock network is shown in Fig.4, with Fig.4a using Metals 4/5 and Fig.4b using 2/3. Comparison results between traditional CTS and the interactive CTS scheme are shown in Table 3. Finally, a skew of 95 ps at almost 16000 sink nodes is achieved. Compared to custom buffer or circuit design, our result is more flexible and efficient, and design cycle is minimized.

Power network design

With today's rapidly shrinking in process technology, narrow metal width confines the amplitude of current meanwhile. IR drop increases and signals slow down notably. It had been pointed out that 5% drop in supply voltage may slow down the circuit performance by as much as 15% or more (Yim *et al*., 1999). This may cause circuit malfunction. The fluctuation of voltage for transistor must be kept in a small range, usually within 10% of supply voltage. For timing consideration, it is necessary to minimize delay variation introduced by IR drop. While IR drop is prone to cause timing problem, electromigration (EM) which shows up itself in high current density power lines has killed more and more ICs. Continuous scaling reduces areas of section although aspect



(a) (b)

Fig.4 Clock tree using metal layer 4/5 (a) and using 2/3 (b)

ratio increases steadily. The easy and efficient way is to keep abundant power lines to millions of logic gates. Static and dynamic simulations should be integrated into design in early floorplan step, which may generate effective power models as references for power planning. The power model analysis results will help to get a better Power/Ground network.

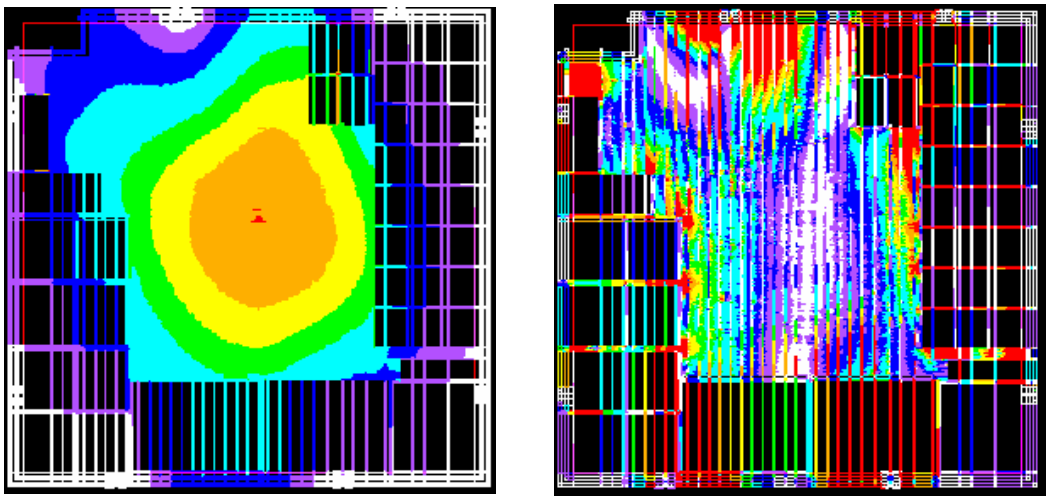
An efficient power/ground network analysis based on library parameters is used to compute power lines width for the whole chip to ensure sufficient supply (Wu and Chang, 2004). During logic design, power model is constructed after each module had been simulated; this serves as reference for power evaluation for floorplan step quantitatively. Based on simulation results and value change dump (VCD) files, toggle rate is acquired for static analysis of power consumption.

In fact, both cores are low power consumption ones in physical design of MediaSoC. Keeping sufficient power lines width and minimizing area overhead to achieve high utilization has become the main goal of our power design. Power pads are exactly computed and placed to keep even distribution. The number of power pads is maximized to satisfy chip consumption. Stacked vias are inserted to make layer connections parallel so that resistance decreases. Core rings are doubled to provide expressway to cores/modules. Power strips in the standard cell area are moved from low layers to high layers to avoid collision with succeeding signal routing and spare some area for cell placement. This change effectively decreases search and repair time by 35%. Overlapping power routing is allowed based on congestion to minimize area overhead, so more placement and route resources are available. The diagonal floorplan favours power design too because perpendicular power lines easily traverse the body of the two cores, which are main consumer of power supply. Fig.5 shows IR drop and electromigration results. Using diagonal floorplan reduced the worst case voltage drop from 110 mV to 100 mV and electromigration violation decreased by 20%. Power dissipation result is given in Table 1.

CONCLUSION

This multiprocessor SoC is fabricated in SMIC advanced 0.18 μm CMOS process with 6 layers of Al and a dielectric of SiO_2. The transistor count is about 5.7 M, of which 4 M is SRAM. The 22 mm^2 die is packaged in a 144-pin PQFP. Its power consumption is less than 400 mW at clock frequency of 200 MHz. It has already passed tests of real-time playback of MPEG 1 coded streams at 162 MHz and MPEG 4 SP @L3 decoding at 81 MHz (Ni, 2006).

Using fast prototyping methodology helps a lot to achieve a fast turn-around time. The diagonal floorplan method to balance the timing budget of each core is the key point of successful implementation.



(a) (b)

Fig.5 (a) IR drop map; (b) Electromigration result

The clock and power network turned out to be highly efficient as final utilization has reached 77%. Results showed that our methods are practical and effective. Future work will be focused on research of high performance multiprocessor SoC of 130 nm process technologies.

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