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A robust polysilicon-assisted SCR in ESD protection application*

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Abstract: A novel polysilicon-assisted silicon-controlled rectifier (SCR) is presented and analyzed in this paper, which is fabricated in HHNEC's 0.18 μm EEPROM process. The polysilicon-assisted SCRs take advantage of polysilicon layer to help bypass electro-static discharge (ESD) current without occupying extra layout area. TLP current-voltage (*I-V*) measurement results show that given the same layout areas, robustness performance of polysilicon-assisted SCRs can be improved to 3 times of conventional MLSCR's. Moreover, one-finger such polysilicon-assisted SCRs, which occupy only 947 μm^2 layout area, can undergo 7-kV HBM ESD stress. Results further demonstrate that the S-type *I-V* characteristics of polysilicon-assisted SCRs are adjustable to different operating conditions by changing the device dimensions. Compared with traditional SCRs, this new SCR can bypass more ESD currents and consumes smaller IC area.

Key words: Electro-static discharge (ESD), Silicon-controlled rectifier (SCR), Robustness performance, Polysilicon-assisted, Human body model (HBM)

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INTRODUCTION

ESD (electro-static discharge) is one of the most important issues on IC reliability. As the technology is scaled down constantly, the demand for high performance ESD protection devices is becoming more and more urgent (Wang, 2004; Wang *et al*., 2005; Chang and Ker, 2007; Lin and Ker, 2007; Si Moussa *et al*., 2007). ESD protection in ICs is established by involving integration of the input/output (I/O) protection and the supply clamp. These protection components are typically implemented with diodes, MOSFETs, bipolar junction transistors, and sometimes Silicon-controlled rectifiers (SCRs). Robustness performance is one of the most important concerns that should be taken into account when designing such ESD protection devices (Salcedo *et al*., 2005; Liou *et al*., 2007). Although MLSCR, one of the conventional SCRs, has better robustness performance than other traditional devices in double-well submicron technology, the robustness requirements can be obtained only by multiplying the MLSCR's fingers. In general, multi-finger devices consume much more area than one-finger ones. Facing the challenge of robustness performance and over-sized IC area, novel polysilicon-assisted SCRs are developed and analyzed in this paper.

STRCUTURES AND TERMINAL CONNECTION

The conventional SCR-based ESD protection device's structure, named as MLSCR, is demonstrated in Fig.1. An N+ region is located above the boundary region of NWELL and PWELL. One of the novel SCR-based ESD protection devices' structures, named as FDSCR (Forward Diode Silicon Controlled Rectifier), is depicted in Fig.2, from which we can observe that the device is built with two parts: substrate silicon and polysilicon. The two parts are par-

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alleled, thus the device can bypass more current under ESD without extra layout areas. Polysilicon part actually consists of paralleled diodes (Fig.2b). Every diode is formed with P-type polysilicon, intrinsic polysilicon and N-type polysilicon. The holes in the polysilicon layer ensure that N+ implant can go through to form N+ region bestraddling NWELL and PWELL. There is one STI region surrounding one N+ region in every hole. Substrate silicon part is quite like the conventional MLSCR depicted in Fig.1, except that the N+ region is separated and discontinuous in FDSCR while N+ region is continuous in MLSCR. These devices have been designed in the process of HHNEC's EE180 G. Another SCR-based ESD protection devices' structure, named as RDSCR (Reverse Diode Silicon Controlled Rectifier), is presented in Fig.3. In RDSCR, N-type polysilicon is connected to the anode terminal and P-type polysilicon to the cathode terminal, and this is the only different point from FDSCR. All the SCRs in this paper, no matter MLSCRs, FDSCRs, or RDSCRs, occupy the same layout area (Fig.4 and Table 1). Dimensions of *W* and *D* are the same in all the SCRs. Detailed dimensions of *D* (*D1*~*D5* in Figs.1~3) are also fixed (see Table 1). The value of *L* is changeable in FDSCRs and RDSCRs.

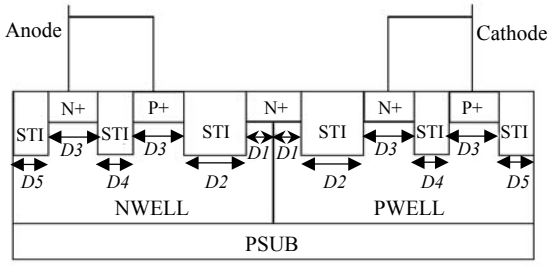

Fig.1 Cross section of conventional MLSCR

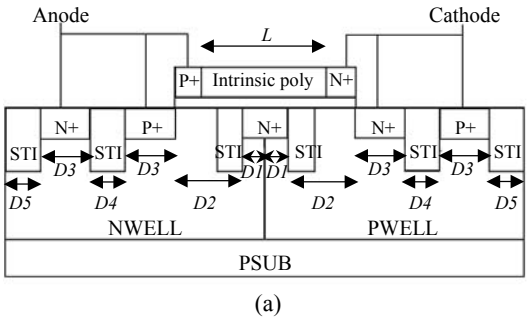

Fig.2 Structure of FDSCR. (a) Cross section of FDSCR; (b) Planform of FDSCR

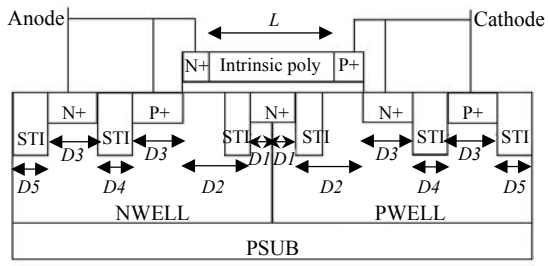

Fig.3 Cross section of RDSCR

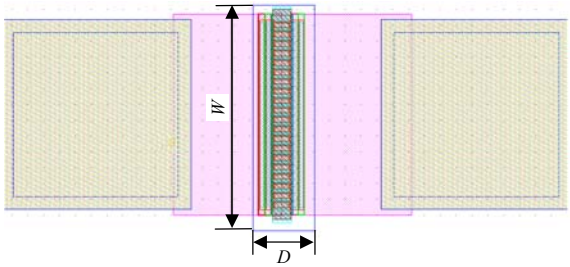

Fig.4 Overall layout of MLSCRs, FDSCRs, and RDSCRs

Table 1 Dimensions (unit: μm) of MLSCRs, FDSCRs, and RDSCRs

Parameters	Values	Parameters	Values
D1	2.14	*D5*	0.36
D2	1.36	*D*	14.70
D3	1.50	*W*	65.00
D4	0.50		

MEASUREMENT RUSULTS OF ROBUSTNESS PERFORMANCE

Fig.5 is the measured TLP *I-V* characteristics of MLSCR, FDSCR and RDSCR. At DP_ML_1, the leakage current of MLSCR increased by three orders, and this device fails at DP_ML_2 as the leakage current increased by another three orders. At DP_FD and DP_RD, the leakage currents suddenly increased by six orders to failure. Area-considered robustness performance is evaluated by "I_{ESD}/μm" and "V_{ESD}/μm^2" as shown in Eqs.(1) and (2):

$$I_{\mathrm{ESD}}/\mu\mathrm{m}=\frac{I_{\mathrm{t2}}}{W}, \tag{1}$$

$$V_{\mathrm{ESD}}/\mu\mathrm{m}^2=\frac{I_{\mathrm{t2}}\times R_{\mathrm{HBM}}}{W\times D}. \tag{2}$$

The leakage current of MLSCR is firstly increased to the order of 10^{-6}~10^{-5}, and then reaches 10^{-3}~10^{-2}, which shows the latent vulnerability of MLSCR's robustness. In contrast, leakage currents of FDSCR and RDSCR increased abruptly from the order of 10^{-9}~10^{-8} to the order of 10^{-3}~10^{-2}. The results show that the robustness performance of FDSCR and RDSCR can be increased by 80%, and that if latent robustness problems taken into account, robustness performance of RDSCR and RDSCR is at least 3 times of that of MLSCR.

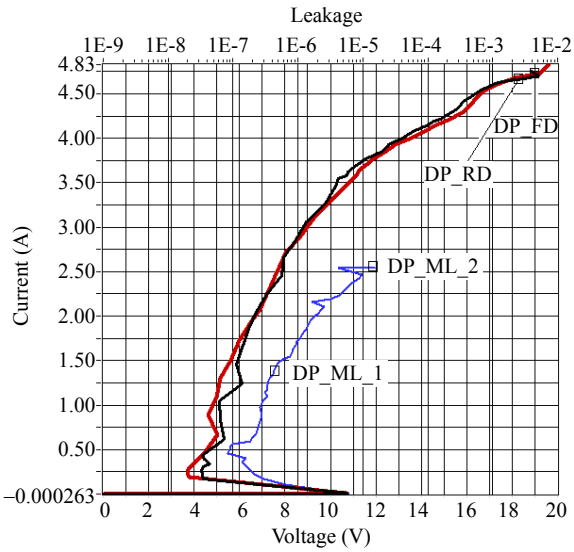

Fig.5 Characteristics of MLSCR, FDSCR and RDSCR

Table 2 Comparing robustness performance. (a) Leakage currents of the three devices; (b) Latent robustness problem ignored; (c) Latent robustness problem considered

(a)

Devices	Leakage currents		
	10^{-9}~10^{-8}	10^{-6}~10^{-5}	10^{-3}~10^{-2}
MLSCR	0<*I*<1.37	1.37<*I*<2.6	*I*>2.60
FDSCR	0<*I*<4.68	–	*I*>4.68
RDSCR	0<*I*<4.66	–	*I*>4.66

(b)

Devices	I_{t2} (A)	I_{ESD}/μm (mA/μm)	V_{ESD}/μm^2 (V/μm^2)
MLSCR	2.60	40.0	4.08
FDSCR	4.68	72.0	7.41
RDSCR	4.66	71.7	7.38

(c)

Devices	I_{t2} (A)	I_{ESD}/μm (mA/μm)	V_{ESD}/μm^2 (V/μm^2)
MLSCR	1.37	21.1	2.15
FDSCR	4.68	72.0	7.41
RDSCR	4.66	71.7	7.38

ROBUSTNESS ANALYSIS AND CHARACTERIZATIONS OF POLYSILICON-ASSISTED SCRS

A four-terminal device is presented in Fig.6a, where FDSCR is separated into two parts. Poly_Anode and Poly_Cathode are two terminals of polysilicon part, with Sub_Anode and Sub_Cathode being the substrate silicon parts. Results of substrate silicon part's and FDSCR's TLP *I-V* characteristics are presented in Fig.6b, and polysilicon part's and FDSCR's characteristics in Fig.6c. The polysilicon part of FDSCR is actually not completely triggered in the ESD event, considering the 36-V trigger voltage shown in Fig.6c and the FDSCR's I_{t2} exceeds the sum of those of substrate silicon and polysilicon. In other words, the robustness of polysilicon-assisted SCR exceeds the sum of those of polysilicon and substrate. The explanation is that the polysilicon part covered above the substrate silicon part induces a high electric field, which can reach the substrate part surface to form a high-conductance carriers layer in ESD event. The temporary high-conductance will improve the bypassing situation of polysilicon-assisted SCRs remarkably.

The relation between dimension of FDSCRs (RDSCRs) and TLP characteristics is given in Table 3. Trigger voltages of FDSCR and RDSCR are quite the same, and not sensitive to the length *L*. This is because triggering of RDSCR and RDSCR is fulfilled by substrate silicon part, and all the substrate SCRs are just the same. Holding voltages of RDSCR are higher than those of FDSCR by about 1 V. Larger *L* will induce larger holding voltages. In practice, larger holding voltages provide better immunities against latch up (Tremouilles *et al*., 2004; Ker and Hsu, 2006). Therefore, connection ways of polysilicon part and different *L* can be utilized to adjust to various operation circuits without inducing latch up damage.

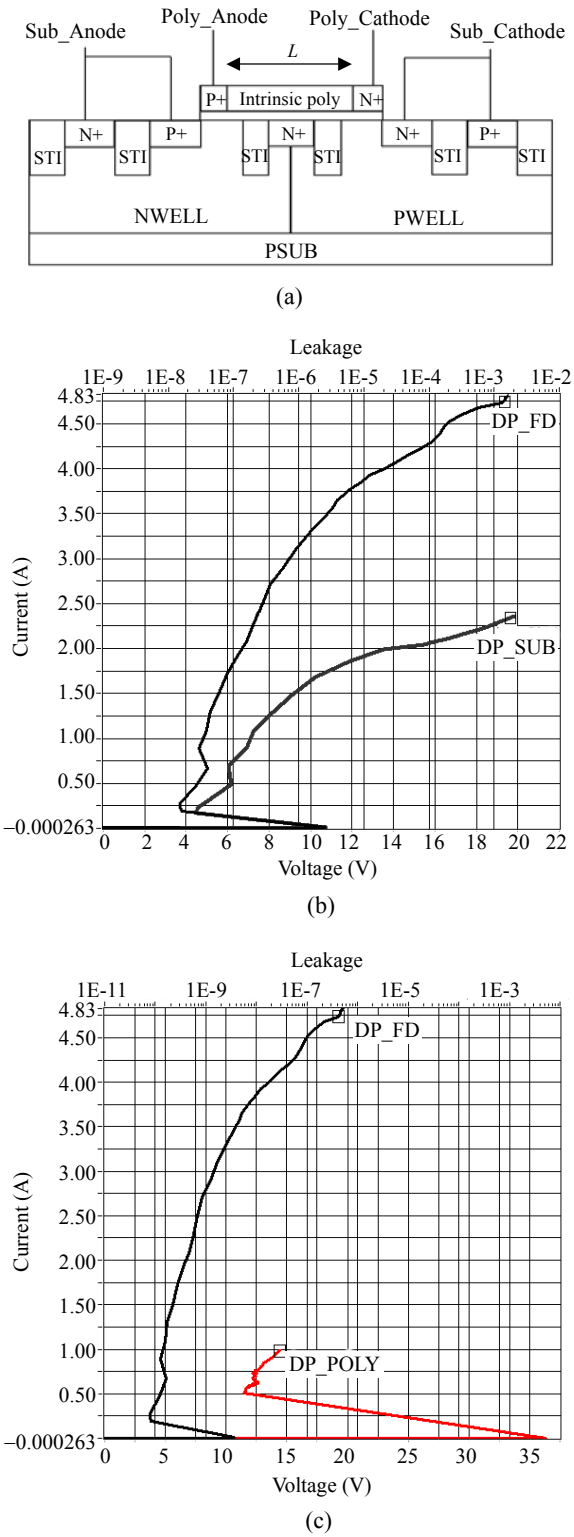

Fig.6 Analysis of FDSCR's robustness. (a) Four-terminal device; (b) Robustness of FDSCR and substrate silicon part; (c) Robustness of FDSCR and polysilicon part

Finally, measurements show that larger intrinsic polysilicon's lengths will induce higher second breakdown currents (I_{t2}). This is because larger polysilicon length L means larger area of substrate silicon part in polysilicon-assisted SCRs influenced by high electric field in ESD event. And, the induced electric field plays a critical role in improving the robustness performance in the polysilicon-assisted SCRs in ESD protection application.

Table 3 Characterizations of FDSCRs and RDSCRs

Devices	L (μm)	V_{t1} (V)	V_h (V)	I_{t2} (A)
FDSCR1	2.5	11.63	3.51	4.22
FDSCR2	5.9	11.69	3.63	4.68
RDSCR1	1.0	11.57	4.45	3.26
RDSCR2	2.5	11.62	4.53	4.34
RDSCR3	5.9	11.69	4.62	4.55

CONCLUSION

Two polysilicon-assisted SCRs have been designed, fabricated and characterized. Measurment results show that given the same layout areas, the robustness performance of polysilicon-assisted SCRs can be improved to 3 times of that of conventional MLSCR, and that one-finger such polysilicon-assisted SCRs, which occupy only 947 μm^2 layout area, can undergo 7-kV HBM ESD stress. Results further demonstrate that the S-type current-voltage (*I-V*) characteristics of polysilicon-assisted SCRs are adjustable to different operating conditions by changing the device dimensions.

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