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Synchronization analysis on cascaded multilevel converters with distributed control*#

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Abstract: Cascaded multilevel converters built with integrated modules have many advantages such as increased power density, flexible distributed control, multi-functionality, increased reliability and short design cycles. However, the system performance will be affected due to the synchronization errors among each integrated modules. This paper analyzes the impact of the three kinds of synchronization errors on the whole system performance, as well as detailed synchronization implementation. Some valuable conclusions are derived from the theoretical analysis, simulations and experimental results.

Key words: Cascaded multilevel converter, Integrated module, Synchronization
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INTRODUCTION

Multilevel converters have become a significant research aspect of power electronic technology due to their many advantages, such as low voltage stress on each component, low harmonic output and EMI emission that make them suitable for high-voltage and high-power applications (Suh and Hyun, 1997; Peng, 2001; Rodriguez *et al*., 2002; Marchesoni and Tenca, 2002). Especially the hybrid multilevel converters can be generalized for different arrangements of DC voltage levels and distinct topologies of multilevel cells, increasing significantly the flexibility of their design (Ghiara *et al*., 1991; Rech and Pinheiro, 2007).

In another way, with the development of semiconductor devices, materials and packaging techniques, power electronics system integration is attracting increasing interest, which is promising to make improvements in quality, reliability, and cost of the whole system. To achieve predicted high performance, many researchers contribute great efforts to investigate the reconfiguration of multi-cell converter structures using integrated modules which are generally composed of power devices, digital controllers, sensors, actuators and so on (Hu *et al*., 2004). These structures have many advantages when compared to the traditional topologies, such as increased power density, flexible distributed control, multi-functionality, increased reliability, lower costs and short design cycles (Lee and Peng, 2000; du Toit and Beukes, 2001). Especially the distributed control scheme enables fault-tolerance technology to be implemented in the new converter structures, because each integrated module is independent, i.e., one module's failure will no longer lead to the whole system collapse (Hu *et al*., 2005).

A number of papers have reported the developments in related aspects. The overview of power electronics building block (PEBB) concept and some of the issues such as the packaging approaches, thermal management, etc., are presented in (Lee and Peng, 2000). In (du Toit and Beukes, 2001), a dis-

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tributed control strategy for multi-cell converters (especially for multilevel converters such as cascaded multilevel converters) is proposed, and the control and communication of integrated modules are discussed. The design methods of the integrated modular controller, including its structure and communication protocol, are introduced in (du Toit *et al*., 1998; Celanovic *et al*., 2000; Hu *et al*., 2004). The reconfiguration of fault tolerant multilevel converters built with basic modules is included in (Hu *et al*., 2005). A flexible loss-minimizing and stress-sharing basic switch cell for power converters is proposed in (Chen *et al*., 2006). But to date, the detailed synchronization effects and requirements of each integrated module to achieve the theoretically predicted system benefits have not been reported. However, the synchronization characteristic is particularly important for PWM strategies for converters with distributed control, since their theoretical harmonic cancellations can only be achieved in practice with the proper synchronization of carrier and reference waveforms (Loh *et al*., 2005). These issues are now addressed systematically in this paper through double Fourier analysis and experimental results of a three-phase five-level cascaded multilevel inverter built with several integrated modules.

The paper discusses the impact on system performance of the cascaded multilevel converter when phase synchronization errors exist between the carriers and three-phase references of each integrated modules. The validity of the analysis is proven by Matlab simulation and experimental results.

DISTRIBUTED PWM MULTILEVEL CONVERTERS BUILT WITH INTEGRATED MODULES

As described in (Hu *et al*., 2004), the integrated module shown in Fig.1 is valid for many topologies, such as half/full bridge converters, rectifiers and inverters. Especially, it is suitable for the applications requiring complex and advanced control schemes such as the cascaded multilevel converters. To show how it operates, a three-phase five-level cascaded multilevel topology under phase-shifted pulse-width modulation (PSPWM) strategy is constructed in this paper. As illustrated in Fig.2, each gray block represents an integrated module.

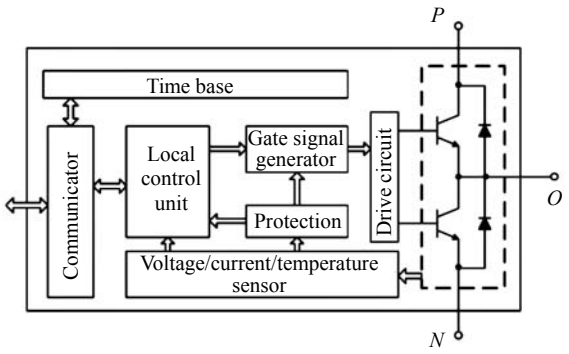


Fig.1 Block diagram of the integrated modules

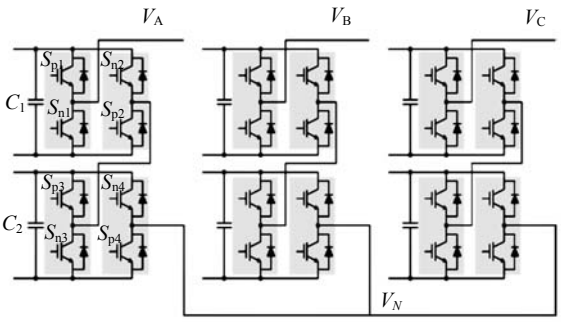


Fig.2 Three-phase five-level cascaded converter with modules

Each module contains two power switches (S_n and S_p) and each with an anti-parallel diode. Its integrated controller can perform many tasks, such as the generation of complementary pulse-width modulation (PWM) signals for S_n and S_p, the generation of dead band, the detection of fault, and the communication with other modules or upper level controllers. The drive for two power switches is realized by a special chip integrated inside. In addition, protection and isolation functions can also be implemented in the module.

To achieve appropriate output for a multilevel converter built with integrated modules, synchronization of their digital controllers is necessary. When the PSPWM strategy is applied, each controller must generate its own proper carrier and reference signals inside its module separately, and waits for the synchronization signal sent by the upper controller for synchronizing modules' working to start its own comparison of its carrier and reference at the beginning of each fundamental cycle. Its detailed implementation will be discussed in Section 4.

SYNCHRONIZATION OF INTEGRATED MODULES

As illustrated in Fig.2, each phase leg comprises four modules, i.e., there are four controllers in one phase leg. So for an N-level topology, $N-1$ controllers must be provided. The synchronization mode for all controllers can be summarized as carrier synchronization and reference synchronization. This section will analyze the impact of synchronization errors on the output voltage performance of a three-phase five-level cascaded topology under PSPWM strategy.

Synchronization analysis

According to the PSPWM principle described in (Holmes and Lipo, 2003), as illustrated in Fig.3, the gate signal is generated by comparison of the sinusoidal reference with the triangular carrier. The carrier frequency is set to be an integral multiple of the reference frequency generally; the harmonics of the switched waveforms can then be expressed as a double summation Fourier series:

$$\begin{aligned}U_{\mathrm{g}}(\alpha)&=(1+M\sin\omega_{\mathrm{r}}t)/2+\\&\sum_{m=1,3}^{\infty}\{2/(m\pi)\sin[m(\omega_{\mathrm{c}}t-\pi/2+\alpha)]J_0(m\pi M/2)\}-\\&\sum_{m=1,3}^{\infty}\sum_{n=2,4}^{\infty}\{2/(m\pi)J_n(m\pi M/2)\sin[m(\pi/2-\alpha)]\cdot\\&\quad[\cos(m\omega_{\mathrm{c}}t-n\omega_{\mathrm{r}}t)+\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{r}}t)]\}+\\&\sum_{m=2,4}^{\infty}\sum_{n=1,3}^{\infty}\{2/(m\pi)J_n(m\pi M/2)\cos[m(\pi/2-\alpha)]\cdot\\&\quad[\sin(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{r}}t)-\sin(m\omega_{\mathrm{c}}t-n\omega_{\mathrm{r}}t)]\}+\\&\sum_{m=1,3}^{\infty}\sum_{n=2,4}^{\infty}\{2/(m\pi)J_n(m\pi M/2)\cos[m(\pi/2-\alpha)]\cdot\\&\quad[\sin(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{r}}t)+\sin(m\omega_{\mathrm{c}}t-n\omega_{\mathrm{r}}t)]\}+\\&\sum_{m=2,4}^{\infty}\sum_{n=1,3}^{\infty}\{2/(m\pi)J_n(m\pi M/2)\sin[m(\pi/2-\alpha)]\cdot\\&\quad[\cos(m\omega_{\mathrm{c}}t-n\omega_{\mathrm{r}}t)-\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{r}}t)]\},\end{aligned}\tag{1}$$

where α is the phase-shifted angle of the carrier, ω_{r} and ω_{c} are the angular frequencies of the reference and the carrier, respectively, and M is the modulation index. Because each carrier is phase shifted by $\pi/2$ from its adjacent one under the PSPWM strategy, the four gate signals are thus expressed as

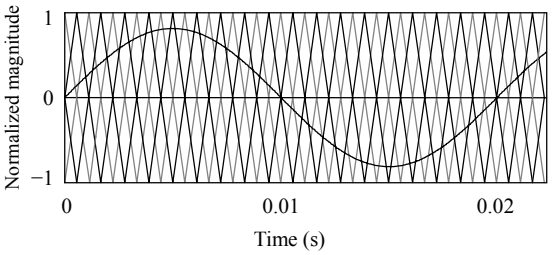


Fig.3 The carrier and the reference waveforms for PSPWM strategy

$$U_{\mathrm{g}i}=U_{\mathrm{g}}\left(\frac{i-1}{2}\pi\right),\quad i=1,\ 2,\ 3,\ 4.\tag{2}$$

The phase voltage waveform can then be expressed in simplified form using the double Fourier analysis method

$$\begin{aligned}U_{\mathrm{out}}&=2M\sin\omega_{\mathrm{r}}t+\sum_{m=4,8}^{\infty}\sum_{n=1,3}^{\infty}\{2/(m\pi)J_n(m\pi M/2)\cdot\\&\cos[m(\pi/2-\alpha)][\sin(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{r}}t)-\sin(m\omega_{\mathrm{c}}t-n\omega_{\mathrm{r}}t)]\}.\end{aligned}\tag{3}$$

Eq.(3) describes that only the four times carrier frequency sideband harmonic components exist, which can be expressed as $4k\omega_{\mathrm{c}}\pm n\omega_{\mathrm{r}}$ (k=1,2,3,… and n=1,3,5,…). The Matlab simulation results of the phase leg voltage waveform and its FFT spectrum are shown in Fig.4, where the carrier frequency is 3 kHz, the reference frequency 50 Hz, and the modulation index M=0.8. It can be seen from Fig.4 that the sideband harmonics are centered about the quadruple multiples of the carrier frequency, and the most significant sideband harmonic is at 12 kHz.

Impact of carrier synchronization error under PSPWM on output voltage

Only carrier synchronization error between two modules in the same phase leg is considered here as an example. According to the above analysis, the gate signals can then be expressed as

$$U_{\mathrm{g}i}=U_{\mathrm{g}}\left(\frac{i-1}{2}\pi+e_i\right),\quad i=1,\ 2,\ 3,\ 4.\tag{4}$$

Combining Eq.(1) and Eq.(4), the expression of the phase voltage can be derived through the double Fourier analysis (Due to its complication, the expression is not presented here). Fig.5 and Fig.6 illustrate

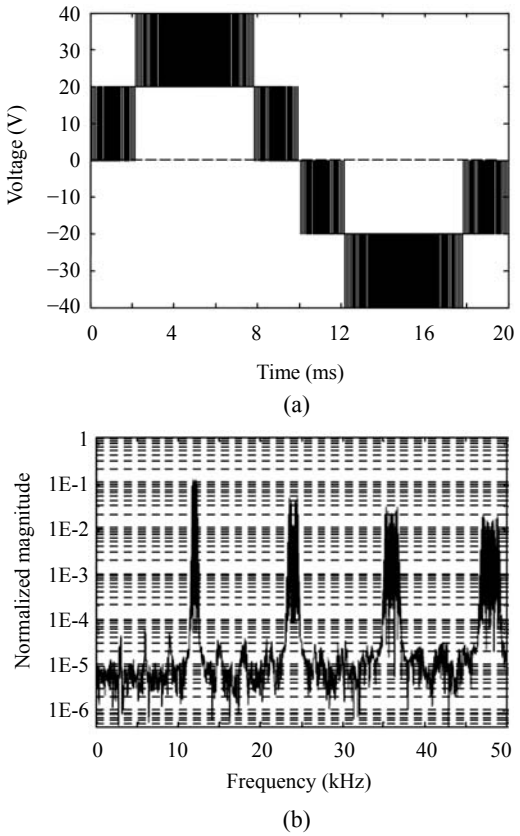


Fig.4 Simulation results under the normal condition (reference frequency: f_r=50 Hz, carrier frequency: f_c=3 kHz, M=0.8). (a) The phase leg voltage waveform; (b) FFT spectrum of the phase leg voltage (normalized to phase leg voltage)

the impact of carrier synchronization error on output phase leg voltage, where $e_2=e_3=e_4=0$, $e_1=\pi/30$ in Fig.5 and $e_1=2\pi/333$ in Fig.6, respectively. As shown in Fig.5 and Fig.6, the low order carrier sideband harmonics in the phase voltage are introduced due to the carrier synchronization error. Meanwhile, with the carrier synchronization error increased, low order harmonic components increase, which means that the THD of the output voltage will increase because of the presence of these low frequencies harmonic energies.

Table 1 shows the comparison of the phase voltage between the theoretical values with double Fourier analysis and the simulation results with Matlab when carrier synchronization error is considered. The table clearly shows that the even harmonic sideband components locate around odd multiples of the carrier fundamental, and odd harmonic sideband components exist around even multiples of the carrier fundamental. The normalized magnitudes of these harmonics can also be seen in the table. These additional harmonic energies contribute considerably to the THD of the output phase leg voltage.

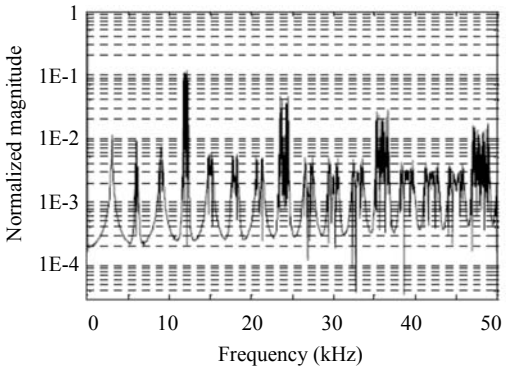


Fig.5 Simulation results of FFT spectrum of the phase voltage with carrier phase error being 5.55 μs (reference frequency: f_r=50 Hz, carrier frequency: f_c=3 kHz, M=0.8, normalized to the phase leg voltage)

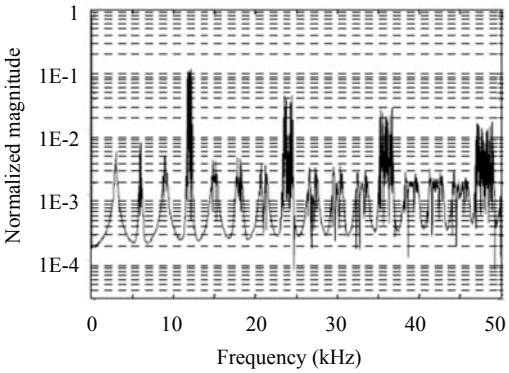


Fig.6 Simulation results of FFT spectrum of the phase voltage with carrier phase error being 1 μs (reference frequency: f_r=50 Hz, carrier frequency: f_c=3 kHz, M=0.8, normalized to the phase leg voltage)

Table 1 Normalized magnitude of harmonics with different carrier synchronization errors (e_1)

Harmonic order	Normalized magnitude			
	$e_1=\pi/30$		$e_1=2\pi/333$	
	Theoretical values	Simulation results	Theoretical values	Simulation results
ω_c	0.0214	0.0215	0.0039	0.0038
$\omega_c\pm2\omega_r$	0.0057	0.0060	0.0010	0.0010
$2\omega_c\pm\omega_r$	0.0164	0.0165	0.0030	0.0031
$2\omega_c\pm3\omega_r$	0.0073	0.0074	0.0013	0.0013
$3\omega_c$	0.0133	0.0135	0.0024	0.0025
$3\omega_c\pm2\omega_r$	0.0138	0.0141	0.0025	0.0024
$4\omega_c\pm\omega_r$	0.1035	0.1092	0.1051	0.1111
$4\omega_c\pm3\omega_r$	0.1128	0.1207	0.1146	0.1030

Impact of reference synchronization error under PSPWM on output voltage

Only the reference synchronization error is considered here. The gate signals are determined by replacing $\omega_r t$ with $\omega_r t+e$ in Eq.(1), the expression of the phase voltage is not presented. Assume that only one module's reference of one phase leg is not in-phase, Fig.7 and Fig.8 can then be obtained through Matlab simulation, where errors of 333 μs and 1 μs (i.e., $e=\pi/30$ and $e=\pi/10\,000$, respectively) are illustrated in Fig.7 and Fig.8, respectively. Besides spectral plots, Table 2 shows the comparison of the phase voltage between the theoretical values with double Fourier analysis and the simulation results with Matlab when carrier synchronization error exists. The conclusion of this case is similar to the above one, and a major difference between the two cases is the absence of odd multiples carrier components, which leads to the variation of harmonics arrangements.

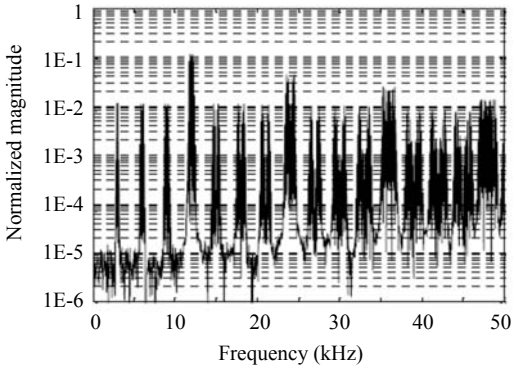


Fig.7 Simulation results of FFT spectrum of the phase voltage with reference phase error being 333 μs (reference frequency: f_r=50 Hz, carrier frequency: f_c=3 kHz, M=0.8, normalized to the phase leg voltage)

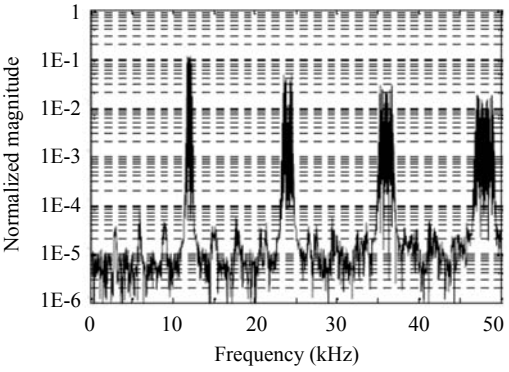


Fig.8 Simulation results of FFT spectrum of the phase voltage with reference phase error being 1 μs (reference frequency: f_r=50 Hz, carrier frequency: f_c=3 kHz, M=0.8, normalized to the phase leg voltage)

Table 2 Normalized magnitude of harmonics with different reference synchronization errors (e)

Harmonic order	Normalized magnitude			
	$e=\pi/30$		$e=\pi/10\,000$	
	Theoretical values	Simulation results	Theoretical values	Simulation results
$\omega_c\pm2\omega_r$	0.0115	0.0114	3.4533E-5	3.801E-5
$2\omega_c\pm\omega_r$	0.0082	0.0082	2.4689E-5	5.398E-5
$2\omega_c\pm3\omega_r$	0.0109	0.0112	3.2861E-5	2.051E-5
$3\omega_c\pm2\omega_r$	0.0092	0.0085	2.7686E-5	2.065E-5
$4\omega_c\pm\omega_r$	0.1051	0.1107	0.1052	0.1111
$4\omega_c\pm3\omega_r$	0.1136	0.1022	0.1147	0.1030

Impact of sampling synchronization error under PSPWM on output voltage

When the PSPWM modulation strategy is implemented digitally with the three-phase references regularly sampled, the sampling synchronization error must be considered. To achieve theoretical harmonic cancellation for the PSPWM modulation strategy, it is necessary to phase shift the sampling points correctly (McGrath and Holmes, 2002). Many ways of synchronizing the samplings are possible, and an optimal way is that the sinusoidal reference is sampled at the peaks or bottoms of the respective phase-shifted carriers. Fig.3 shows that four 90° phase-shifted carriers are needed in one phase for a five-level cascaded multilevel converter, so the sampling points should be shifted by 90° with each other to achieve the predicted output performance. From Fig.9 it can be seen that the sampling synchronization error is equivalent to the carrier synchronization error. So the output performance when the sampling synchronization error exists is identical to the one when the same carrier synchronization error exists. The method discussed in Section 3.2 is feasible for the analysis of the sampling synchronization error as long as the same carrier synchronization error is adopted instead of the sampling synchronization error. So the detailed analysis will not be duplicated here.

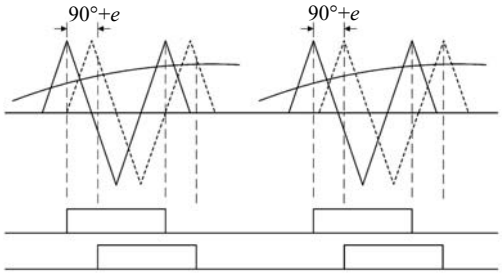


Fig.9 Equivalence relationship between the samplings synchronization error and the carrier synchronization error

Some conclusions can be derived from the analysis above. First, both synchronization errors will lead to additional low order carrier sideband harmonics in the phase leg output voltage, the THD of the output voltage will also increase as synchronization errors increase. But when the errors are tiny, the effects of the synchronization will be ignored. Secondly, the carrier synchronization error affects the output voltage performance more significantly than the reference synchronization error, mainly because more harmonic components are produced with the carrier synchronization error compared to that with the reference synchronization error. Thirdly, these low frequencies harmonic components produced by both synchronization errors cannot be cancelled in the *l-l* output voltage, except for the expected intrinsic cancellation of triple harmonics between the phase legs.

SYNCHRONIZATION IMPLEMENTATION

To achieve optimal synchronization performance, practical synchronization implementation is crucial for the whole system. Due to the high performance of digital controller integrated inside the module, the digital phase lock technique can be used to achieve the synchronization of carriers and references. And the synchronization method introduced in this paper can minish the synchronization errors effectively.

First, one controller acts as a master controller and sends out a common square synchronization signal which has the same period with the reference signal to other slave controllers. Second, upon receiving the common square synchronization signal, the slave controllers measure their respective carrier phase shift and reference phase shift. This common square synchronization signal is the time base not only for the carrier synchronization, but also for the reference synchronization.

For the synchronization of carriers within a five-level cascaded inverter, four modules' controllers add appropriate offsets to the common square synchronization signal as their own carrier phase signals, i.e., 0, $\pi/2$, π, $3\pi/2$ are for the four controllers, respectively, and the carriers are synchronized only once throughout each fundamental cycle. The accurate carrier signal can then be obtained from its carrier phase signal using phase lock algorithm provided by the integrated controller.

For the synchronization of reference within a three-phase cascaded inverter, three-phase legs' controllers add appropriate offsets to the common square synchronization signal as their own reference phase signals, i.e., 0 for Phase A, $-2\pi/3$ for Phase B and $2\pi/3$ for Phase C, respectively, and the proper reference signal can be implemented similarly.

EXPERIMENTAL RESULTS

Experimental facility

To verify the validity of above analysis, a three-phase five-level cascaded inverter under PSPWM modulation is built with modules in the laboratory. The prototype is composed of discrete components in this experiment [Further step is to realize this prototype based on system-on-package (SOP)]. Each phase leg of the cascaded inverter consists of four independent modules. The gate signals are produced by a CPLD of EPM7064SLC44 embedded in the module. Fig.10 illustrates a CPLD based controller structure under the distributed control scheme. As seen, "count_updn" sub cell is tasked to generate the symmetrical triangular carrier; "spwm" sub cell storages the reference signal information and compares the sinusoidal reference with the triangular carrier to obtain the PWM control signal and "dead" sub cell provides a dead band for the gate signal. In addition, simple protected function is also shown in Fig.10.

There is a significant input pin marked as "period" in Fig.10, from which the common synchronization signal can be received for synchronization between modules when this module is regarded as a slave one. Once this module is treated as a master one, the output pin marked as "period" of "count_updn" sub cell will be tasked to send out the common synchronization signal to other slave ones for synchronization.

Experimental results

In this experiment, the switching frequency is set to 3 kHz, the sinusoidal reference frequency is set to 50 Hz and the modulation index is set to 0.8. Fig.11 shows the synchronization performance of two modules using the above synchronization method. Fig.11a and Fig.11b illustrate the carrier phase signals and the gate PWM signals for two adjacent modules, respec-

tively. It can be seen that an approximate phase shift of 83 μs (i.e., a quarter of carrier period 333 μs) is between two modules, which is the proper theoretical phase shift. Fig.12a and Fig.12b show the phase voltage waveform and its FFT spectrum, respectively. Note that the first set of sideband harmonics is centered at the quadruple carrier frequency. It confirms the accuracy of double Fourier analysis and simulation investigation.

Fig.13 and Fig.14 show the synchronization performance when the carrier phase error and the reference phase error exist, respectively. These plots closely match those obtained from the simulation results of Fig.5 and Fig.7. It can be seen from all these figures that the low order harmonic components increase significantly when the synchronization error is large. Due to the measurement noise, though the low order harmonic components increase when the synchronization error is small, their magnitudes are very small and the experimental spectrums are similar to those under normal condition, so they are not shown in this paper.

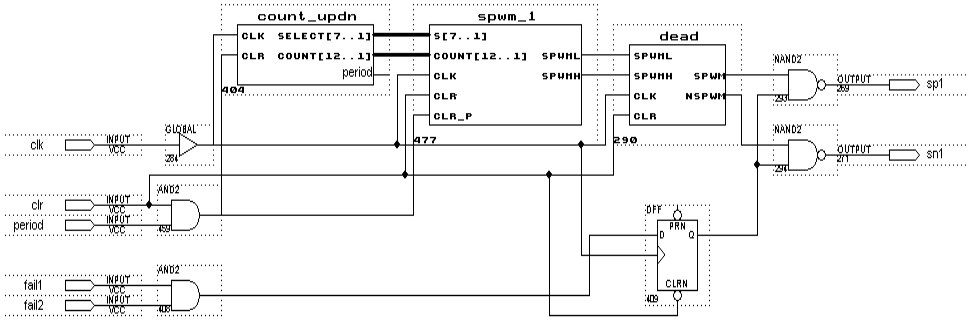
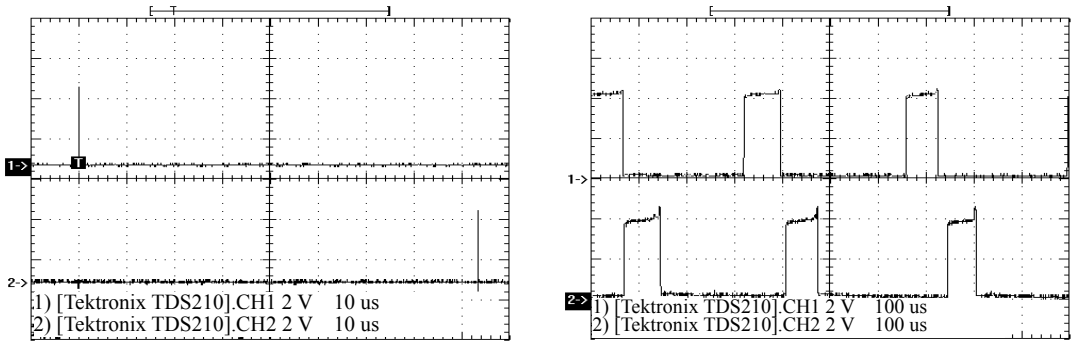
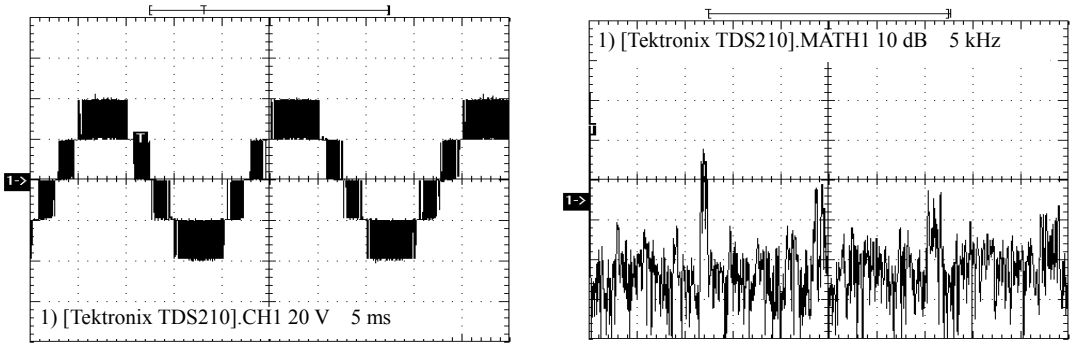


Fig.10 Control scheme of an integrated controller



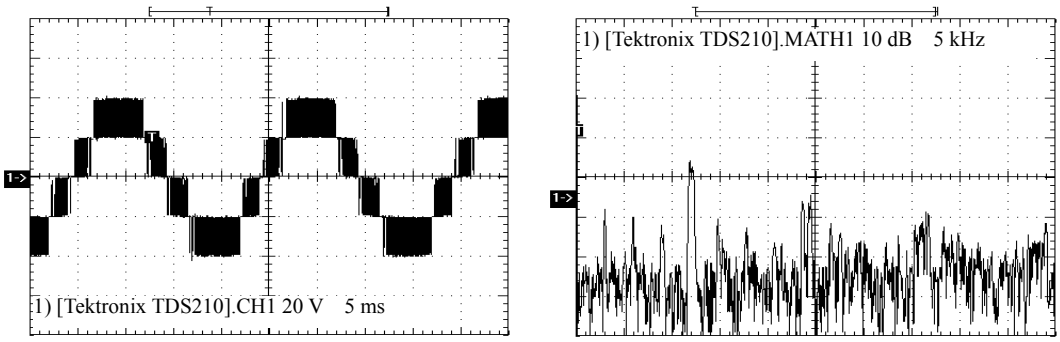
(a) (b)

Fig.11 Synchronization results of two adjacent modules
(a) Carrier phase signals of two adjacent modules; (b) PWM signals of the adjacent modules



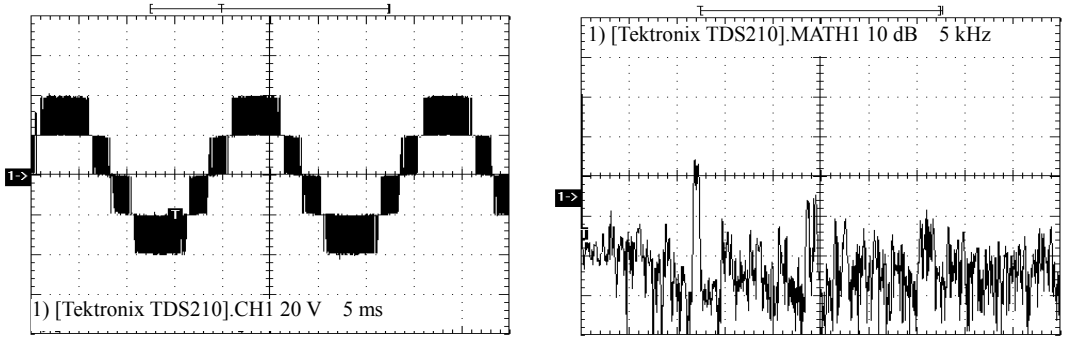
(a) (b)

Fig.12 Experimental results of the phase voltage in synchronization mode
(a) Phase voltage waveform; (b) FFT spectrum of the phase voltage



(a) (b)

Fig.13 Experimental results with carrier phase error being 5.55 μs
(a) Phase voltage waveform; (b) FFT spectrum of the phase voltage



(a) (b)

Fig.14 Experimental results with reference phase error being 333 μs
(a) Phase voltage waveform; (b) FFT spectrum of the phase voltage

CONCLUSION

The paper analyzes the synchronization performance when three kinds of synchronization errors exist by a three-phase five-level cascaded inverter built with integrated modules. Some conclusions can be derived from the analysis. First, both synchronization errors will lead to additional low order carrier sideband harmonics in the phase leg output voltage. Secondly, the carrier synchronization error affects the output voltage performance more significantly than the reference synchronization error. Thirdly, these low frequencies harmonic components produced by both synchronization errors cannot be cancelled in the *l-l* output voltage, except for the expected intrinsic cancellation of triple harmonics between the phase legs. These conclusions are valuable for the practical applications of PWM converters built with integrated modules by distributed control scheme.

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