Journal of Zhejiang University SCIENCE A
ISSN 1673-565X (Print); ISSN 1862-1775 (Online)
www.zju.edu.cn/jzus; www.springerlink.com
E-mail: jzus@zju.edu.cn

In-package P/G planes analysis and optimization based on transmission matrix method*

Yin-jun WANG†, Cheng ZHUO, Jun-yong DENG, Jin-fang ZHOU†‡, Kang-sheng CHEN

(*Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China*)

†E-mail: vividbubu@hotmail.com; Zhoujf@zju.edu.cn

Received Sept. 15, 2007; revision accepted Jan. 23, 2008

Abstract: Power integrity (PI) has become a limiting factor for the chip's overall performance, and how to place in-package decoupling capacitors to improve a chip's PI performance has become a hot issue. In this paper, we propose an improved transmission matrix method (TMM) for fast decoupling capacitance allocation. An irregular grid partition mechanism is proposed, which helps speed up the impedance computation and complies better with the irregular power/ground (P/G) plane or planes with many vias and decoupling capacitors. Furthermore, we also ameliorate the computation procedure of the impedance matrix whenever decoupling capacitors are inserted or removed at specific ports. With the fast computation of impedance change, in-package decoupling capacitor allocation is done with an efficient change based method in the frequency domain. Experimental results show that our approach can gain about 5× speedup compared with a general TMM, and is efficient in restraining the noise on the P/G plane.

Key words: Decoupling capacitor, Power/ground (P/G) planes, Simultaneous switching noise (SSN), Transmission matrix method (TMM), Irregular partition, Power integrity (PI)

doi:10.1631/jzus.A071489 **Document code:** A **CLC number:** TN402

INTRODUCTION

Power integrity (PI) has become a limiting factor for the overall performance of modern chip design due to the current surges caused by simultaneous switching noise (SSN). As an indispensable part of the power delivery system (PDS), the power/ground (P/G) planes provide coupling paths for large current flows. And a robust P/G plane design is crucial for meeting performance targets and guaranteeing reliable operations. To ensure the robustness of the design, it is essential to make an exact analysis of the noise on the P/G plane pairs and optimize the P/G planes design to mitigate the noise. Adding in-package decoupling capacitors is one of the most efficient ways of improving the in-package PI.

Many methods have been proposed for the analysis and optimization of P/G planes. A 3D full-wave field solver can provide a very accurate solution, but is too time and memory consuming (Fang *et al*., 1993). To improve the efficiency of full-wave simulators, other methods have been used such as multilevel Green's function interpolation method (MLGFIM) (Wang *et al*., 2004), precorrected fast Fourier transform (FFT) (Phillips and White, 1997) and sparse-matrix canonical grid (SMCG) (Li *et al*., 2001). But MLGFIM is used to extract the capacitances in RF ICs while precorrected FFT and SMCG are efficient only if the circuit traces are densely packed. The cavity resonator model is proposed in (Na *et al*., 2000). However, its restriction to very regular P/G planes limits its application to the initial design stage or to some specific cases. There also have been many works (Lee and Barber, 1995; Kim and Swaminathan, 2001; 2002; Wang *et al.*, 2006) aimed at speeding up the analysis of the P/G

‡ Corresponding author

* Project supported by the Ph.D Programs Foundation of Ministry of Education of China (No. 20060335065) and the Natural Science Foundation of Zhejiang Province, China (No. Y106513)

planes with an arbitrary structure. Wang *et al*.(2006) systematically combine the cavity model with the segmentation method. Lee and Barber (1995) and Kim and Swaminathan (2001; 2002) develop the transmission line method and the transmission matrix method (TMM), respectively. But all these three methods are restricted to segment partitioning with a regular shape.

In-package decoupling capacitor optimization is a nonlinearly constrained discrete optimization problem while most existing approaches are trial-and-error methods. The most comprehensive works on automatic in-package decoupling capacitor optimization are by Chen and He (2007) and Zheng *et al*.(2003). They use a macro-model based simulated annealing algorithm to decide the optimal value of decoupling capacitors at different locations to obtain the target impedances at chip I/O ports. MOR (model order reduction) technique (Zheng and Pileggi, 2002) is used when building packages' macro-models.

In high performance microprocessors, the package may have many vias, decoupling capacitors, irregular geometries and multiple plane layers. The complex structure and various border effects restrict the size of the segment in regular partition when discretizing the P/G planes. A small enough segment would guarantee the accuracy at the cost of memory and CPU time. In this paper we propose an irregular partition strategy in which the P/G planes can be partitioned into different rectangular shapes according to the vias, decoupling capacitors or other details of the structures. Such a strategy is more practical and efficient, because a larger segment can be used for non-critical regions and a smaller one for regions full of vias or decoupling capacitors. We integrate this strategy into TMM to analyze the multi-layered P/G planes with complex structures. Based on the improved TMM method, we have proposed a methodology for in-package decoupling capacitor optimization on a multi-layered P/G plane. Compared with previous work, our method can obtain more accurate results with less CPU runtime. The main contributions of this paper are summarized as follows:

(1) We propose an irregular partition strategy to divide the P/G planes. This strategy partitions the planes with different-sized segments depending on the specific structures or requirements.

(2) We apply the irregular partition strategy to the TMM method. Based on that, we simplify the computation procedure of TMM and give a fast flow for multi-layered P/G planes analysis.

(3) We use the improved TMM for fast decoupling capacitance allocation. A methodology to guide the decap optimization is also proposed. When decoupling capacitors are added or removed, we use a matrix refinement technique to speed up the transmission matrix update. Experimental results show that our methodology can optimize the target impedance very efficiently and accurately.

BACKGROUND

Since the P/G planes in the package and board can be represented as a cascade of unit cells, the TMM can be used to simulate arbitrarily shaped, electrically large structures efficiently. The response of the P/G planes at specific ports can be computed by multiplying the individual square matrices. For multi-layered P/G planes, each individual square matrix is based on a pair of P/G planes. In the TMM, the problem of obtaining the individual square matrices of a pair of P/G planes is tackled in the following two-step procedure (Kim and Swaminathan, 2001; 2002).

(1) The P/G plane pair is divided into unit cells with a lumped element model for each cell. Then the distributed network of RLCG elements can be generated from the spice model for the unit cells as shown in Fig.1. Either the T or Π equivalent circuit for the unit cells can be used.

(2) The transmission matrix for the distributed network of RLCG elements can be derived in terms of node voltages and port currents using Eq.(1) (Kim and Swaminathan, 2002):

$$\begin{bmatrix} \boldsymbol{V}_{\text{in}} \\ \boldsymbol{I}_{\text{in}} \end{bmatrix} = \boldsymbol{T} \begin{bmatrix} \boldsymbol{V}_{\text{out}} \\ \boldsymbol{I}_{\text{out}} \end{bmatrix}, \tag{1}$$

where

$$\boldsymbol{T} = \begin{bmatrix} \boldsymbol{T}_A & \boldsymbol{T}_B \\ \boldsymbol{T}_C & \boldsymbol{T}_D \end{bmatrix} \tag{2}$$

is the transmission matrix of Eq.(1), and is derived according to the definition of the transmission matrix.

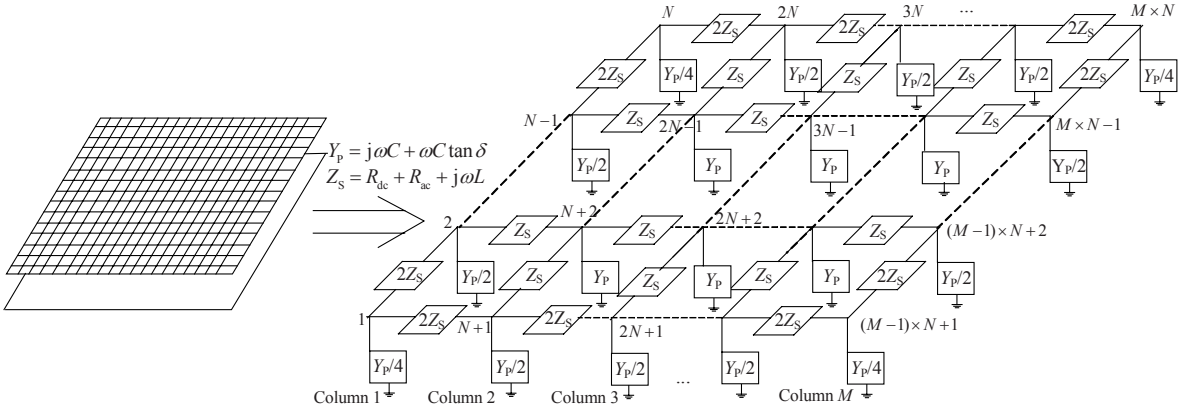


Fig.1 Equivalent circuit for a pair of P/G planes using ∏ model for unit cells

IRREGULAR PARTITION BASED TMM

Motivation of irregular partition

When using a regular partition strategy on a realistic package structure, the size of the regular segments must meet the requirements below: (1) Segments should be small enough so that different ports/vias/decoupling capacitors could be located at different segments; (2) For irregularly shaped P/G planes, the size of segments is limited by the small apertures, splits and flexural boundary.

Actually, for P/G planes, large segments would also work well for general parts of the planes without vias or decoupling capacitors, while small segments are necessary only for some specific parts of the planes with decoupling capacitors or apertures. Thus, a TMM based on irregular partition may make the partitioning procedure more suitable for realistic structures of packages. It makes finer partition only in specific parts of the planes with coarser partition in general parts.

Methodology of irregular partition based TMM for a pair of P/G planes

Fig.2 shows the irregular partition of a pair of P/G planes. On rectangular P/G planes there are ports and decoupling capacitors ("decap" for short) at different locations. The methodology of irregular partition for a single pair of P/G planes is as follows:

(1) Partition the planes according to the coordinates of decoupling capacitors and ports as shown in Fig.2a.

(2) Divide the remaining parts of the P/G planes as shown in Fig.2b. We should try to partition the remaining parts of the planes regularly and coarsely. In order to obtain good accuracy, the maximum size of unit cells must be 10 times less than the wavelength of the highest frequency of interest. It can be observed that the finer partition was only made around the decoupling capacitors and ports. This will make the calculating process more effective with slight accuracy loss.

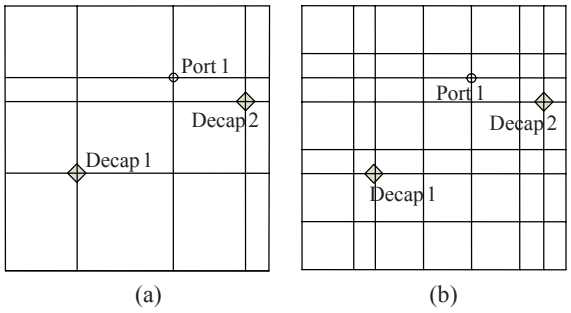
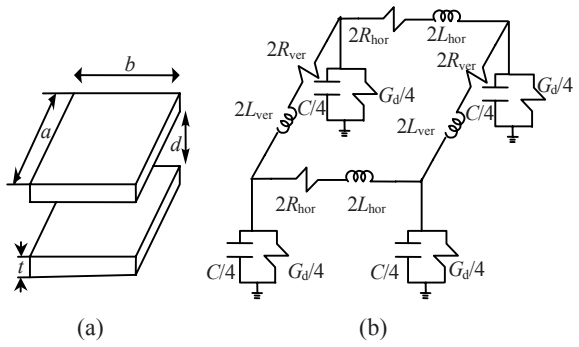


Fig.2 Idea of irregular partition
(a) Make nodes at specific locations; (b) Divide the remaining part of the package

Even though the unit cells after partition are not uniform any more, we can still use the SPICE model of unit cells similar to that in (Kim and Swaminathan, 2001; 2002) as shown in Fig.3. However, the equations for computing the parameters of the model must be modified correspondingly.

Parameters in Fig.3b can be computed as (Chen, 2001)

$$\begin{cases} C = \varepsilon_0 \varepsilon_r \dfrac{ab}{d}, \quad L_{ver} = \mu_0 d \dfrac{a}{b}, \quad R_{ver\,dc} = \dfrac{2}{\sigma_c t} \dfrac{a}{b}, \\ L_{hor} = \mu_0 d \dfrac{b}{a}, \quad R_{hor\,dc} = \dfrac{2}{\sigma_c t} \dfrac{b}{a}, \quad G_d = \omega C \tan\delta, \end{cases} \tag{3}$$



(a) (b)

Fig.3 Unit cell and equivalent circuit (∏ model)
(a) Unit cell; (b) Equivalent circuit of unit cells

where ε_0 and μ_0 are the permittivity and permeability of free space, respectively; ε_r is the relative permittivity of the dielectric and σ_c is the metal conductivity. $R_{\text{ver dc}}$ and $R_{\text{hor dc}}$ are resistances of steady DC current in the vertical and lateral directions respectively in the quasi-static model. L_{ver} and L_{hor} are inductances in the vertical and lateral directions respectively in the quasi-static model.

R_{ac} accounts for the skin effect on both conductors. The equations to compute R_{ac} are

$$R_{\text{ver ac}} = 2\sqrt{\frac{\pi f \mu_0}{\sigma_c}}\frac{a}{b},\quad R_{\text{hor ac}} = 2\sqrt{\frac{\pi f \mu_0}{\sigma_c}}\frac{b}{a}, \qquad (4)$$

where $R_{\text{ver ac}}$ and $R_{\text{hor ac}}$ represent R_{ac} in the vertical and lateral directions, respectively.

Now that all the parameters of a single unit cell have been derived, we can obtain the equivalent distributed network of the whole P/G plane by combining the equivalent distributed RLCG circuits of all the unit's irregularly partitioned cells according to the principles of getting RLCG series-parallel circuits. Then the transmission matrix of the P/G plane pair can be obtained.

Methodology of irregular partition based TMM for multi-layered P/G planes

We now analyze multi-layered P/G planes based on the method for a single pair of P/G planes. It is important to note that when partitioning each plane pair must have the same number of rows and columns of nodes. Only in this way can we guarantee the cascade of each pair of P/G planes when creating the overall transmission matrix. Because of different specifications, the partition of each plane pair is different. Thus it may be necessary to modify the partition of some P/G plane pairs to fit the demand mentioned above.

The methodology of irregular partition for multi-layered P/G planes is as follows:

Step 1: According to the specification for each plane pair, partition each pair of P/G planes using the irregular partition methodology mentioned above. Assume there are n pairs of P/G planes. M_i and N_i are the number of rows and columns of nodes of the ith pair of P/G planes after partition, respectively. Each plane pair is divided into $(M_1-1)\times(N_1-1)$, $(M_2-1)\times(N_2-1)$, …, $(M_n-1)\times(N_n-1)$ unit cells, respectively.

Step 2: Modify the partition of each plane pair. The aim of modification is to divide each plane pair into $(M-1)\times(N-1)$ unit cells by increasing the number of rows and columns in the necessary plane pairs based on the partition in Step 1. Here, $M=\max(M_1, M_2, \ldots, M_n)$ and $N=\max(N_1, N_2, \ldots, N_n)$. Take the ith pair of P/G planes, which is divided into $(M_i-1)\times(N_i-1)$ unit cells in Step 1, as an example. Assuming $M_i<M$ and $N_i<N$, we should insert $M-M_i$ rows and $N-N_i$ columns into the partition result. As an increasing number of rows and columns mean finer partition and higher accuracy, we can insert the extra partition lines at any part of the plane pair. After modification, the transmission matrices of each P/G plane pair, which are of the same size of $(2MN)\times(2MN)$, can be generated.

Step 3: Construct the transmission matrices for vias and decoupling capacitors. The transmission matrices for them are $(2MN)\times(2MN)$ matrices (Kim and Swaminathan, 2002).

Step 4: The overall transmission matrix of the multi-layered P/G planes can be obtained by multiplying the individual matrix. It is a $(2MN)\times(2MN)$ matrix.

Though the number of nodes for some plane pairs may be increased in Step 2, the dimension of the overall transmission matrix of the multi-layered P/G planes derived by irregular partition is still much smaller than that of regular partition. This is because regular partition generates more nodes than irregular partition in each plane pair. As the dimension of the package increases, the efficiency advantage of irregular partition based TMM will be more obvious.

TMM BASED IN-PACKAGE DECOUPLING CAPACITOR OPTIMIZATION

Incremental update of impedance matrix

The insertion or removal of decoupling capacitors will change the impedance matrix and further affect the in-package noise. Thus, the impedance matrix of the planes is updated corresponding to the decoupling capacitors allocation. Here we use a matrix refinement technique to speed up the impedance matrix update when decoupling capacitors are added or removed.

Fig.4 shows the realistic structure of n multi-layered P/G plane pairs. The power planes and ground planes are connected through vertical vias, respectively. While the bottom plane pair is connected to the PCB by balls, and the chips and decoupling capacitors are put on V_1 and G_1, respectively (Chen and He, 2007). SSN shows up when a rapid switching of current occurs in inductive parasitic circuit elements of the P/G planes (Lee *et al*., 2005). As the bottom of the package connects to the PCB, we consider these I/Os connecting the package to the PCB in the bottom plane of the package to be the inductors of SSN. Therefore, in our methodology for optimization, the observation ports are the ports on chips and the excitation ports of SSN are I/Os on the bottom plane pair.

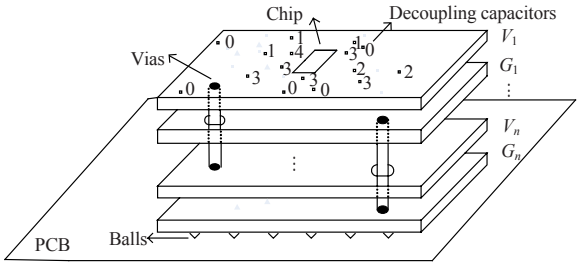


Fig.4 Structure of multi-layered power distribution

According to the realistic structure of P/G planes shown in Fig.4, the overall transmission matrix for the structure to be optimized can be expressed as follows (Kim and Swaminathan, 2002):

$$\boldsymbol{T}_m=\begin{bmatrix}\boldsymbol{A}_m & \boldsymbol{B}_m\\ \boldsymbol{C}_m & \boldsymbol{D}_m\end{bmatrix}=\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p+\boldsymbol{C}_{\text{cap}} & \boldsymbol{I}\end{bmatrix}_1\begin{bmatrix}\boldsymbol{I} & \boldsymbol{B}_{\text{via}}\\ \boldsymbol{0} & \boldsymbol{I}\end{bmatrix}_{1,2}\cdot\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p & \boldsymbol{I}\end{bmatrix}_2\cdots\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p & \boldsymbol{I}\end{bmatrix}_n, \tag{5}$$

where n represents the number of P/G plane pairs, $\boldsymbol{C}_p$ represents the "C" part of the transmission matrix of the P/G planes without decoupling capacitors.

The impedance matrix can be derived using the relation between the transmission matrix and the impedance matrix (Kim and Swaminathan, 2002):

$$\boldsymbol{Z}_{\boldsymbol{B}}=\boldsymbol{Z}_{\boldsymbol{C}}=\boldsymbol{C}_m^{-1}. \tag{6}$$

For a chip with N ports, the effective impedance of port i can be defined as (Zheng *et al*., 2003)

$$\left|Z_i(f)\right|_{\text{eff}}=\sum_{j=1}^{N}\left|Z_{ij}(f)\right|W_j, \tag{7}$$

where W_j denotes the relative switching intensity of partition j (Zheng *et al*., 2003). Z_{ij} is the transfer impedance from port j to port i. Our objective is to restrain the SSN on the observation ports by optimizing Z_{ij}. To achieve that, we need to obtain the transfer impedance matrix $\boldsymbol{Z}_{\boldsymbol{B}}$ first.

From Eq.(5),

$$\begin{aligned}\boldsymbol{T}_m=&\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p & \boldsymbol{I}\end{bmatrix}_1\begin{bmatrix}\boldsymbol{I} & \boldsymbol{B}_{\text{via}}\\ \boldsymbol{0} & \boldsymbol{I}\end{bmatrix}_{1,2}\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p & \boldsymbol{I}\end{bmatrix}_2\cdots\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p & \boldsymbol{I}\end{bmatrix}_n\\ &+\begin{bmatrix}\boldsymbol{0} & \boldsymbol{0}\\ \boldsymbol{C}_{\text{cap}} & \boldsymbol{0}\end{bmatrix}_1\begin{bmatrix}\boldsymbol{I} & \boldsymbol{B}_{\text{via}}\\ \boldsymbol{0} & \boldsymbol{I}\end{bmatrix}_{1,2}\begin{bmatrix}\boldsymbol{0} & \boldsymbol{0}\\ \boldsymbol{C}_{\text{cap}} & \boldsymbol{0}\end{bmatrix}_2\cdots\begin{bmatrix}\boldsymbol{I} & \boldsymbol{0}\\ \boldsymbol{C}_p & \boldsymbol{I}\end{bmatrix}_n\\ =&\begin{bmatrix}\boldsymbol{A}_{ma} & \boldsymbol{B}_{ma}\\ \boldsymbol{C}_{ma} & \boldsymbol{D}_{ma}\end{bmatrix}+\begin{bmatrix}\boldsymbol{0} & \boldsymbol{0}\\ \boldsymbol{C}_{\text{cap}} & \boldsymbol{0}\end{bmatrix}_1\begin{bmatrix}\boldsymbol{A}_{mb} & \boldsymbol{B}_{mb}\\ \boldsymbol{C}_{mb} & \boldsymbol{D}_{mb}\end{bmatrix}\\ =&\begin{bmatrix}\boldsymbol{A}_{ma} & \boldsymbol{B}_{ma}\\ \boldsymbol{C}_{ma}+\boldsymbol{C}_{\text{cap}}\boldsymbol{A}_{mb} & \boldsymbol{D}_{ma}+\boldsymbol{C}_{\text{cap}}\boldsymbol{B}_{mb}\end{bmatrix}.\end{aligned} \tag{8}$$

From Eqs.(5), (6) and (8), we have

$$\boldsymbol{Z}_{\boldsymbol{B}}=\boldsymbol{C}_m^{-1}=\left(\boldsymbol{C}_{ma}+\boldsymbol{C}_{\text{cap}}\boldsymbol{A}_{mb}\right)^{-1}. \tag{9}$$

From Eq.(8), $\boldsymbol{C}_{ma}$ and $\boldsymbol{A}_{mb}$ can be derived before inserting any decoupling capacitor. In other words, $\boldsymbol{Z}_{\boldsymbol{B}}$ only depends on $\boldsymbol{C}_{\text{cap}}$. Without computing $\boldsymbol{C}_{ma}$ and $\boldsymbol{A}_{mb}$ in each iterative process, the computation efficiency could be improved.

Methodology for decoupling capacitor optimization

In many earlier works, the optimization method can only optimize one port's noise every time. In this paper, we develop the methodology in (Zheng *et al*.,

2003) to optimize noises of several ports simultaneously. We formulate the following in-package decoupling capacitor optimization problem: given a set of decoupling capacitors and some user-defined target impedances at the specific on-chip ports, find the set of decoupling capacitors with the lowest possible cost. The allocation of decoupling capacitors should ensure that the peak of impedances is below the target impedances. Expressed mathematically, the formulation can be written as

$$\min \sum_{i=1}^{n} P_i \text{ subject to } \max(Z_{\text{peak}}^{j_k}) \le Z_{\text{target},k}, \forall k = 1,2,\ldots,m, \tag{10}$$

where n is the number of the decoupling capacitor ports and P_i is the price of the decoupling capacitor at port i. $Z_{\text{peak}}^{j_k}$ is the peak of the effective impedance at port j_k as defined in (Zheng *et al*., 2003); m is the number of observation ports; $Z_{\text{target},k}$ is the target impedance at port j_k.

Four common types of surface mount package decoupling capacitors are used for the analysis here (Zheng *et al*., 2003; Na *et al*., 2004).

We combined the TMM with simulated annealing which is a stochastic optimization procedure accommodating the open cost function to solve the problem above (Zheng *et al*., 2003). The cost function for this problem is

$$W_P \sum_{i=1}^{n} P_i + \sum_{k=1}^{m} W_{Z,k}[\max(Z_{\text{peak}}^{j_k}) - Z_{\text{target},k}]. \tag{11}$$

In Eq.(11), W_P and $W_{Z,k}$ are the adjusting weights for decoupling capacitor cost and target impedances, respectively. To enforce the requirements of target impedances during the annealing process, $W_{Z,k}$ increases dynamically when $Z_{\text{peak}}^{j_k}$ is greater than the target impedance and is zero when the impedance requirement is satisfied.

The flow for iterative decoupling optimization is shown in Fig.5.

EXPERIMENTAL RESULTS

We implement the algorithms in Matlab 6.1 and conduct experiments on a 3.2 GHz Pentium IV Windows Server with 3.2 G RAM.

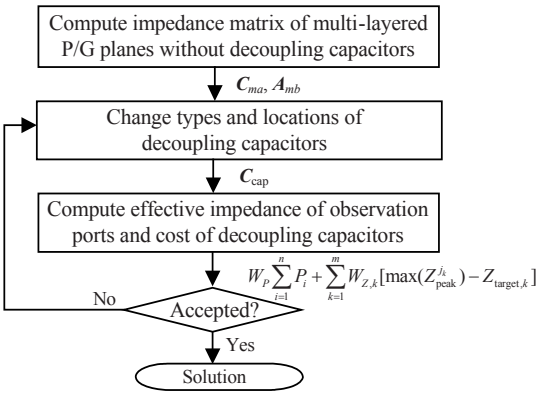


Fig.5 Flow of decoupling capacitor optimization

Accuracy and efficiency of irregular partition based TMM

1. Test structure: a pair of regular planes

To check the accuracy of irregular partition based TMM, the results have been compared with a technique based on the analytical solution (Na *et al*., 2000) and the regular partition based TMM. The test structure is a plane pair having dimensions of 62.8000 mm×62.8000 mm with a 25.12 μm thick FR4 dielectric, and the relative permittivity ε_r=4. The conductor planes are made of copper (σ_c=5.8×10^7 S/m) with a thickness of 30.144 μm . The excitation point (Port 1) is located at (x=0, y=3.7680 mm) and the observation point (Port 2) is at (x=30.1440 mm, y=30.1440 mm). For this test case, the dielectric loss was assumed to be negligible. In regular partition based TMM, using a unit cell size of 2.5120 mm×2.5120 mm, the rectangular plane was divided into 625 cells. The propagating modes were set to m=n=100 in the analytical solution in (Na *et al*., 2000). Figs.6a and 6b show the regular partition and irregular partition of the P/G plane pair, respectively. As shown in Fig.7, the irregular partition based method showed good agreement with the regular partition based method and the analytical solution.

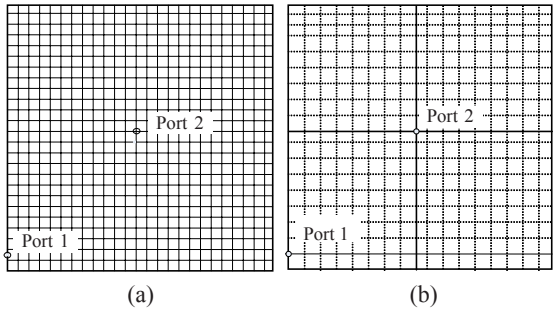


Fig.6 Regular partitioning (a) and irregular partitioning (b) of the P/G plane pair

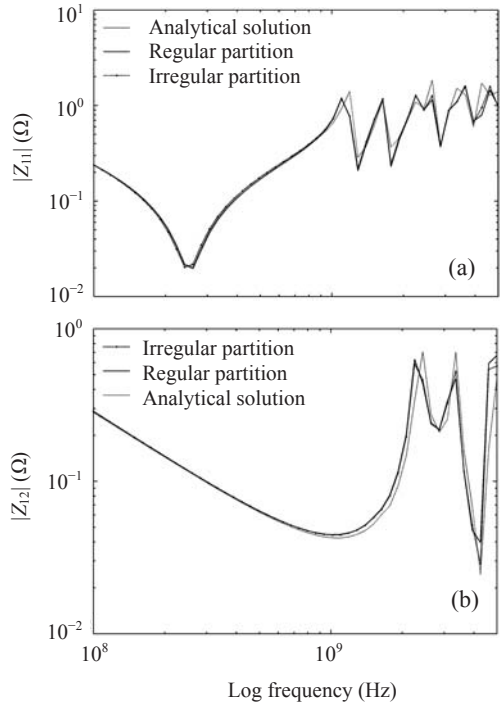


Fig.7 Self impedance (Z_{11}) (a) and transfer impedance (Z_{12}) (b) of a pair of P/G planes

2. Efficiency of irregular partition based TMM

With the number of cells decreased, the runtime will be reduced, but the accuracy will be reduced too. Table 1 shows that irregular partition based TMM leads to much less runtime with slight accuracy loss. Using the same test structure as that in the above subsection, we partition the plane pairs irregularly in different maximal grid sizes. Table 1 compares the runtime and the results of computation. The spectrum here is from 1.0×10^8 to 2.5×10^9 Hz. From Table 1, we see that a speedup 5× can be obtained using irregular partition based TMM while the relative errors are below 10%.

Table 1 Efficiency and accuracy of the irregular partition based TMM

Maximal grid size (mm×mm)	Number of cells	Relative runtime (%)	Relative error Z_{11} (%)	Relative error Z_{12} (%)
2.5120×2.5120*	625	100	0	0
3.0144×3.0144	539	57.10	1.76	2.16
3.3158×3.3158	441	42.70	3.32	4.08
3.7680×3.7680	361	23.61	5.31	6.51
4.1950×4.1950	289	14.47	7.97	10.24

* Regular partition

3. Irregular partition based TMM for the analysis of multi-layered P/G planes

In the structure, the conductor planes stack up in the order $V_1/G_1/V_2$ as shown in Fig.4. Each plane pair is the same as that in the subsection "Test structure: a pair of regular planes". Port 1 is located at (2.5120 mm, 0) between planes V_1 and G_1; Port 2 is located at (15.0720 mm, 17.5840 mm) between planes V_2 and G_1. In the regular partition based method, we divide each P/G plane into 2.5120 mm×2.5120 mm unit cells. And there are 625 unit cells in each pair. In the irregular partition based method, we take the location of vias and ports into consideration. Then we make the maximal grid size to be 3.7680 mm×3.7680 mm. There are 306 segments in each pair after segment division. Fig.8 shows the comparison of impedances of this structure. It demonstrates that the solution of irregular partition based TMM matches well with that using the regular based method. Moreover, the irregular partition based TMM takes 156.2 s while the regular partition based TMM takes 1107.1 s.

Efficiency of decoupling capacitor optimization using irregular partition based TMM

The test structure for optimization consists of

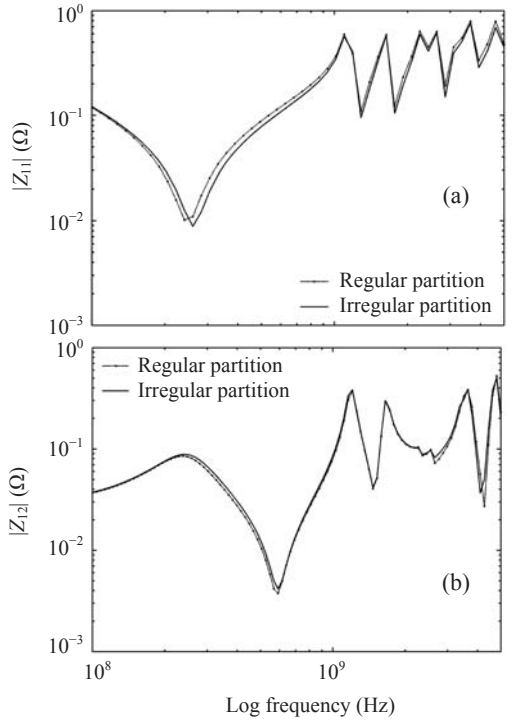


Fig.8 Self impedance (Z_{11}) (a) and transfer impedance (Z_{12}) (b) of multi-layered P/G planes

five 279.40 mm×228.60 mm rectangular pairs of P/G planes as shown in Fig.4, where the conductor planes stack up in the order $V_1/G_1/V_2/G_2/V_3$, with the FR4 dielectric ε_r=4.5. The dielectric thicknesses of V_1/G_1, V_2/G_2 and V_3/G_2 plane pairs are all 109.22 μm. And the dielectric thickness of V_2/G_1 and V_3/G_3 plane pairs are both 337.82 μm. The conductor planes are made of copper (σ_c=5.8×10^7 S/m) with a thickness of 30.144 μm, and the dielectric loss tangent $\tan\delta$=0.02 at 1 GHz. In our experiment we use the same decoupling capacitors as (Zheng *et al*., 2003), which are also summarized in Table 2. Here some numbers correlated with the quality are used to represent the price. The numbers are not the actual price. We pre-define 16 ports for decoupling capacitors insertion on the planes.

Table 2 Decoupling capacitors in our experiment*

Capacitor	ESC (nF)	ESR (Ω)	ESL (nH)	Price
C1	50	0.060	100	1
C2	100	0.060	100	2
C3	50	0.030	40	2
C4	100	0.040	40	4

* We use the same decoupling capacitors as (Zheng *et al*., 2003)

The target impedance to be restricted is Z_{eff}, which is the effective impedance at the on-chip port as defined in Eq.(7). Excitation points are located at the bottom plane pair connecting to the PCB board. In practice, when different types of decoupling capacitors work together, the frequency range of effectiveness is roughly 1 kHz to several hundred MHz. In this paper, the spectrum to be optimized is 10~200 MHz.

Fig.9 shows the optimization results of Port 1.

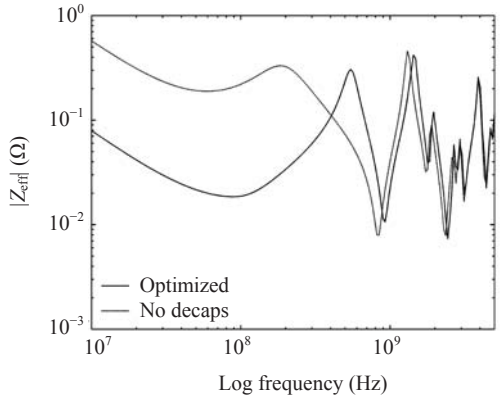


Fig.9 Optimization results of Port 1 after using our proposed method

Table 3 shows the optimization results of three ports. After optimization, 11 decoupling capacitors are needed to meet the SSN target. The locations of decoupling capacitors and ports are shown in Fig.4, in which the numbers beside the decoupling capacitors represent the types of decoupling capacitors as shown in Table 2. The 0 in Fig.4 denotes that no decoupling capacitor is inserted at the pre-defined ports.

Table 3 Optimization results of peak effective impedances at different ports

Port	Peak effective impedance (Ω)	
	Before optimization	After optimization
1	0.5733	0.3616
2	0.5737	0.3788
3	0.5738	0.3957

CONCLUSION

In this paper, an irregular partition scheme was proposed to make the TMM more efficient for realistic structures of P/G planes. Then, based on the improved TMM, we proposed a method for fast decoupling capacitance allocation, which can ensure the peak impedance below the target impedance with low cost. To make the TMM suitable for the iterative optimization process we also used a methodology for the impedance matrix update whenever decoupling capacitors at specific ports are inserted or removed. Experimental results show that the proposed methods have great efficiency and accuracy in practical applications.

References

Chen, J., He, L., 2007. Efficient in-package decoupling capacitor optimization for I/O power integrity. *IEEE Trans. on Computer-Aided Design Integr. Circuits Syst.*, **26**(4): 734-738. [doi:10.1109/TCAD.2006.888262]

Chen, K.S., 2001. Applied Electromagnetism. Zhejiang University Press, Hangzhou, p.76-109 (in Chinese).

Fang, J., Liu, Y., Chen, Y., Wu, Z., Agrawal, A., 1993. Modeling of power/ground plane noise in high speed digital electronics packaging. *Electr. Perform. Electr. Pack.*, p.206-208. [doi:10.1109/EPEP.1993.394553]

Kim, J.H., Swaminathan, M., 2001. Modeling of irregular shaped power distribution planes using transmission matrix method. *IEEE Trans. on Adv. Pack.*, **24**(3):334-336. [doi:10.1109/6040.938301]

Kim, J.H., Swaminathan, M., 2002. Modeling of multilayered power distribution planes using transmission matrix

method. *IEEE Trans. on Adv. Pack.*, **25**(2):189-199. [doi:10.1109/TADVP.2002.803258]

Lee, J., Dragos, M.H., Iyer, M.K., Kim, H., Kim, J., 2005. Analysis and suppression of SSN noise coupling between power/ground plane cavities through cutouts in multilayer packages and PCBs. *Adv. Pack.*, **28**(2):298-309. [doi:10.1109/TADVP.2005.846932]

Lee, K., Barber, A., 1995. Modeling and analysis of multichip module power supply planes. *Comp., Pack., Manufact. Technol.*, **23**(4):628-639. [doi:10.1109/96.475268]

Li, S.Q., Yu, Y.X., Chan, C.F., Chan, K.F., Tsang, L., 2001. A sparse-matrix/canonical grid method for analyzing densely packed interconnects. *IEEE Trans. on Microwave Theory Tech.*, **49**(7):1221-1228. [doi:10.1109/22.932239]

Na, N., Choi, J., Chun, S., Swaminathan, M., Srinivasan, J., 2000. Modeling and transient simulation of planes in electronic packages. *IEEE Trans. on Adv. Pack.*, **23**(3):340-352. [doi:10.1109/6040.861546]

Na, N.J., Budell, T., Chiu, C., Tremble, E., Wemple, I., 2004. The Effects of On-chip and Package Decoupling Capacitors and an Efficient ASIC Decoupling Methodology. Electronic Components and Technology Conf., p.556-567. [doi:10.1109/ECTC.2004.1319394]

Phillips, J.R., White, J.K., 1997. A precorrected-FFT method for electrostatic analysis of complicated 3-D structures. *IEEE Trans. on Computer-Aided Design Integr. Circuits Syst.*, **16**(10):1059-1072. [doi:10.1109/43.662670]

Wang, C., Mao, J.K., Selli, C., Luan, S.F., Zhang, L., Fan, J., Pommerenke, D.J., DuBroff, R.E., Drewniak, J.L., 2006. An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances. *IEEE Trans. on Adv. Pack.*, **29**(2):320-334. [doi:10.1109/TADVP.2006.871202]

Wang, H.G., Chan, C.H., Tsang, L., 2004. A New Multilevel Green's Function Interpolation Method for Large Scale EM Simulations in RF ICs. IEEE Antennas and Propagation Society Int. Symp., p.1182-1186. [doi:10.1109/APS.2004.1330394]

Zheng, H., Pileggi, L.T., 2002. Robust and Passive Model Order Reduction for Circuit Containing Susceptance Elements. IEEE Int. Conf. on Computer Aided Design, p.761-766.

Zheng, H., Krauter, B., Pileggi, L., 2003. On-Package Decoupling Optimization with Package Macromodels. Proc. IEEE Custom Integrated Circuits Conf., p.723-726.