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Design and FPGA verification of a novel reliable real-time data transfer system

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Abstract: Considering the increasing use of information technology with established standards, such as TCP/IP and XML in modern industrial automation, we present a high cost performance solution with FPGA (field programmable gate array) implementation of a novel reliable real-time data transfer system based on EPA (Ethernet for plant automation) protocol and IEEE 1588 standard. This combination can provide more predictable and real-time communication between automation equipments and precise synchronization between devices. The designed EPA system has been verified on Xilinx Spartan3 XC3S1500 and it consumed 75% of the total slices. The experimental results show that the novel industrial control system achieves high synchronization precision and provides a 1.59-μs standard deviation between the master device and the slave ones. Such a real-time data transfer system is an excellent candidate for automation equipments which require precise synchronization based on Ethernet at a comparatively low price.

Key words: Ethernet for plant automation (EPA), IEEE 1588, Precise synchronization, Real-time data transfer
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INTRODUCTION

Reliable real-time data transfer communication is an important issue in industrial automation. Several field buses, such as CAN (controller area network), Profibus and so on are used in industrial automation control systems. Among them, CAN bus, which has high reliability and good performance, is widely used in automobile industry, robot, building automation, vehicle and space engines, etc. However, its speed (1 Mbps for a length of 40 m) is not high enough to work properly for data transferring in the automation environment. Ethernet technology supports most of the network protocols such as TCP/IP, SMTP. The combination of Ethernet and Fieldbus is the future of industry automation (Chen *et al.*, 2007). Some researchers analyzed Fieldbus based on Ethernet (Pang *et al*., 2007; Dopatka and Wismuller, 2007). Xu and Fang (2005) adopted Ethernet to build Profibus Fieldbus, and showed that the communication speed could reach 12 Mbps when communicating with devices (Profibus slaves) at the lower layer and realize 10/100 M self-adapting communication. However, this achievement always needs to integrate an additional Ethernet interface, which complicates the system. PROFInet-IRT has a strict definition and good performance. This bus performs well in a high-speed data transfer communication system. Nevertheless, the establishment price is comparatively high since it needs ASIC (application specific integrated circuit) for handling node synchronization and cycle subdivision as well as an intelligent 2- or 4-port switch (Paula, 2005). Compared to the conventional Fieldbus, Ethernet PowerLink (EPL) is a new solution with an outstanding real-time performance. Limal *et al.*(2007) validated the medium redundancy management of EPL.

In this paper, we present another method using EPA (Ethernet for plant automation) and IEEE 1588 to realize real-time performance based on a normal

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Ethernet. EPA supports a distributed control system with a cycle being composed of only two main phases, which is simpler for scheduling compared to the three main phases of EPL. EPA can provide good scheduling service, support precise synchronization by employing PTP (precision time protocol), and meet the requirement of a real-time application. We propose a new design method to realize the network layer, transport layer, and data link layer of EPA using Verilog HDL (IEEE Std 1364, 2006) and adopt IEEE 1588 to guarantee the synchronization precision of the whole network. The system is verified on FPGA (field programmable gate array) by employing a normal Ethernet card and the results show that it provides a 1.59-μs synchronization precision. This high cost performance solution can adequately satisfy the demands of industrial plant automation.

SYSTEM OVERVIEW, DESIGN AND FPGA IMPLEMENTATION

Overview of the EPA network control system

EPA is a new real-time industrial Ethernet-based protocol. It can be utilized to link up all equipments for cooperation of industrial measurement and control (Feng *et al*., 2003; Chu, 2006). The EPA protocol data are packed using the UDP (user datagram protocol) protocol. To improve the real-time performance of the communication system, a schedule entity called 'communication schedule management entity' (CSME for short) is added between the network layer and the data link layer to cope with the uncertainness aroused by CSMA/CD and BEB (binary exponential backoff) algorithms in traditional Ethernet. So it can provide data determination service for industrial Ethernet, and the CSME is what we have employed to provide a real-time system based on a normal Ethernet.

Communication between EPA field devices is processed on schedule. The time needed to accomplish a communication cycle is called a 'poll period', which can be divided into periodic information transmission and non-periodic information transmission (Fig.1). In terms of configuration, the periodic packets (relevant to process parameters, such as measurement and control data, which need to be transmitted periodically in the control loop) would be sent at a fixed time point, while the non-periodic packets would be sent according to their priorities. The scheduling technique mentioned above is based on precise time synchronization between different devices.

Introduction of IEEE 1588

IEEE 1588 is a protocol to synchronize independent clocks running on separate nodes of a distributed measurement and control system to a high degree of accuracy and precision. The time information is transferred through four kinds of packets, i.e., Sync, Follow_up, Delay_Resp, and Delay_Req, as shown in Fig.2.

First, the master clock (M) sends the Sync message to Ethernet and then the Follow_up message to record the actual sent time of the Sync message, since Sync is packed in the transfer layer and cannot contain its real sent time. The slave clock (S) then receives the Sync message and gets its arrival time

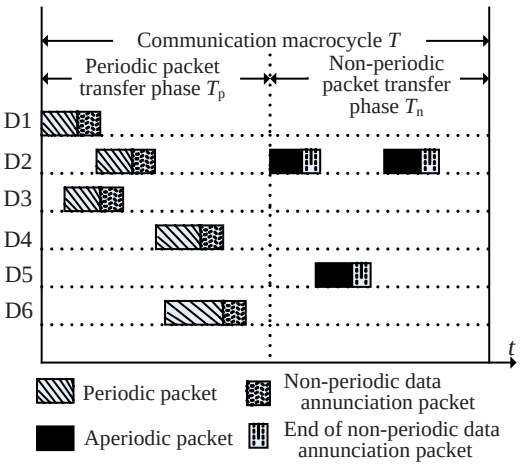

Fig.1 Time-sharing communication scheduling of the EPA network control system

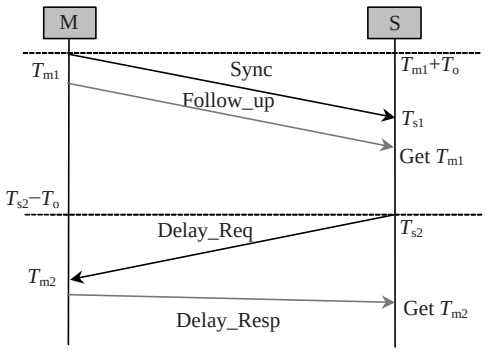

Fig.2 Delay time diagram between the master (M) and the slave (S) devices

T_{s1}. By unpacking the Follow_up message, S gets the sent time T_{m1} of the Sync message, and then sends the Delay_Req message at T_{s2} to Ethernet to synchronize itself to M. M then records the arrival time T_{m2} of the Delay_Req message, packs the time information in the Delay_Resp message, and resends this packet to Ethernet. Thus S gets T_{m2}. Assume the one_way_ delay between M and S is T_d and the time offset of S to M is T_o, then

$$T_{s1}=T_{m1}+T_d+T_o, \quad (1)$$

$$T_{m2}=T_{s2}+T_d-T_o. \quad (2)$$

From Eqs.(1) and (2), we can get T_o as follows:

$$T_o=[(T_{s1}-T_{m1})+(T_{s2}-T_{m2})]/2. \quad (3)$$

Thus S can adjust its clock according to that of M.

Design of the whole system

Since our objective is to provide a high cost performance solution and make sure the system is compatible with the current industrial system as much as possible, we adopt a normal Ethernet card instead of some PTP transceivers such as DP83640 from NI Corp. All modules are presented in Fig.3. The ARP module provides the address resolution protocol. The PTP module provides precise time synchronization of the whole network. The CSME module realizes the main EPA scheduling function. The ICMP (Internet control message protocol) is used to identify whether a requested service is available or a host or router can be reached (Wikipedia, http://en.wikipedia.org/wiki/Internet_Control_Message_Protocol). Pack and Unpack modules pack all the packets that need to be sent to the network and unpack those fetched from Ethernet. The NicIF module offers a communication interface between the system and the Ethernet card—AX88796L provided by ASIX Corp. The HostIf provides a user interface. The Global REG module is used to manage the register's reading and writing functions. Tx/RxMem is a memory management module. The worldwide popular WISHBONE bus is utilized to communicate between different modules since it is a free bus and can be easily implemented. Since both the host interface and the Ethernet card interface have access to the WISHBONE bus, we configure the host interface a higher access priority considering the user's specified interface timing requirements when both the HostIf and the NicIF want to communicate with the same slave.

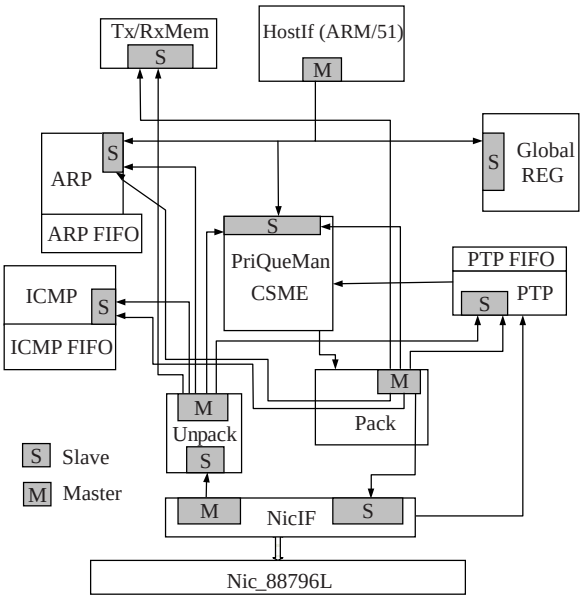

Fig.3 System architecture of Ethernet for plant automation

Scheduling of the whole system is controlled by the CSME module. All packets that need to be sent to Ethernet, such as ARP, PTP, ICMP and so on, should first be transferred to the CSME module and accept its scheduling. The CSME module manages these packets sending requests and informs the Pack module to pack them at proper time points. To simplify communications between the CSME module and the Pack module, all the packets that need to be sent in the CSME module should follow the routine as follows: first, write the packet information which includes data source and storage information to a register; secondly, notify the Pack module by interruption. The Pack module then uses its WISHBONE master interface to fetch more information about this interruption from the CSME module and packs the data according to a certain protocol.

In our system architecture, real-time transfer performance can be improved by implementing the CSME before IP packing and after unpacking. This change can simplify the system implementation and reduce the internal transfer time of the packets, and thus improve scheduling efficiency.

The basis of all the scheduling above is precise time, thus it is very important to choose a good master clock and achieve a high synchronization precision. The clock priority is a key factor in determining which device is the master clock. We provide a configurable register, which can prevent the device in an adverse environment from declaring itself the master device, to determine the clock priority. In addition, this modification can reduce the design complexity and power dissipation. However, as for devices with the same priority, the device with the smallest number of the lowest 8 bits of its IP address has the highest priority, and it turns to be the master clock. The slave clock should then calculate its offset time from the master clock and modify this counting frequency by increasing the counting period if its clock time is ahead of the master's and decreasing it otherwise. The PTP module also provides 1 ms enable signal to the CSME module for packet scheduling since the whole scheduling is executed by the CSME based on precise time calculation.

FPGA implementation

The system is implemented using Xilinx Spartan3 family XC3S1500-4-fg676. Fig.4 presents the layout of the whole system. The utilization summary is presented in Table 1.

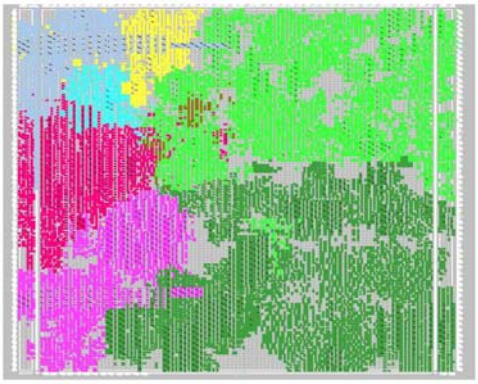

Fig.4 Integrated layout of the EPA system

Table 1 Utilization result summary of the system

Parameter	Value	Utilization
Number of slices	9948	75%
Number of slice flip flops	7305	27%
Number of 4-input LUTs	16809	63%
Number of RAM16s	8	25%
Minimum period	20.959 ns	

Our system consumes 75% of the whole resource. The minimum period is 20.959 ns, which satisfies the demands of industrial control systems. For comparison, we also estimated the ASIC area and timing based on SMIC 0.18-μm technology. The critical path delay is 14.27 ns and the chip area contains 230k gates, which is much smaller than FPGA's.

FPGA VERIFICATION AND DISCUSSION

The system has two interfaces, i.e., the host interface supporting ARM7 or MCS51 series and the network interface supporting the normal network interface card such as RealTek and AX88796 series. The FPGA verification is based on the AX88796L network interface card, which is widely used by industry automation plants. Fig.5 demonstrates our test system. Devices 1 and 2 have almost the same configuration except for IP and MAC address.

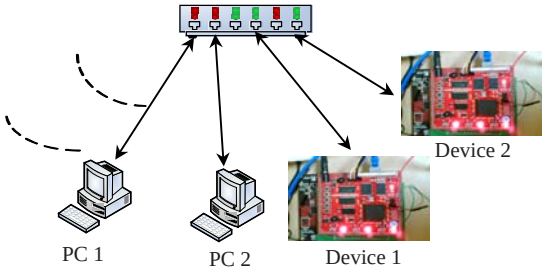

Fig.5 Test system of the Ethernet for plant automation

In this experiment, we used a broadcast packet sent by the PC to both Device 1 and Device 2. When the devices got the test packet, they packed the arrival time information in a response packet and resent it to the PC, thus the time information could be obtained by unpacking the response packet. EPA test software was developed to control and verify the whole test system. In this study, we had monitored the whole system running continuously for 20 d and found it worked well and no packet was discarded, missed or resent. To evaluate the synchronization precision, we tracked 1184 broadcast test packets and recorded each arrival time of the two devices. The time deviation between the master clock and the slave clock is sketched using Matlab as shown in Fig.6.

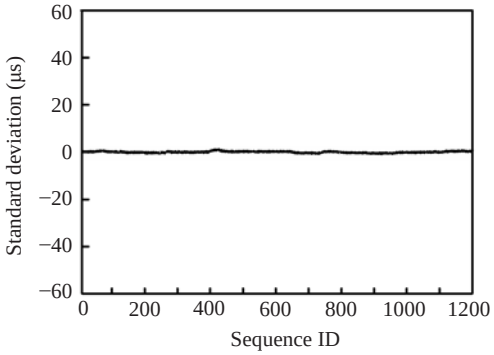

Fig.6 Time deviation between the master clock and the slave clock

The average time difference between two devices is 0.469 μs, the maximum deviation between the master and the slave is 3.721 μs, and the minimum is −3.694 μs. This result indicates that the deviation between the master and the slave is very small and the time difference decreases to microsecond level. The standard deviation σ is calculated to evaluate the deviation:

$$\sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(X_i - \bar{X})^2}. \quad (4)$$

In our experiment σ=1.59×10^{-6}, which shows a 1.59-μs standard deviation. Therefore, our EPA system can provide microsecond level synchronization precision and thus adequately satisfies the demands of industry automation equipments.

CONCLUSION AND FUTURE WORK

This paper presents the design and implementation of a novel reliable real-time data transfer system based on EPA protocol and PTP protocol. This new industrial control system meets the demands of deterministic communication based on Ethernet at a competitive price. FPGA verification results indicate that our design can provide a stable and effective communication between different devices. The synchronization precision between automation equipments can achieve a 1.59-μs standard deviation, which satisfies the requirement of an industrial Ethernet.

Our future work emphasizes on improving synchronization precision between devices and implementing the ASIC chip which can be used conveniently in industrial field automation plants. The ASIC chip has been taped out and is being manufactured using SMIC 0.18-μm fabrication technology.

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