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Performance improvement of complementary feeders using static transfer switch system

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Abstract: The performance of complementary feeders, running in parallel, can be significantly improved by installing static transfer switches (STSs) at critical locations. We develop the STS control logic, which transfers the critical load from the preferred feeder to the alternate feeder when a voltage sag or a fault occurs on the preferred feeder. A forced commutation technique is proposed and implemented to turn off the preferred feeders' thyristor, thus avoiding cross current to flow and minimizing the transfer time. Simulation results show that the forced commutation technique is more effective as compared to the recently proposed time delay technique for STS operation. Two different feeders, namely New Exchange, the preferred feeder, and Sector I-10/2, the alternate feeder of Islamabad Electric Supply COmpany (IESCO), Pakistan, have been selected for case studies. The software PSCAD/EMTDC professional package has been used for simulation.

Key words: Complementary feeder, Cross current, Static transfer switch (STS), Sensitive load, Voltage sag, PSCAD/EMTDC
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INTRODUCTION

In the era of deregulation, it is crucial for utilities to keep their consumers satisfied (Brown and Ochoa, 2000). It is important that distribution feeders meet their best performance parameters such as uninterruptible power supply and elimination of voltage sag or swell. However, in most of the developing countries, electric power distribution networks (EPDNs) are facing quite a few operating problems, including violation of voltage limits, unscheduled power interruptions, poor power quality and reliability. These problems in EPDNs cause financial loss to consumers in terms of industrial production, poor quality of the finished products, and failure to meet the production targets. As a result, the cost of interruption becomes quite high when these indirect losses to the consumers are also accounted for. It has been observed that most of the distribution feeders in the state-owned utilities in Pakistan are 10 times longer than their permissible length. As a distribution feeder becomes lengthy, the number of consumers connected to the feeder also increases. All this expansion of the distribution feeder, to meet the load growth, is made without increasing the capacity of the equipment at the substation or the conductor size for the feeder. Hence the overall impact of these factors is that the distribution feeders become overloaded and unable to meet the best performance parameters. In some service areas, different distribution feeders either overlap or run side by side in the densely populated urban areas. Such a kind of scenario is common in the industrial estates having multiple distribution feeders running side by side to feed the industrial, commercial and residential load in the urban areas. In such situations, it has been observed that among the parallel feeders, a particular distribution feeder is overloaded during certain hours of the day while a nearby feeder is lightly loaded at the same time. When a feeder is overloaded, it draws more current than its rating capacity, and hence voltage drops as well as power losses go beyond the permissible limits. If voltage drops are more than the permissible limits (±5%), then at different nodes of

the feeder the magnitude of voltage limits is violated and sensitive equipments may experience voltage sag or interruption. Such cases have been identified by the authors for the daily load curve and weekly load curve of the distribution feeder. The authors have taken this disparity and problematic situation as an opportunity to improve the performance of the complementary feeders in these service areas of an EPDN. Under this scenario, feeder performance can be improved for the overloaded feeder by transferring load from the overloaded feeder to the nearby lightly loaded feeder, and vice versa during particular hours of the day or particular days of the week. This approach will postpone investment in other alternatives to cater for the load growth on the overloaded feeder by devising the load transfer strategy on the nearby lightly loaded feeder. A lightly loaded feeder can serve some load of the heavily loaded feeder through load transfer using a static transfer switch (STS). The STS has low operational and maintenance cost. This approach avoids investment in other methods to improve the quality and reliability of power of the overloaded feeder. The other alternatives can be, for example, laying down of an express feeder, installation of a dispersed generation (DG), and building up of a new substation. But all these alternatives are quite expensive and are not cost effective for feeding of only peak hour load of the overloaded feeder.

Schwartzenberg and de Doncker (1995) proposed a three-phase medium voltage static transfer switch (MVSTS) system to be used as a bypass switch in normal and emergency configurations of sensitive loads. They have shown the results for this relatively simple configuration. It needs to be investigated for complex configurations and duty cycle requirements. Mokhtari *et al.*(2001b; 2002) analyzed the STS performance in terms of switching time for its applications in a distribution feeder. Different gating approaches were employed for different applications. It was concluded that the transfer time of the STS depends upon the load configuration. Hence the control logic for STS operation, transfer and detection of voltage sags have been tested on an IEEE test bench under zero difference in phase angle and magnitude between preferred and alternate source prefault voltages, whereas in many practical applications this condition does not apply. Moschakis and Hatziargyriou (2003) considered a more practical case for TS operation. They have included commutation circuit in the control logic. Their approach makes the STS operation more realistic. They have considered the fault on the primary side of a 150/20-kV substation. The voltage ratings of the sources are adjusted before the occurrence of a fault or sag for smooth commutation of thyristors. Their control logic is based upon the voltage sag magnitude and voltage sag duration. Cheng and Chen (2006) showed more extensive treatment of commutation techniques in the control logic of the STS. They have presented the results for an impulse-commutated STS. Their approach can be used for many applications in power distribution systems with modification in the commutation logic and control circuit. Hong and Hsieh (2007) proposed a hybrid intelligent approach for determination of STS location in a 33-bus system.

Results of these researches show that the role of STS control logic is very crucial in implementation of load transfer between the complementary distribution feeders to offset their overloading and under loading effects. None of the available control strategies show significant performance for implementation of the STS to transfer the load of a heavily loaded feeder to a lightly loaded feeder.

In this paper the control logic for the operation of an STS system has been developed, which performs the switching operation to transfer the load among the complementary feeders as per requirement on daily or weekly basis. The proposed control logic of the STS system transfers the load of the preferred feeder to the alternate feeder and then back to the preferred feeder. The transfer time of the proposed STS's control logic is within permissible limits as laid down in IEEE Std. 446. Whenever an overloading condition occurs on the preferred feeder, STS control logic provides fast transfer of sensitive loads to the alternate feeder. In addition to being fast, the transfer is performed with no source paralleling (Mokhtari *et al.*, 2002).

The performance of the control logic is important to the implementation of load transfer for the feeders in urban areas. The STS system utilized has two thyristors per phase and the forced commutation technique has been implemented to turn off the outgoing thyristors while transferring the load. Another important consideration for implementation of this approach is the selection of the optimal location for the installation of STS that pays the maximum

dividend to the consumer as well as the utility. This issue is not addressed in this paper. However, different simulation tests were performed for the feeders under study to optimize the best simulation results. PSCAD/EMTDC professional package (Olimpo and Acha, 2002; Manitoba HVDC Research Centre, 2004) was used for the modeling and analysis of the considered distribution network feeders.

In this paper, two complementary distribution feeders, New Exchange and Sector I-10/2, have been considered for the case study. Both distribution feeders are of Islamabad Electric Supply Company (IESCO), Pakistan and are in close proximity to their service areas. Figs.1 and 2 show the one-line diagram of the New Exchange feeder and the Sector I-10/2 feeder, respectively.

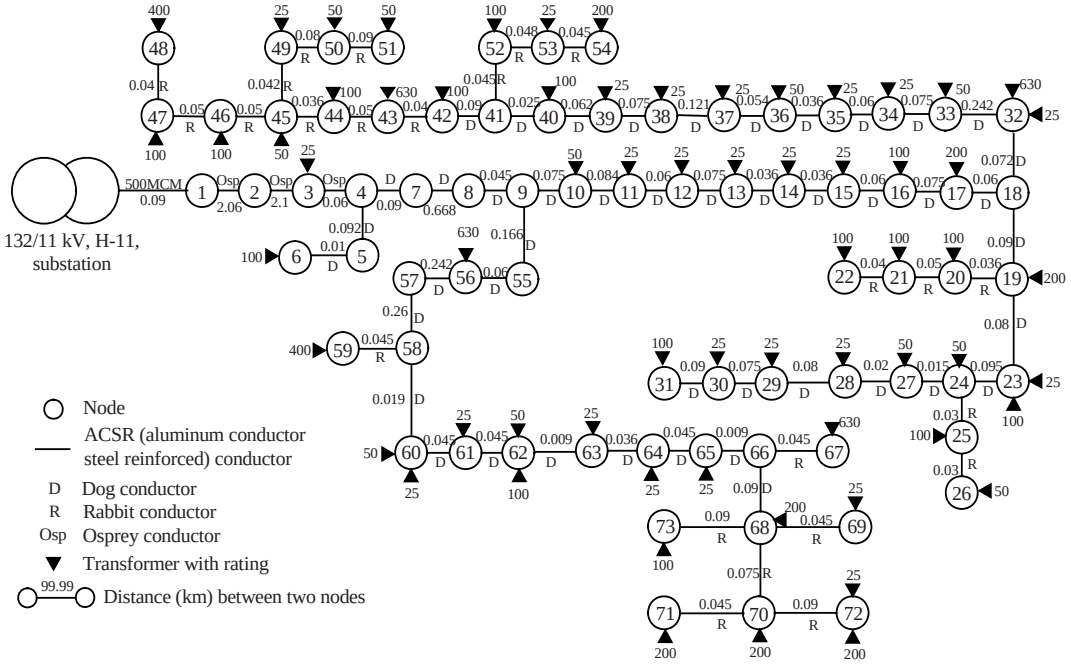


Fig.1 One-line diagram of the New Exchange feeder (preferred feeder)

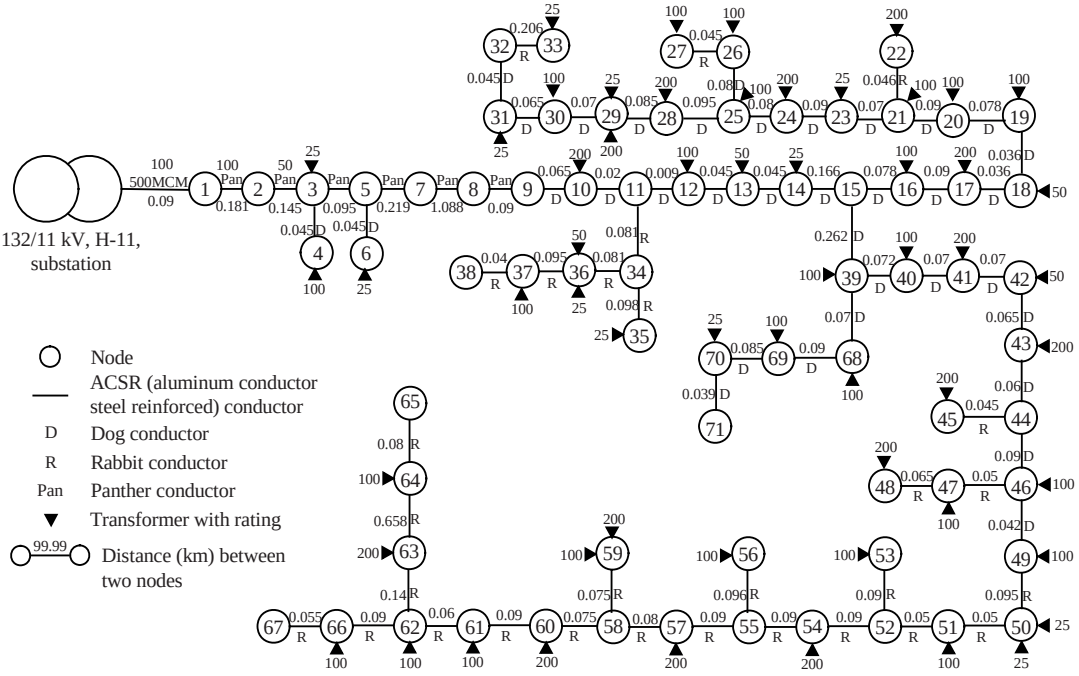


Fig.2 One-line diagram of the Sector I-10/2 feeder (alternate feeder)

STRUCTURE OF A STATIC TRANSFER SWITCH SYSTEM

Availability of reliable semiconductor switches and stringent voltage quality requirements of sensitive loads have made medium-voltage thyristor-based STSs attractive substitutes to electro-mechanical transfer switches during the recent years (Mokhtari *et al.*, 2001a). STSs are available for voltages up to 38 kV and load current ratings of 1200 A (Reed *et al.*, 1999). This makes them suitable for high power industrial operations. Normally an STS system consists of mainly two thyristor blocks and a control logic block. The structure of both STS blocks, i.e., block-I and block-II, is the same at the point of installation, as shown in Fig.3. Each STS block has two thyristors per phase connected back-to-back to allow load current to flow in both positive and negative directions.

Both feeders, preferred and alternate, are feeding their normal load. However, the preferred feeder is also feeding the sensitive load and STS-block-I is normally ON. Each thyristor of a block conducts only when a high gate pulse is applied at the respective thyristor. The detailed diagram of the proposed STS system for the implementation of the load transferring strategy is shown in Fig.4. The two different feeders along with their loads, segment impedances '*Z*' and STS systems are also shown schematically in Fig.4.

The two different feeders along with their loads, segment impedances and STS systems are also shown schematically in Fig.4. The proposed STS system consists of a total of three blocks, i.e., two thyristor blocks and one control logic block. The control logic block is further divided into two blocks, i.e., voltage detection block and main thyristor monitoring and commutation block. The description of the two thyristor blocks and one control logic block for the STS system is given in the following.

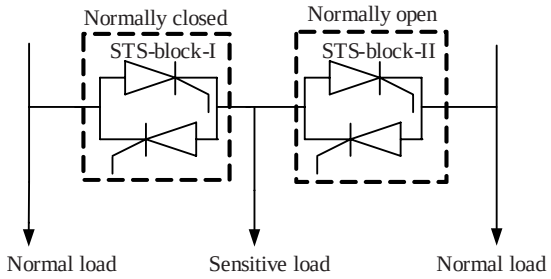


Fig.3 Schematic diagram of preferred and alternate feeders (with normal, sensitive load) and STS blocks

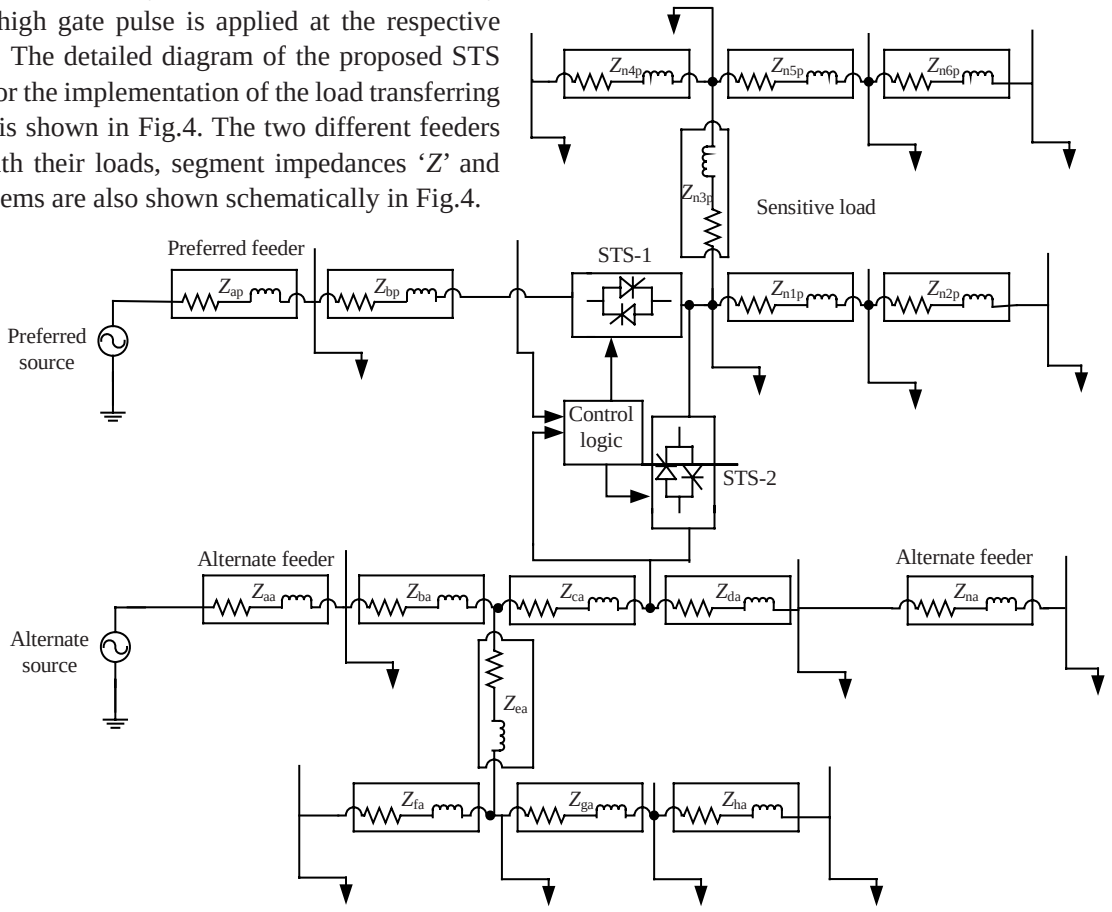


Fig.4 Schematic diagram of the preferred feeder, alternate feeder, and STS system

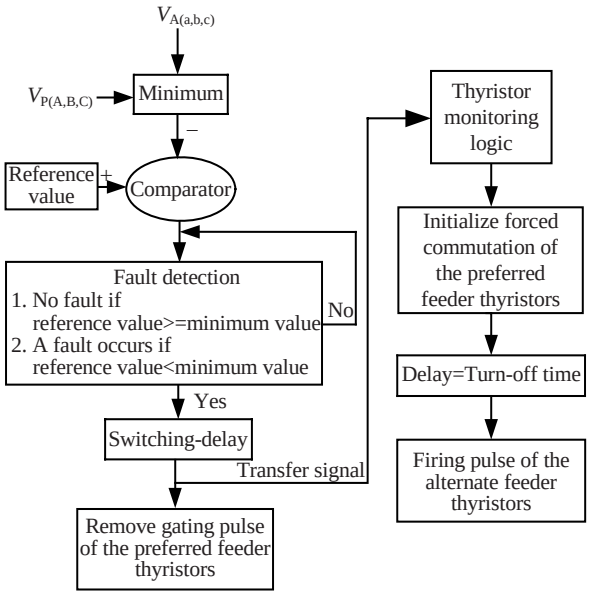
STS-block-I

This block is connected in series with the preferred feeder and is normally ON, i.e., the load is fed from the preferred feeder. The control logic block generates the required gate pulses for the respective thyristors of this block to turn it ON.

STS-block-II

This block is connected across both the feeders, preferred and alternate, and is normally OFF, i.e., no gate pulse is applied by the control logic block to turn it ON. When the preferred feeder is overloaded, the control logic block detects a voltage sag at the point of installation (PoI) of the STS and generates a high gate signal to turn ON the thyristors of STS-block-II.

At the same time, the control logic generates a low gate signal for the thyristors of STS-block-I. Ultimately, STS-block-II is turned ON and STS-block-I is turned OFF. Hence the sensitive load of the preferred feeder is now fed by the alternate feeder.



$V_{P(A,B,C)}$: Preferred feeder RMS voltages at PoI of STS
$V_{A(a,b,c)}$: Alternate feeder RMS voltages at PoI of STS

Fig.5 Schematic diagram of the control logic of the STS system

STS CONTROL LOGIC

The control logic performs load transfer if needed to the alternate feeder and back when faults or disturbances are removed. The schematic diagram of the STS control logic is shown in Fig.5. It is assumed that all the commutation capacitors are already charged and sensitive load is fed by the preferred feeder prior to the working of control logic of Fig.5. STS control logic generates high or low gating pulses for firing of the main thyristors of both STS-block-I and STS-block-II. In case of a fault or disturbance, the preferred feeder's thyristor block, i.e., STS-block-I, will receive a low gating pulse, and the alternate feeder's thyristor block, i.e., STS-block-II, will now receive a high gating pulse as it has already been receiving a low gating pulse.

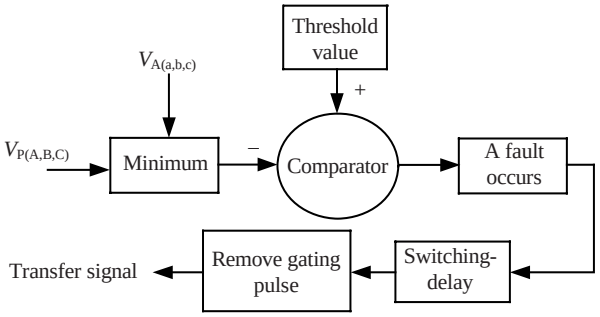
Each thyristor block has two main thyristors connected back-to-back as shown in Fig.4. Hence there will be three such blocks for the preferred feeder and three blocks for the alternate feeder. As for each main thyristor, an independent gate pulse is generated. Hence a total of 12 gating pulses will be generated for both feeders' main thyristors.

The control logic monitors the status of the voltage of both the feeders at the PoI of the STS. In case of any violation in performance indices on the preferred feeder, the control logic generates a high gating pulse for STS-block-II to turn it ON and a low gating pulse for STS-block-I to turn it OFF. But to turn off the thyristors of STS-block-I, forced commutation has been implemented. When disturbance on the preferred feeder is removed, the control logic generates a high gate pulse for the thyristor of STS-block-I and transfers the load again on the preferred feeder. The control logic consists of the voltage detection logic, and main thyristor monitoring and commutation block.

Voltage detection logic

The voltage detection logic detects a fault or disturbance at the preferred feeder at the PoI of the STS and removes gating signals of the preferred feeder's thyristor. The proposed voltage detection circuit is shown in Fig.6. The RMS phase voltages from the preferred feeder and the alternate feeder are compared. The output of the comparator block is further compared with a threshold value, which is

usually 5% of the rated voltage value. As long as the output of the comparator block is within the threshold value, the output of the comparator is low. When a fault or disturbance occurs, the output of the comparator will be high. A switching-delay block is also introduced to avoid momentary switching of the thyristor block. As soon as the output of the switching-delay block is high, the gating signals of the main thyristors of STS-block-I are removed. If interruption time is greater than delay time of the switching-delay block, the transfer signal will be generated and applied as a firing pulse for the commutation thyristors. Voltage detection and transfer time must be slightly less than one-fourth of the rated frequency cycle (Cheng and Chen, 2004).



$V_{P(A,B,C)}$: Preferred feeder RMS voltages at PoI of STS
$V_{A(a,b,c)}$: Alternate feeder RMS voltages at PoI of STS

Fig.6 Schematic diagram of voltage detection circuit

Thyristor monitoring logic and commutation technique

When a voltage sag or a fault occurs on the preferred feeder, the thyristor monitoring logic determines which of the main six thyristors are in conducting mode. The thyristor monitoring logic will generate a positive-high signal for positive half conducting main thyristors and a negative-low signal for negative conducting main thyristors. These signals are used to trigger the commutation thyristors to commutate the preferred feeder's main thyristors. As voltage detection logic generates a high output signal, the gating pulse for the main thyristors of the alternate feeder, i.e., STS-block-II, would not be high immediately. But the outgoing main thyristors of the preferred feeder are forced commutated first using the forced commutation technique as shown in Fig.7. Then a high gating pulse is applied to turn ON the alternate feeder thyristors. Sensitive load is now completely transferred to the alternate feeder. The detailed description of Fig.7 is described in the next section.

The proposed commutation technique has been tested for different types of faults and loads having power factor 0.85 lagging according to IEEE Std. 929.

WORKING OF PROPOSED COMMUTATION TECHNIQUE

Fig.7 shows a schematic diagram of the proposed commutation technique implemented on both feeders, the preferred and the alternate.

Two three-phase independent voltage sources are used to feed the three-phase sensitive load through preferred and alternate feeders alternatively. The sensitive load is mainly fed from the preferred feeder. For an effective implementation of the STS system and its control logic, six main thyristors are used for each feeder to feed the sensitive load. Two main thyristors per phase, connected back-to-back, are used for the conduction of a full AC cycle. On the preferred feeder side for phase A, two main thyristors TM_{AP} and TM_{AN} have been used. Similarly, phase B has two main thyristors TM_{BP}, TM_{BN} and phase C has two main thyristors TM_{CP}, TM_{CN}. The main thyristor of each phase on the preferred feeder has its own commutation circuitry and a total of six commutation circuits have been used. To describe the proposed commutation technique in detail, only one of the two commutation circuits of phase A of the preferred feeder has been considered. The considered commutation circuit for the main thyristor—TM_{AP} of phase A—consists of an inductor L_{AP}, a capacitor C_{AP}, a resistor R, a thyristor TC_{AP} for charging the capacitor C_{AP}, and two thyristors, TA_{PComm} and TD_{AP}, for discharging the capacitor C_{AP}.

To initialize the commutation circuit at t=0, all of the six capacitors of the commutation circuits are charged to voltage V_{cc} through their respective thyristors and resistors. The polarity of each capacitor voltage is shown in Fig.7. Then at t=0, all the main thyristors are fired by applying a gating pulse to feed the power to the sensitive load through the preferred feeder.

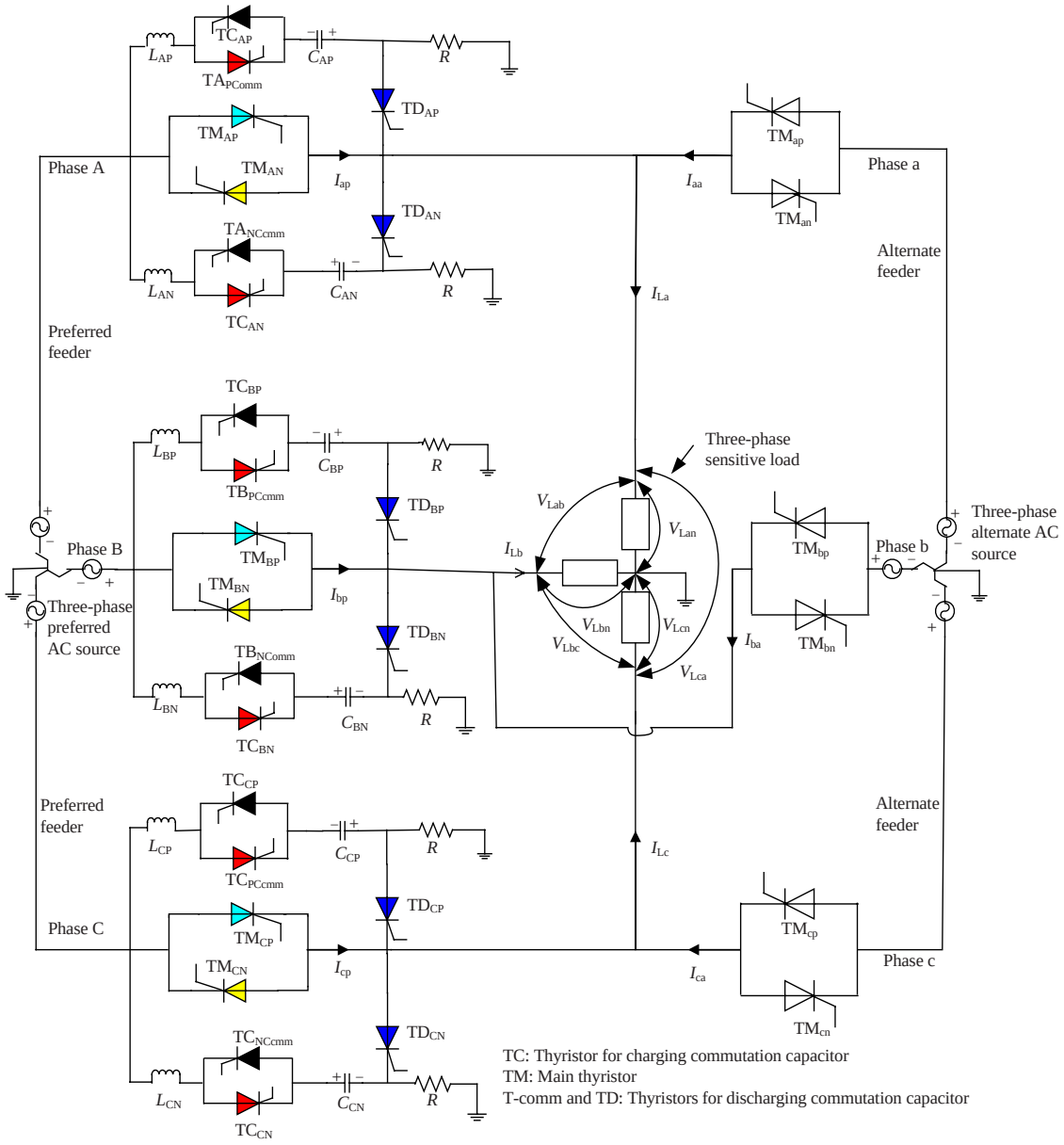


Fig.7 Schematic diagram of the proposed commutation technique implemented for the operation of the STS system for a three-phase 11 kV distribution feeder

When a voltage sag or a fault occurs on the preferred feeder or preferred source, the voltage detection block of the control logic removes the gating pulse of all the main thyristors. At this instance, all or some of the three main thyristors may not be fully turned OFF due to the lagging current. Therefore, to turn OFF the main thyristors of the preferred feeder (STS-block-I), a forced commutation technique has been implemented. To initialize forced commutation of the main thyristor TM_{AP} of phase A, the thyristors TA_{PComm} and TD_{AP} need to be fired for discharging of capacitor C_{AP}. Therefore when the transfer signal of the voltage detection block is high, the thyristor monitoring logic generates a gate pulse for firing of these two thyristors. In this way, the capacitor voltage V_{cc} appears across the main thyristor TM_{AP} in a reverse direction and TM_{AP} will be commutated. The same commutation process will be repeated for all other main thyristors. The control logic then issues a high gating pulse for firing of all the six thyristors of the alternate feeder after a predetermined turn-off time of the respective main thyristors of the preferred

feeder. The sensitive load is now transferred to the alternate feeder completely.

The proposed commutation technique is more effective and efficient as compared to simply applying the time delay logic without a forced commutation technique, as proposed by some researchers. Time delay logic has been used to avoid the cross current phenomena, and hence to reduce the transfer time of the sensitive load from the preferred feeder to the alternate feeder. In the time delay logic, the time of delay varies for loads having different power factors and also for symmetrical as well as unsymmetrical faults.

But as stated above, the drawback of this delay logic is that the delay time is quite different for different types of faults for a three-phase system and delay time also depends on the instance of the occurrence of faults. Whereas, the forced commutation technique ensures safe and sound operation of thyristors and hence the STS system.

Commutation technique implementation

To implement the proposed commutation technique and to validate the effectiveness of STS control logic, two test cases—without forced commutation and with forced commutation—were simulated by considering a three-phase-to-ground fault (balanced fault) and a two-phase-to-ground fault (unbalanced fault) on the preferred feeder. The schematic diagram of Fig.7 has been considered for these test case studies.

The total simulation time is 0.500 s. Fault duration time is 0.100 s whereas the fault occurs at 0.301 s for both the above types of faults. The simulation was performed using the PSCAD/EMTDC professional software package.

Three-phase-to-ground fault

Firstly, consider the case of three-phase-to-ground fault that occurs on the preferred feeder as the forced commutation circuitry is not involved. As soon as a fault occurs on the preferred feeder, the control logic removes the gating pulse of the preferred feeder thyristors after a certain delay and gating pulse of the alternate feeder thyristors are high without proper commutation of the outgoing thyristors. As a result, the cross current occurs in phase C and hence the transfer time is maximum. The simulation results are summarized in Fig.8.

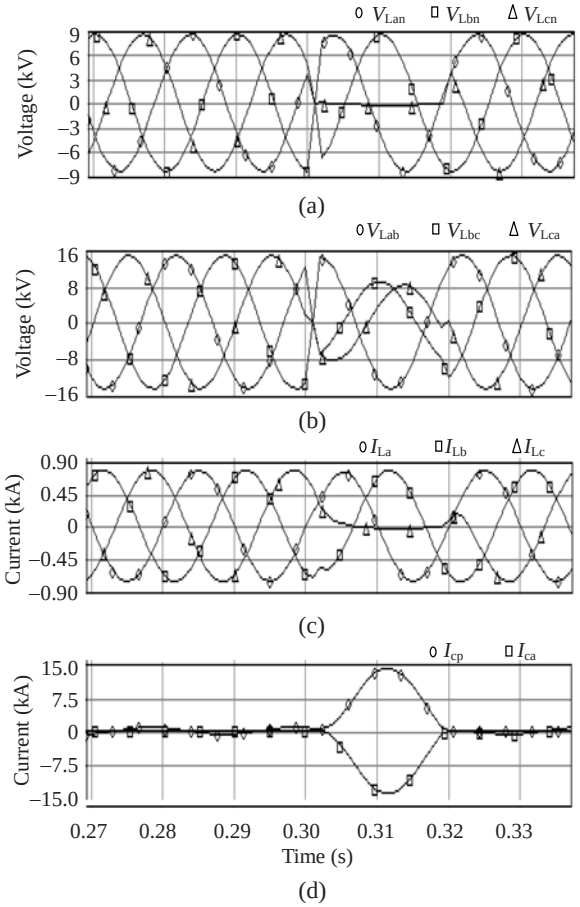


Fig.8 Simulation results of three-phase circuit for a three-phase-to-ground fault at the preferred feeder as the forced commutation is not involved

(a) Load side line-to-ground voltages; (b) Load side line-to-line voltages; (c) Load side line currents; (d) Main thyristor phase current for phase C

These simulation results show that if the alternate feeder's main thyristors are forward-biased while the preferred feeder thyristors are still conducting, the cross current can occur in any phase. It is also observed during different simulation studies that as the fault point-on-wave changes, the cross current does not always occur even if the forced commutation is not involved. But in this particular case study the cross current occurs in phase C and the transfer time is beyond the permissible limit—20 ms.

Secondly, consider the case when forced commutation is involved in the STS operation for feeder load transfer. As soon as a fault occurs on the preferred feeder, the control logic removes the gating pulse of the preferred feeder thyristors after a certain switching delay. Main thyristors of the preferred

feeder are forced commutated first by triggering of thyristors for capacitors discharging.

After the completion of commutation of the preferred feeder's main thyristors, the gating pulse to the alternate feeder thyristors is applied. The time to complete the commutation of the preferred feeder's main thyristors can be calculated from the following circuit parameters: commutation branch inductors and capacitors; maximum load current and system voltage rating; capacitor voltage.

As the commutation process starts, the capacitor voltage appears across the main thyristors as shown in Fig.9. This figure shows that

(1) For phase-a, there is no need of capacitor current, I_C, because the transfer is smooth;

(2) For phase b during the transfer process, a small amount of current is required and the total time delay is 2 ms;

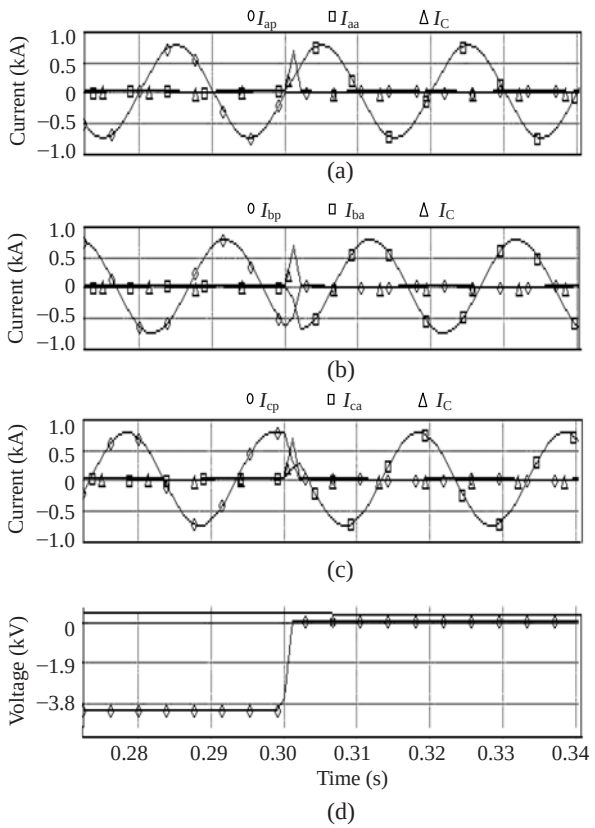


Fig.9 Main thyristor phase currents waveforms for phases a, b, and c along with capacitor current and voltage

(a) Main thyristor phase a and capacitor currents; (b) Main thyristor phase b and capacitor currents; (c) Main thyristor phase c and capacitor currents; (d) Capacitor voltage

(3) For phase c during the transfer, there is need of capacitor current to be supplied to the load, and the time of transfer is 2 ms.

Fig.10 summarizes the same circuit parameters as Fig.8 but with the forced commutation involved. The cross current through the main thyristors is eliminated and the transfer time is within the permissible limit, i.e., less than 2 ms.

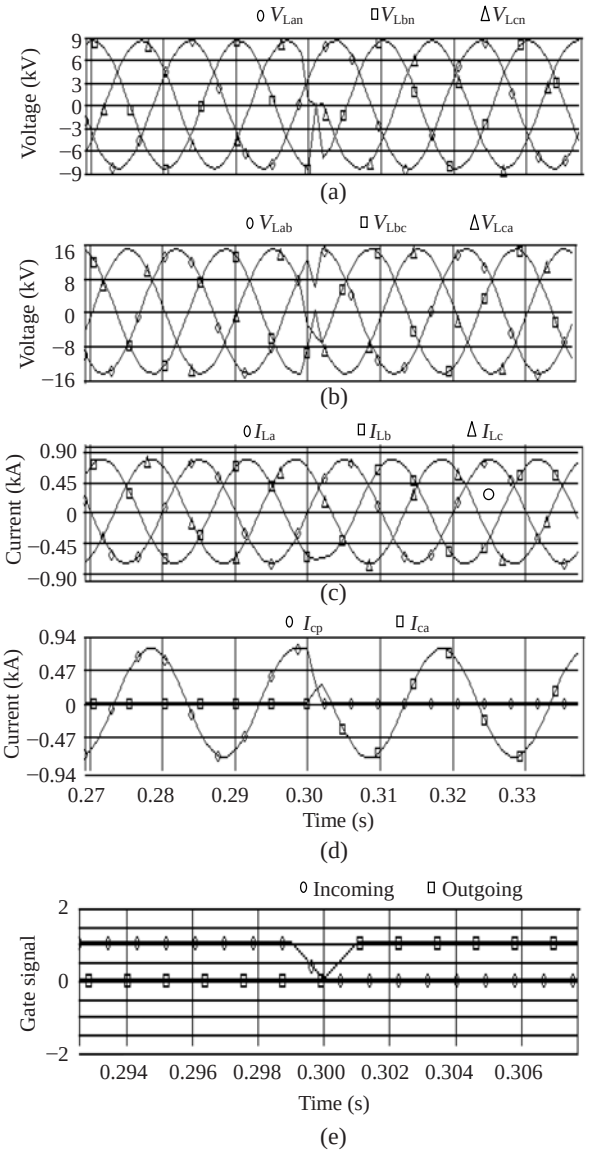


Fig.10 Simulation results of the three-phase circuit when a three-phase-to-ground fault occurs at the preferred feeder as the forced commutation is involved

(a) Load side line-to-ground voltages; (b) Load side line-to-line voltages; (c) Load side line currents; (d) No cross currents for phase C; (e) Incoming and outgoing gate signals

Two-phase-to-ground fault

In case of a two-phase-to-ground fault on the preferred feeder and forced commutation not involved, the simulation results are shown in Fig.11.

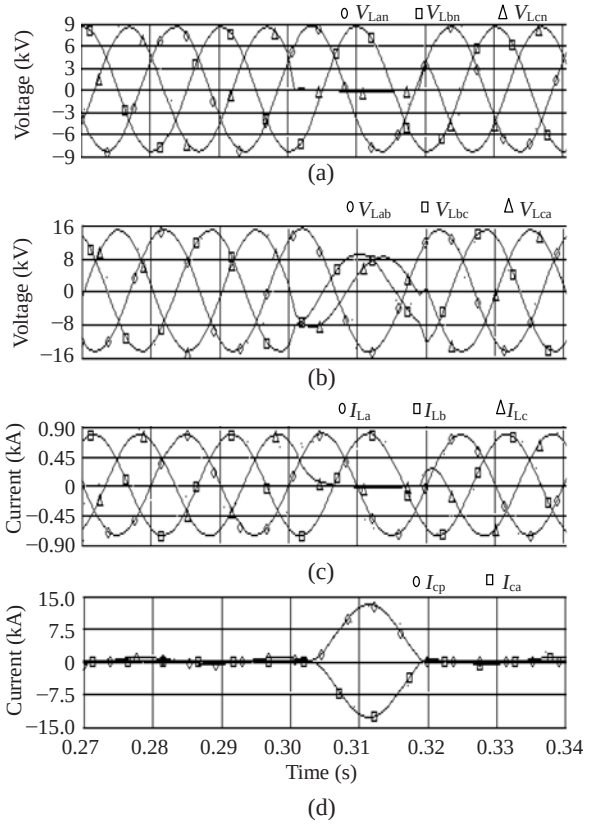


Fig.11 Simulation results of three-phase circuit when a two-phase-to-ground fault occurs at the preferred feeder as the forced commutation is not involved

(a) Load side line-to-ground voltages—the maximum voltage sag occurs only in V_{Lcn}; (b) Load side line-to-line voltages—the maximum voltage sag occurs in V_{Lbc} and V_{Lca}; (c) Three-phase load side line currents—the maximum sag occurs only in I_{Lc}; (d) Cross current flows in phase C for main thyristor phase current

These simulation results show that the main thyristors in the alternate feeder are forward-biased while the thyristors in the preferred feeder are conducting. In this case study, the cross current occurs in phase C, and the transfer time is approximately 20 ms, beyond the permissible limit.

Secondly, consider the case when forced commutation is involved. Fig.12 summarizes the same circuit parameters as Fig.11. Now no cross current phenomena occur and the transfer time is less than 2 ms.

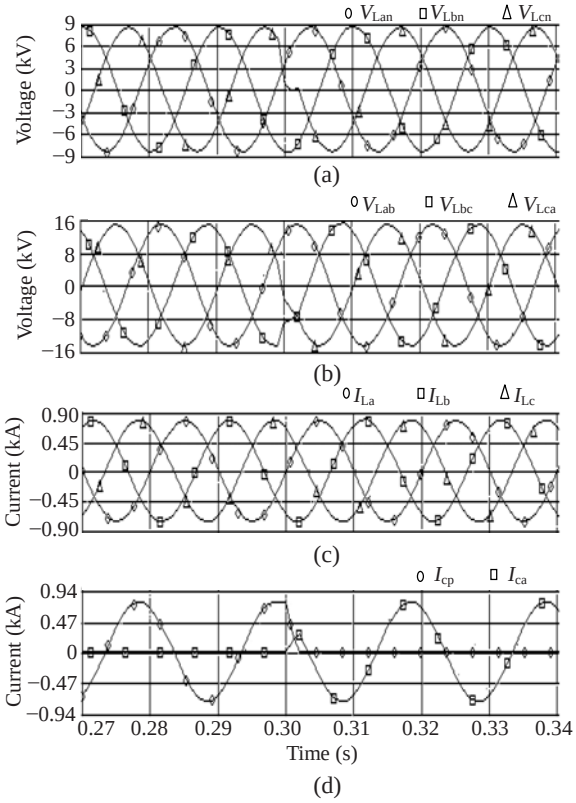


Fig.12 Simulation results of the three-phase circuit when a two-phase-to-ground fault occurs at the preferred feeder as the forced commutation is involved

(a) Load side line-to-ground voltages; (b) Load side line-to-line voltages; (c) Load line currents; (d) No cross currents for phase C

CASE STUDIES

Two 11-kV distribution network feeders, the New Exchange and the Sector I-10/2, were selected for case studies. These network feeders, as described earlier, are located in the jurisdiction of IESCO, Pakistan. Two feeders having different lengths, diversities in consumers, and non-homogenous conductor types are considered. The code names and other specifications of these conductors are shown in Table 1. The conductor used for both feeders is aluminum conductor steel reinforced (ACSR).

Table 1 Data for feeder's conductors (Hesterlee *et al.*, 1996)

Conductor code	Number of strands*	Diameter* (mm)	Layer(s) of aluminum	GMR (mm)
Rabbit	6/1	3.35/3.35	1	2.5125
Dog	6/7	4.72/1.57	1	3.5375
Panther	30/7	3.00/3.00	2	8.6730
Osprey	18/1	4.47/4.47	2	8.6718

* Aluminum/Steel. GMR: geometric mean radius

New Exchange feeder (preferred feeder)

This feeder emanates from a 132/11 kV substation, H-11 Islamabad. The feeder including laterals and sub-laterals is 9.015 km in total length and contains 77 nodes. The whole system is of three-phase, 50 Hz, and 11.0 kV ratings. Various categories of loads, including sensitive loads, are fed by this feeder. The sensitive loads are located at nodes 38~45. The total number of distribution transformers connected is 68 and the total load is 7495 kV·A, as shown in Table 2. The data required for complete network feeder simulation was collected by field visits and consulting the concerned officers and staff.

Table 2 Load data for the New Exchange feeder

Distribution transformer rating (kV·A)	Number of transformers	Connected load (kV·A)
25	27	675
50	12	600
100	17	1700
200	6	1200
400	2	800
630	4	2520
Total	68	7495

Sector I-10/2 feeder (alternate feeder)

This feeder also starts from a 132/11 kV substation, H-11 Islamabad and terminates within the vicinity of the preferred feeder near node 11. The feeder including laterals and sub-laterals is 7.458 km in the total length and contains 71 nodes. The whole system is of three-phase, 50 Hz, and 11.0 kV ratings. Various categories of loads, including sensitive loads, are fed by this feeder. The feeder consists of 57 distribution transformers and 6375 kV·A load, as shown in Table 3.

When a fault occurs on the preferred feeder, the sensitive loads are shifted to an alternate feeder within minimum time.

Table 3 Load data for the Sector I-10/2 feeder

Distribution transformer rating (kV·A)	Number of transformers	Connected load (kV·A)
25	11	275
50	4	200
100	25	2500
200	17	3400
Total	57	6375

Simulation results

As the load on distribution feeders is highly variable in nature, the entire connected load is not served all the time. For analysis, a maximum of three-fourths load is considered to be served by both feeders. Simulations were carried for a time period of 500 ms. Firstly, the preferred network feeder was considered with no alternate feeder and hence no STS system for a period of 200 ms. It is observed that the value of voltage sag is greater than permissible limits (±5%) for different nodes as shown in Fig.11 (IEEE-Std-141, 1986). The alternate feeder feeds only its own load for a period of 200 ms. Secondly, the preferred network feeder was considered with an alternate feeder and with an STS system for a period of 300 ms. Now the alternate feeder feeds and shares the sensitive loads of the preferred feeder for 300 ms.

The simulation results are plotted on Fig.13, which shows that the accumulated voltage profiles all the considered nodes. With the use of STS, voltage sag can be avoided.

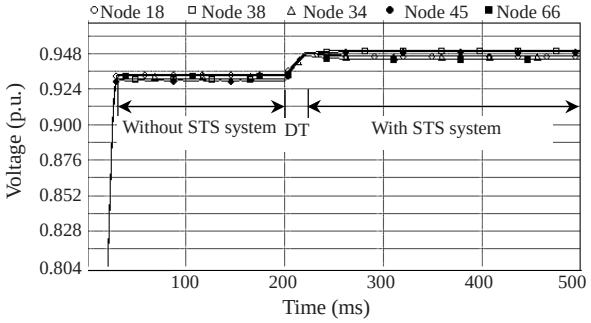


Fig.13 Simulation results showing voltage magnitude in per unit at different nodes on the preferred feeder without and with the STS system

DT: detection and transfer

CONCLUSION

A steady load growth has become a global phenomenon in recent years. In this era of deregulation and restructuring environment, it is a challenging task for utilities to provide uninterruptible power to the consumers. Electric utilities try to meet the demand for reliable power by utilizing different technologies. The technique adopted here is the installation of a static transfer switch system at the point of interest to meet the load for peak hours of the

complementary feeders. This approach is much economical for improving the performance of the complementary feeders. The commutation technique implemented in this paper prevents the source paralleling, and hence no cross current flows. There is a significant scope for the proposed technique for performance improvement of the feeders under different loading conditions, demand side management program implementation, and load management program implementation. The simulation results show that when a fault or voltage sag occurs, the control logic transfers the critical load to the alternate feeder efficiently and effectively.

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