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Multi-mode controller IC for soft-switched flyback converter with high efficiency over the entire load range*

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Abstract: This paper presents a multi-mode control scheme for a soft-switched flyback converter to achieve high efficiency and excellent load regulation over the entire load range. At heavy load, critical conduction mode with valley switching (CCMVS) is employed to realize soft switching so as to reduce turn-on loss of power switch as well as conducted electromagnetic interference (EMI). At light load, the converter operates in discontinuous conduction mode (DCM) with valley switching and adaptive off-time control (AOT) to limit the switching frequency range and maintain load regulation. At extremely light load or in standby mode, burst mode operation is adopted to provide low power consumption through reducing both switching frequency and static power dissipation of the controller. The multi-mode control is implemented by an oscillator whose pulse duration is adjusted by output feedback. An accurate valley switching control circuit guarantees the minimum turn-on voltage drop of power switch. The prototype of the controller IC was fabricated in a 1.5-μm BiCMOS process and applied to a 310 V/20 V, 90 W flyback DC/DC converter circuitry. Experimental results showed that all expected functions were realized successfully. The flyback converter achieved a high efficiency of over 80% from full load down to 2.5 W, with the maximum reaching 88.8%, while the total power consumption in standby mode was about 300 mW.

Key words: Integrated circuit, Multi-mode controller, Soft-switched flyback converter, Valley detection
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INTRODUCTION

As is well known, transition loss during the turn-on or turn-off instant of power switch is generated by the overlap of drain-source voltage and drain current. High current driving for power switch can reduce the length of the overlap. However, it does not reduce the drain-source voltage and drain current (Balogh, 2001). Consequently, its contribution to reducing power loss is limited. Thus soft switching is introduced. In isolated power supply applications with power lower than 200 W, the flyback topology is very attractive due to its simple configuration and thus economy. Moreover, with the parasitic drain capacitance of power switch, no additional component is required to achieve soft switching in such a topology (Tabisz *et al*., 1989). While the flyback converter operates in discontinuous conduction mode (DCM) or critical conduction mode, i.e., at the transition point of continuous conduction mode (CCM) and DCM, LC resonance will occur and make it possible to minimize the turn-on voltage of power switch. Consequently the turn-on transition loss as well as conducted electromagnetic interference (EMI) can be minimized (Liu and Lee, 1990).

In this paper, the critical conduction mode with valley switching (CCMVS) is applied at heavy load so that the converter can achieve soft switching and maintain load regulation. However, being a variable frequency (VF) control, the CCMVS converter suffers from high frequency and consequently efficiency degradation at light load. Moreover, it might degrade

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load regulation due to limited minimum on-time (Spiazzi *et al*., 2000). As a solution, multi-mode control is proposed in this paper to achieve high efficiency and excellent load regulation over the entire load range. At heavy load, CCMVS is kept; while at light load, DCM with valley switching and adaptive off-time control (AOT) is adopted to reduce the switching frequency and maintain proper operation (Panov and Jovanovic, 2002). And at extremely light load or in standby mode, several approaches including pulse frequency modulation (PFM) (Gildersleeve *et al*., 2002; Xiao *et al*., 2004; Sahu and Rincon-Mora, 2007), dithering skip modulation (DSM) (Huang *et al*., 2007) and gate charge modulation (GCM) (Mulligan *et al*., 2007) are utilized to improve efficiency. However, all these measures fail to reduce the static power dissipation of the controller. Therefore, burst mode operation is applied to reduce transition loss of the power switch as well as static power dissipation of the controller.

To realize the proposed multi-mode control, an integrated circuit (IC) controller design is proposed. In the controller, a proposed voltage controlled oscillator (VCO) is used to realize AOT for transition between different modes. Meanwhile, to ensure soft switching down to light load, an accurate valley switching control circuit is proposed. The prototype controller IC was fabricated in a 1.5-μm BiCMOS process with an area of 6.3 mm^2. And the controller IC was applied to a 310 V/20 V, 90 W flyback DC/DC converter. Experimental results demonstrate a high efficiency of above 80% from full load down to 2.5 W as well as excellent load regulation.

PROPOSED MULTI-MODE, SOFT-SWITCHED OPERATION

The functional diagram of the multi-mode soft-switched flyback converter is shown in Fig.1, and its key waveforms in different modes, in Fig.2. The operation principles in each mode are described in the following subsections.

CCMVS at heavy load

The switching cycle starts at $t=t_0$, when the switch SW turns on. During the interval [t_0, t_1], the switch current I_{SW} increases linearly. At $t=t_1$, when I_{SW} reaches the peak value I_{PK}, which is determined by the output signal V_{EA} of the error amplifier EA, the RS latch which controls the gate driver, is reset to turn off SW. After that, transformer magnetizing current is commutated from the primary winding to the secondary one and linearly decreases during the interval [t_1, t_2]. When the secondary current I_s reaches zero at $t=t_2$, transformer magnetizing inductance starts resonating with parasitic capacitances of the power switch C_{SW} and the secondary rectifier C_D. The voltage across the power switch V_{DS} is sensed by the auxiliary winding N_{AU}, the voltage across which, V_{SENSE}, is monitored by the valley detector. V_{SENSE} oscillates, as shown in Fig.2a. When V_{SENSE} reaches the valley at $t=t_3$, output signal of the valley switching control circuit V becomes high. Meanwhile, load condition also affects the way the RS latch is set. At heavy load, the duration of the output pulse P of VCO, $T_{p\,min}$, expires before I_s falls to zero. Thus, at $t=t_3$, signal V propagates through delay flip flop (DFF) and sets the RS latch. As a result, the power switch turns on with voltage $V_{IN}-N(V_O+V_R)$ across it, greatly reducing the turn-on loss.

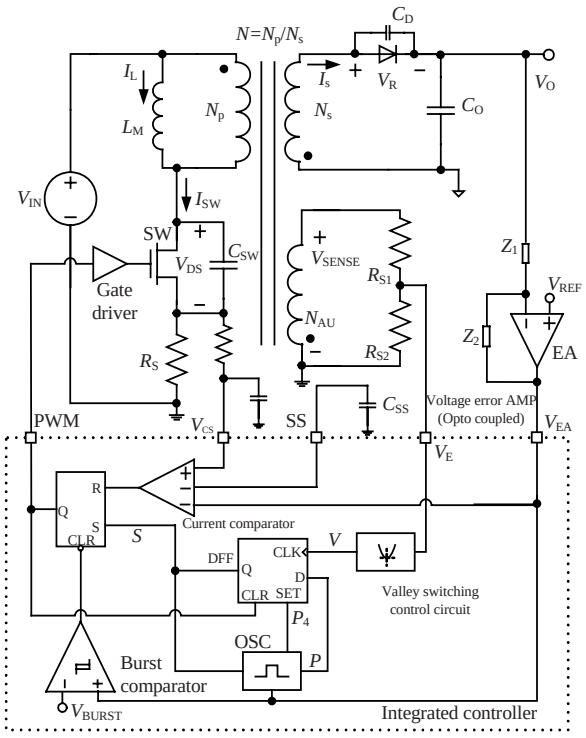


Fig.1 Functional diagram of the multi-mode soft-switched flyback converter

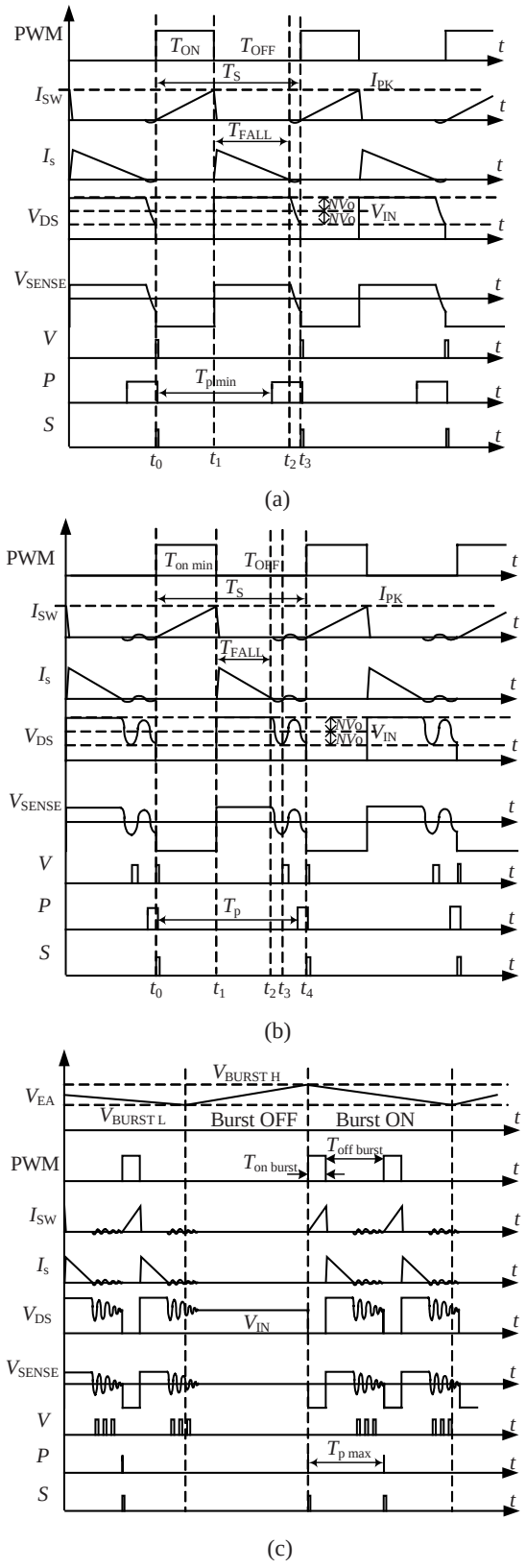


Fig.2 Key waveforms in multi-mode operation. (a) Heavy load; (b) Light load; (c) Extremely light load

The peak value I_{PK} of switch SW is given by

$$I_{PK} = V_{IN} \cdot T_{ON} / L_M , \tag{1}$$

or

$$I_{PK} = N(V_O + V_R)T_{FALL} / L_M . \tag{2}$$

Load current is equal to the average value of the secondary current

$$I_O = \frac{N \cdot I_{PK} \cdot T_{FALL}}{2T_S}. \tag{3}$$

In the critical conduction mode, ignoring the duration of [t_2, t_3], the switching period is

$$T_S = T_{ON} + T_{FALL}. \tag{4}$$

Combining Eqs.(1)~(4), the output current is derived as

$$I_O = \frac{N^2(V_O + V_R)}{2L_M(1 + M \cdot N)^2 f_s}, \tag{5}$$

where $M=(V_O+V_R)/V_{IN}$ is the voltage conversion ratio, and f_s is the switching frequency. The relationship between switching frequency f_s and output power P_{OCCMVS} is given by

$$f_s = \frac{N^2 \cdot V_O(V_O + V_R)}{2L_M(1 + M \cdot N)^2 P_{OCCMVS}}. \tag{6}$$

Eq.(6) shows that f_s is inversely proportional to P_{OCCMVS}. In order to prevent an excessive f_s and consequently efficiency degradation at light load, it is necessary to clamp f_s at a fixed value. In this design $f_{s\,max}$=120 kHz. When clamping happens, the converter operates in DCM mode with a fixed switching frequency. The load regulation is achieved by on-time adjustment, until the minimum on-time is reached. Then the converter enters DCM with valley switching and AOT operation mode.

DCM with valley switching and AOT at light load

As can be seen in Fig.2b, waveforms of the DCM mode coincide with those of the CCMVS until $t=t_3$. At light load, I_s falls to zero before the end of T_p, which is inversely proportional to the output power. Therefore, signal V cannot propagate through DFF until P expires, which results in the first propagation

at $t=t_4$. Valley switching is still obtained, though the turn-on voltage across the power switch is higher than that in the CCMVS mode because of resonance decay.

As mentioned earlier, to solve the problem of load regulation at light load, off-time increases as the load decreases while on-time is kept $T_{\text{on DCM}}$. Off-time adaptation is realized by adjusting the VCO pulse duration T_p, which is in accordance with the error amplifier output signal V_{EA}. The VCO implementation will be discussed later.

According to Eqs.(1)~(3), the relationship between switching frequency f_s and output power P_{ODCM} is written as

$$f_s = \frac{2L_M \cdot P_{ODCM}}{V_{IN}^2 \cdot T_{\text{on DCM}}^2}. \tag{7}$$

The switching frequency is proportional to the output power. However, it is clamped at 40 kHz in this design. So in a certain load condition, over supply occurs and the converter enters burst mode operation.

Burst mode at extremely light load or in standby mode

At extremely light load or in standby mode, the converter switches to burst mode, as in Fig.2c where both on-time $T_{\text{on burst}}$ and off-time $T_{\text{off burst}}$ are forced unchanged. The load regulation is achieved by operating the converter in an alternation of burst on and burst off. The error amplifier output signal V_{EA} is compared with the references $V_{\text{BURST H}}$ and $V_{\text{BURST L}}$. When $V_{EA}>V_{\text{BURST H}}$, the controller operates in burst on, where it generates several pulses to charge the output capacitor. Because the converter delivers excessive power to the load in every pulse, the output voltage increases continuously and V_{EA} decreases. Note that the frequency of every pulse is fixed at 40 kHz. During burst on, the DFF cannot be triggered when P expires, since the output signal V of the valley switching control circuit is unavailable due to resonance decaying to zero. Thus P_4, which corresponds to a maximum pulse duration $T_{\text{p max}}$, is used to forcibly set the DFF. The new switching cycle starts when P_4 expires regardless of V. When $V_{EA}<V_{\text{BURST L}}$, the converter operates in burst off, where it stays idle, causing V_{EA} to rise again. The output power is given by

$$P_{\text{BURST}} = \frac{V_{IN}^2 \cdot T_{\text{on burst}}^2}{2L_M \cdot T_s} \frac{N_{on}}{N_{on} + N_{off}}, \tag{8}$$

where N_{on} and N_{off} are the number of switching pulses contained in burst on and skipped in burst off, respectively. N_{on} drops while N_{off} mounts when the load decreases. During burst off, except the burst comparator and some necessary logic gates, almost all the internal functional blocks are shut down to reduce static power consumption of the controller. Though valley switching cannot be achieved due to resonance decaying to zero, as in Fig.2c, the increase of N_{off} with load decrease still reduces the switching loss and static power dissipation of the controller. Thus, compared with DCM mode, burst mode operation is more suitable at extremely light load or in standby mode for low power consumption.

INTEGRATED CONTROLLER DESIGN

The circuits in the dotted square in Fig.1 can be integrated onto a monolithic chip. Besides them, basic functional blocks in conventional power management IC, such as under voltage lockout, bandgap reference, current bias, and voltage regulator, are also included. Moreover, the controller IC features protection functions like over current protection, over voltage protection, power limit, and soft start. In this section, two important functional blocks in this controller are described in detail.

VCO

The VCO implementation is shown in Fig.3a. As mentioned before, the VCO pulse duration T_p is adjusted in accordance with V_{EA} for off-time adaptation. This is achieved by setting the comparator upper threshold V_H as a function of V_{EA}. The relationship between T_p and V_{EA} is plotted in Fig.3b. When $V_{EA}>2$ V, T_p is clamped at 8.3 μs, and the converter operates in CCMVS; when $V_{EA}<1.4$ V, T_p is clamped at 25 μs, and the converter operates in burst mode, where the DFF is forcibly set by P_4 and a new switching cycle starts; when V_{EA} is in the range of 2~1.4 V, T_p changes linearly from 8.3 μs to 25 μs, and the converter operates in DCM with valley switching and AOT. Since the on-time of the power switch is clamped by constant minimum I_{PK} during DCM, the

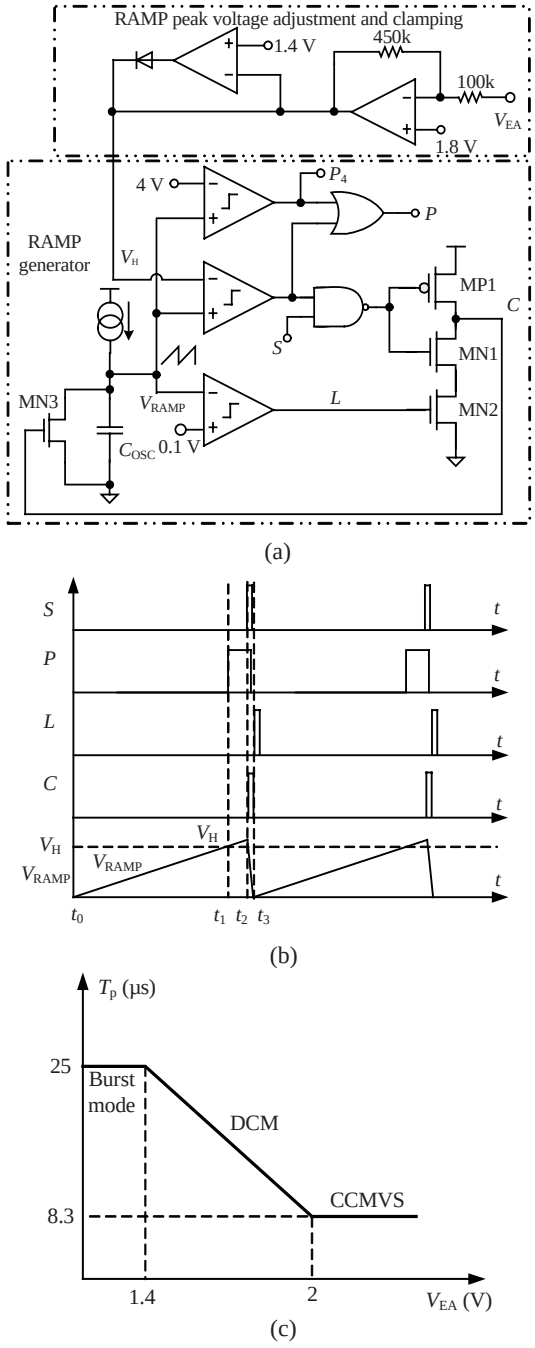


Fig.3 Implementation of VCO. (a) Functional diagram; (b) Key waveforms; (c) Relationship between V_{EA} and T_p

adaptation of off-time is realized indirectly by adjusting T_p.

Accurate valley switching control circuit

In conventional design (Panov and Jovanovic, 2002), a time delay equal to a quarter of the LC resonant period is added between V_{SENSE} zero-crossing and the setting of RS latch to achieve valley switching. The limitation of this method is that the time delay varies from application to application according to the resonant components. Also a high accuracy is difficult to achieve since practical component values vary with different circumstances. In this paper, an accurate control is obtained by directly detecting the valley of the signal waveform. So valley switching can be achieved adaptively. Fig.4a shows the circuit implementation of the valley switching control circuit, where the amplifiers and the comparator are the classical ones described in (Allen and Holberg, 2002).

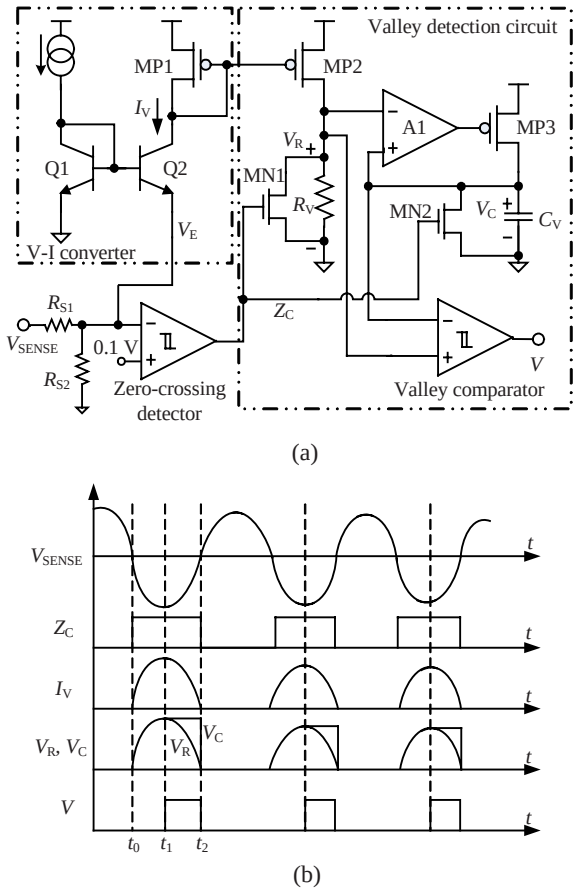


Fig.4 Implementation of valley switching control circuit. (a) Functional diagram; (b) Key waveforms

Fig.4b shows the operational principle. At $t=t_0$, V_{SENSE} changes its polarity from positive to negative, and Z_C, the output signal of the zero-crossing detector, turns high and enables the V-I converter and valley detection circuit. The V-I converter clamps V_E at about zero, and the current through resistor R_{S1} is sensed and mirrored to the valley detection circuit.

During the interval $[t_0, t_1]$, the waveform of current I_V resembles V_{SENSE}. Through the voltage follower A1, V_C (i.e., the voltage across the capacitor C_V) follows V_R (i.e., the voltage across the resistor R_V). At $t=t_1$, V_{SENSE} reaches the valley, so V_R and V_C reach the peak value. After that, V_R begins to fall and the closed loop of the voltage follower is broken, holding V_C at the peak value. And then the valley comparator output signal V turns high. At time $t=t_2$, V_{SENSE} changes its polarity from negative to positive, and Z_C turns low and disables the V-I converter and valley detection circuit. Meanwhile, V_R and V_C are released, and the circuit is ready for the next valley detection.

CONVERTER DESIGN AND EXPERIMENTAL RESULTS

The prototype IC of the proposed controller was fabricated in a 1.5-μm double-metal, single-poly BiCMOS process with an area of 6.3 mm^2. The die photograph of the chip is shown in Fig.5. Note that besides 7 pins, all the rest is for testing. A 310 V/20 V, 90 W flyback converter was constructed with the proposed controller IC (Erickson and Maksimovic, 2001). The key parameters are listed in Table 1.

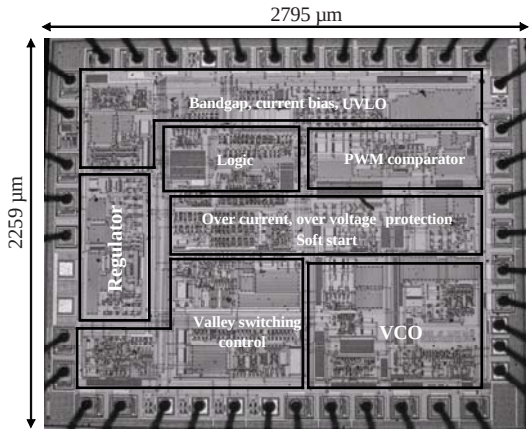


Fig.5 Chip microphotograph

Table 1 Key parameters of the converter

Parameter	Value	Parameter	Value
L_M	350 μH	R_{S1}	200 kΩ
N	4.5	R_{S2}	36 kΩ
R_{CS}	0.2 Ω	SW	IRF450

Multi-mode operation

Experimental results of the converter with the proposed multi-mode control for heavy, light, and extremely light loads are shown in Figs.6, 7, and 8, respectively. In Fig.6, at a load of 85 W, the duration of VCO output pulse T_p expires before the secondary current I_s falls to zero. When I_s reaches zero, the output signal V of the valley switching control circuit triggers the power switch. It shows that the converter operates in CCMVS with a switching frequency of 66 kHz. As load decreases from 85 W to 22 W, on-time $T_{on\,DCM}$ is fixed at 1.2 μs, and T_p increases from 8.6 μs to 10.5 μs. So the secondary current I_s falls to zero before T_p expires, as shown in Fig.7. Signal V cannot trigger the power switch until T_p expires. As a result, the converter operates in DCM with a switching frequency of 81 kHz. Fig.8a shows the results at an extremely light load of 6 W. The load regulation is achieved by the control of the burst comparator, with a switching frequency of about 2 kHz. Fig.8b shows the details of pulses during burst on, where T_p is fixed at 25.6 μs and $T_{on\,burst}$ is 2.8 μs. The test results at different loads show that the converter successfully achieves multi-mode control as expected.

It is worth noting that during transition between DCM and burst mode, hysteresis must be introduced to improve the noise immunity. Otherwise the converter would operate arbitrarily in DCM or burst mode at the boundary of the two modes and result in instability (Chen *et al*., 2007). In this design, on-time in burst and DCM modes is 2.8 μs and 1.2 μs, respectively. Thus there is a hysteresis of load current between bidirectional transitions of the two modes. The transition points are 0.5 A and 2 A respectively in testing. It guarantees high reliability during mode transition.

Figs.6 and 7 show that besides multi-mode operation, accurate valley detection is realized as well. However, there is a time delay of about 400 ns before the power switch is turned on. This is due to the propagation delay in the controller and the turn-on time of the power switch. Optimization of the delay will enable the converter to turn on the power switch in the resonance valley with the minimum voltage, $V_{IN}-N(V_O+V_R)$ in CCMVS. In the design, the turning ratio N is 4.2. So the achievable minimum voltage is

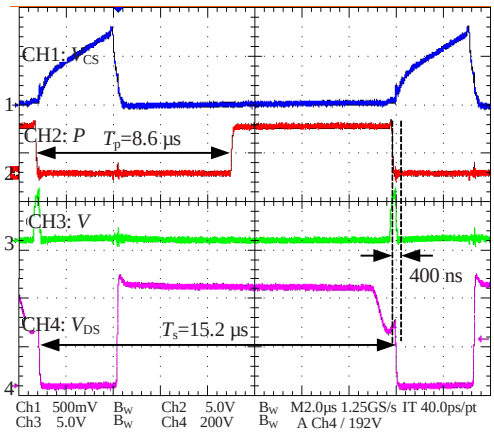


Fig.6 CCMVS operation with I_O=4.25 A, f_s=66 kHz

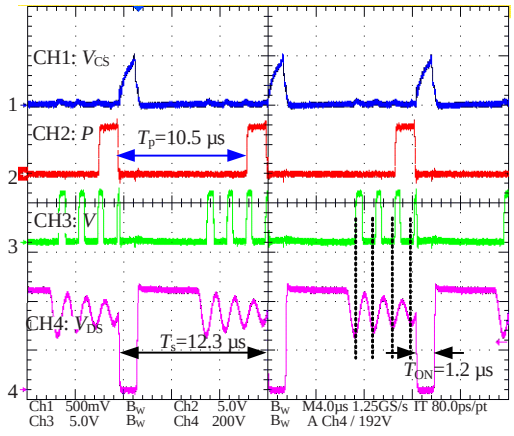
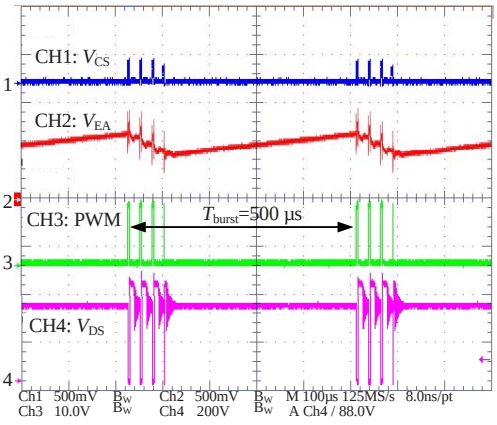
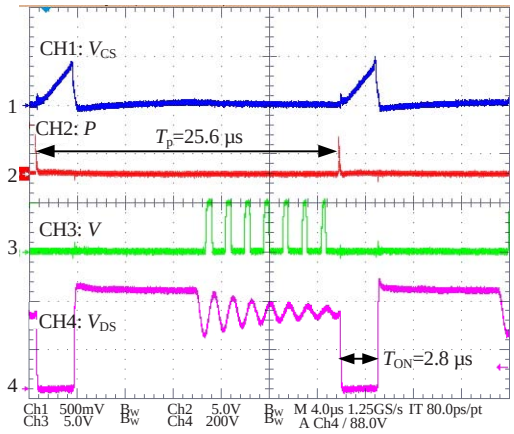


Fig.7 DCM operation with I_O=1.1 A, f_s=81 kHz



(a)



(b)

Fig.8 Burst mode operation. (a) Burst on/off operation with I_O=0.3 A, f_{burst}=2 kHz; (b) Burst on period with I_O= 0.3 A, f_s=39 kHz

about 220 V, which is still a little high. However, it could be reduced for further improvement of efficiency by increasing N. But a high-cost power switch with higher voltage tolerance should be chosen. So there is a tradeoff between efficiency and cost.

Fig.9 shows the waveforms in standby mode. Note that V_O is AC-coupled. The converter operates in the burst mode, and the total power consumption is 0.3 W, which meets the standby power requirements of various organizations and projects, such as 1 W initiative, energy star and blue angel. Fig.10 shows the load regulation of the converter, with only 10 mV variation in the load range of 0~4.5 A. Fig.11 shows the soft start procedure of the converter, with 50 ms startup time and less than 1 V output overshoot.

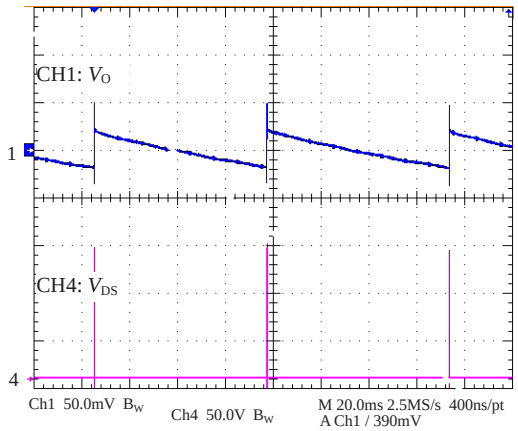


Fig.9 Waveforms in standby mode

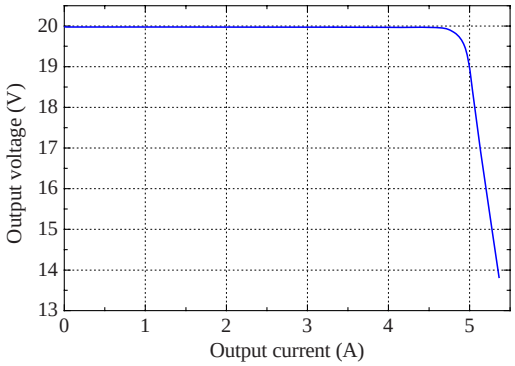


Fig.10 Load regulation of the converter

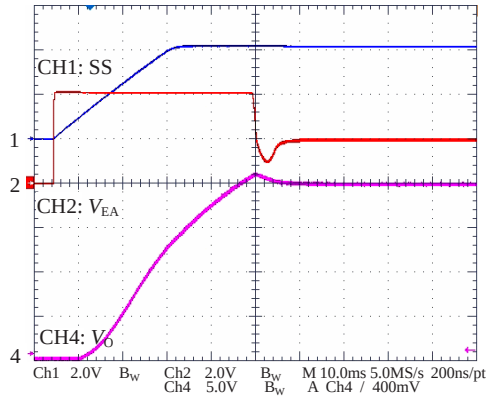


Fig.11 Waveforms during soft start

Note that $T_{p\,min}$ and $T_{p\,max}$ in testing are 8.6 μs and 25.6 μs respectively, and both of them deviate from the specifications, which are 8.3 μs and 25 μs, respectively. The deviation is caused by process variation, but it does not affect system performance seriously. In addition, if necessary, it can be easily eliminated by trimming.

Switching frequency

The experimental switching frequency is plotted in Fig.12. In the load range A (40~100 W), the converter operates in CCMVS, and the switching frequency increases from 55 to 120 kHz as the output power decreases. In the load range B (10~40 W), the converter operates in DCM with fixed on-time and variable off-time. The frequency decreases from 120 to 40 kHz at 10 W. If the load is reduced below 10 W, the converter operates in the range C with burst mode control. The burst off duration increases as the load decreases. Thus, the converter can regulate the output voltage even at no load as shown in Fig.9. The experimental frequency variation according to load condition is consistent with the theoretical predictions. The power consumption curve of the controller, including the gate driver, is also plotted. It is shown that the power consumption is well controlled under different load conditions for that it is related to the switching frequency.

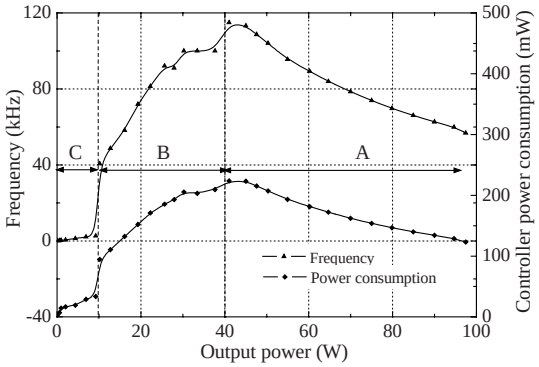


Fig.12 Relationship between frequency, power consumption and load of the converter

Conversion efficiency

The conversion efficiency of the proposed design is shown in Fig.13, together with the conversion efficiency of conventional design. The conventional design with variable frequency control over the entire load range suffers from efficiency degradation with load decreasing. By comparison, the proposed design achieves a high efficiency of over 80% from full load down to 2.5 W, with a peak of 88.8%. Optimizing the switching frequency and soft switching, we can reduce the transition power loss related to power switch over the entire load range and thus achieve high conversion efficiency.

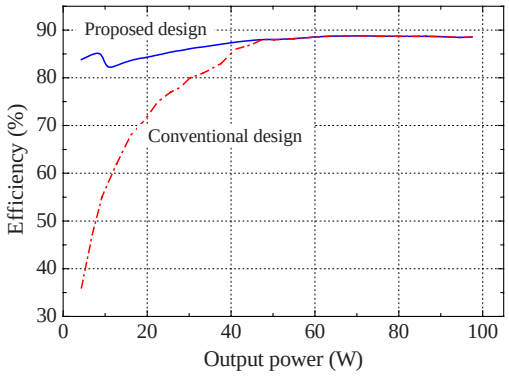


Fig.13 Comparison of conversion efficiency of the proposed and the conventional design

Performance summary

Table 2 summarizes the main performance of the converter design. The converter features excellent load regulation and high efficiency as well as low standby power consumption.

Table 2 Performance summary of the converter

Parameter	Value	Parameter	Value
V_{in}	310 V	Start up overshoot	1V
V_O	20 V	Standby power consumption	300 mW
I_O	0~4.5 A	Efficiency*	>80%
Load regulation	10 mV		

* For I_O=0.125~4.5 A

CONCLUSION

This study is devoted to a multi-mode control scheme for soft-switched flyback converter. CCMVS is employed at heavy load to realize soft switching, reducing turn-on loss of power switch as well as EMI; at light load, the converter operates in DCM with valley switching and AOT, and successfully limits the switching frequency range and maintains load regulation; at extremely light load or in standby mode, both switching frequency and static power dissipation of the controller are reduced through burst mode operation.

The scheme maintains good control over the switching frequency so that high efficiency and excellent load regulation can be achieved over the whole load range including heavy, medium, light load as well as standby mode. To realize the proposed control scheme, a monolithic controller circuit is designed, with a VCO for multi-mode control and an accurate valley switching control circuit. The controller IC was fabricated in a 1.5-μm BiCMOS process and applied to a 310 V/20 V, 90 W flyback DC/DC converter. Experimental results successfully verified the merits of the proposed design. The flyback converter achieves a high efficiency of over 80% from full load down to 2.5 W, with the maximum reaching 88.8%, while the total power consumption in standby mode is about 300 mW.

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