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A sensorless and simple controller for VSC based HVDC systems

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Abstract: Voltage source converter high-voltage direct current (VSC-HVDC) is a new power transmission technology preferable in small or medium power transmission. In this paper we discuss a new control system based on space vector modulation (SVM) without any voltage line sensors. Using direct power control (DPC) SVM and a new double synchronous reference frame phase-locked loop (DSRF-PLL) approach, the control system is resistant to the majority of line voltage disturbances. Also, the system response has accelerated by using a feed forward power decoupled loop. The operation of this control strategy was verified in a SIMULINK/MATLAB simulation environment. To validate this control system, a 5 kV·A prototype system was constructed. Compared to the original controllers, the current total harmonic distortion (THD), the active and reactive deviations and the DC voltage overshoot were lowered by 2.5%, 6.2% and 8%, respectively. The rectifier power factor in the worst condition was 0.93 and the DC voltage settling time was 0.2 s.

Key words: Voltage source converter high-voltage direct current (VSC-HVDC), Space vector modulation (SVM), Direct power control (DPC), HVDC Light

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INTRODUCTION

Voltage source converter high-voltage direct current (VSC-HVDC), controlled by pulse width modulation (PWM), can supply power to both active and passive electrical systems. The introduction of VSC and PWM makes possible fast and flexible control of power flow and more convenient operation of power systems. Besides, this advancement, compared with conventional HVDC, mitigates harmonics in AC current and AC voltage greatly and improves power factors of the connected AC systems (Li GK *et al.*, 2005). VSC-HVDC or HVDC Light, in recent years, have successfully been commercially commissioned in such fields as supplying power to remote isolated loads, empowering urban centers, connecting distributed generation sources, linking two asynchronous electrical power systems, improving power quality, and so on (Asplund, 2000; Li *et al.*, 2003).

The advantages of a VSC based HVDC system are (Asplund, 2000): (1) only a small filter is required to filter high frequency signal components; (2) there is no commutation failure problem; (3) reactive power compensation is not required; (4) there is no restriction on multiple in-feeds; etc.

There are various control methods for VSC based HVDC systems. Zhang *et al.*(2002) used the inverse steady state model controller to trace the operating point and adopted two decoupled controlling loops to eliminate the steady state deviation. Chen *et al.*(2004) proposed a steady-state controller design scheme based on dq0-axis. Zhang *et al.*(2002) and Chen *et al.*(2004) assumed that the two terminals of VSC-HVDC have been connected to an infinite bus system. But one terminal of VSC-HVDC may be connected to a generator and, as in Asplund *et al.* (1997), an HVDC Light system connects the generator (such as an offshore wind farm) to the grid. These strategies focus on control of the HVDC system itself and do not consider the interaction between AC and DC systems. Hu *et al.*(2004) presented an optimal coordinated control strategy between the

generator excitation and VSC-HVDC, whereas the derivation of control law is complicated. Hu *et al.* (2005) applied a genetic algorithm (GA) to optimize parameters of the controller after determining them. Ooi and Wang (1991) and Zhang and Xu (2001) used a phase and amplitude control (PAC) technique for VSC based HVDC applications. Li GI *et al.*(2005) proposed a nonlinear control for an HVDC Light system. These methods have used voltage and current sensors.

A direct power control (DPC) strategy based on virtual flux, called VF-DPC, provides sinusoidal line current, lower harmonic distortion, a simple and noise-robust power estimation algorithm and good dynamic response (Rahmati *et al.*, 2006). However, the VF-DPC scheme has the following well-known disadvantages (Malinowski *et al.*, 2001; 2004): (1) variable switching frequency (difficulties of LC input filter design), (2) high sampling frequency needed for digital implementation of hysteresis comparators, (3) necessity for a fast microprocessor and A/D converters.

Therefore, there is no tendency to implement VF-DPC in industry. All the above drawbacks can be eliminated when, instead of the switching table, space vector modulation (SVM) is applied.

DPC is a method based on instantaneous direct active and reactive power control (Malinowski *et al.*, 2004). In DPC there are no internal current control loops and no PWM modulator block. Moreover, the turn-on and turn-off commands of the static switches of the converters are generated by SVM. Use of space vector modulation causes lower current harmonics, relatively high regulation and stability of output voltage and obtains a higher modulation factor relative to sinusoidal modulation (Malinowski *et al.*, 2004). Also, it can easily be implemented in a DSP based system.

Double synchronous reference frame phase-locked loop (DSRF-PLL) based on VF causes this control system to be resistant to the majority of line voltage disturbances. This assures proper operation of the system for abnormal and failure grid conditions.

In this paper a new control strategy is proposed for VSC-HVDC. In this strategy, the reactive power and output DC voltage in the rectifier station and the reactive and active powers in the inverter station are controlled, separately. Also, the DPC rectifier equations (Malinowski *et al.*, 2004) have been developed for the inverter. For more accuracy in high power, the second order parameter is included in the rectifier and the inverter equations. Active and reactive power feed forward decoupling are used for accelerating the system response. Finally, DPC is applied to the rectifier and inverter stations of VSC-HVDC.

The operation of this control strategy is verified in a SIMULINK/MATLAB simulation environment for steady state, active and reactive power variations, single-line-to-ground faults and unbalanced sources at the rectifier and the inverter stations. Also, this control strategy is applied to a 5 kV·A prototype system which is verification that this control strategy has a fast response and strong stability.

CONTROL of VSC BASED HVDC SYSTEM

VSC based HVDC system

VSC-HVDC involves two voltage source converters with the same configuration, linking with a dc transmission line or cable (Fig.1). There are four control variables represented by U_{dcr}, q_{r}, p_{i} and q_{i} for this system. In this paper, a rectifier station is chosen to control DC-bus output voltage of rectifier (U_{dcr}). Also, reactive power (q_{r}) and inverter station are set to control active power (p_{i}) and also reactive power (q_{i}). R_{c} is the equivalent resistance of the transmission cable and can be practically neglected. Thus we may write $U_{\mathrm{dcr}} \approx U_{\mathrm{dci}} = U_{\mathrm{dc}}$.

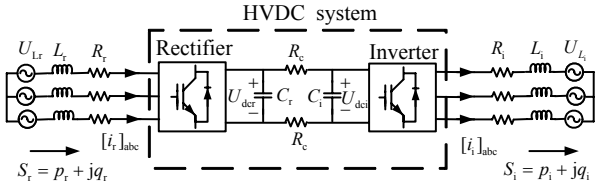

Fig.1 A physical model for a VSC based HVDC system

Virtual-flux estimator for rectifier and inverter

From the economical point of view, and for simplicity, more reliability and separation of power stage and control, AC line voltage sensors are replaced by a flux estimator (Malinowski *et al.*, 2004).

The basic model of a VSC station is shown in Fig.2. If D_{a}, D_{b}, and D_{c} are the duty cycles of S_{a}, S_{b}, and S_{c} signals, respectively, U_{dc} is the converter DC voltage, and $u_{\mathrm{L}\alpha}$ and $u_{\mathrm{L}\beta}$ are line voltage in α-β coordinates, then the related flux of AC voltage, $\boldsymbol{\Psi}_{\mathrm{L}}$, can be written as (Malinowski *et al.*, 2004)

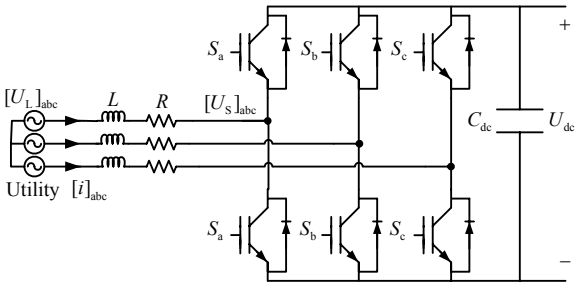

Fig.2 Basic model of a voltage source converter

$$\boldsymbol{\Psi}_{\mathrm{L}}=\begin{bmatrix}\Psi_{\mathrm{L}\alpha}\\ \Psi_{\mathrm{L}\beta}\end{bmatrix}=\begin{bmatrix}\int u_{\mathrm{L}\alpha}\mathrm{d}t\\ \int u_{\mathrm{L}\beta}\mathrm{d}t\end{bmatrix}. \tag{1}$$

Also, the converter voltage equations in α-β coordinates are:

$$u_{\mathrm{S}\alpha}=\sqrt{\frac{2}{3}}U_{\mathrm{dc}}\left[D_{\mathrm{a}}-\frac{1}{2}(D_{\mathrm{b}}+D_{\mathrm{c}})\right], \tag{2}$$

$$u_{\mathrm{S}\beta}=\frac{1}{\sqrt{2}}U_{\mathrm{dc}}(D_{\mathrm{b}}-D_{\mathrm{c}}). \tag{3}$$

Direct power control

Active and reactive power in the rectifier and the inverter stations are estimated using the line current vectors ($i_{\mathrm{L}\alpha}$, $i_{\mathrm{L}\beta}$) and estimated virtual flux ($\Psi_{\mathrm{L}\alpha}$, $\Psi_{\mathrm{L}\beta}$) in α-β coordinates (Malinowski *et al.*, 2004):

$$p=\omega(\psi_{\mathrm{L}\alpha}i_{\mathrm{L}\beta}-\psi_{\mathrm{L}\beta}i_{\mathrm{L}\alpha}), \tag{4}$$

$$q=\omega(\psi_{\mathrm{L}\alpha}i_{\mathrm{L}\alpha}+\psi_{\mathrm{L}\beta}i_{\mathrm{L}\beta}). \tag{5}$$

Rectifier control design

The full control algorithm of the proposed control system is presented in Fig.3. The DPC-SVM uses closed-loop power control. In the rectifier station, reference reactive power (q_{refr}) is set to zero for unity-power-factor operation. In an ideal case, the active power in the rectifier station and the active power in the inverter station are equal, and no storage elements are needed. Nevertheless, in real systems differences between these active powers are inevitable, and these differences are absorbed by the DC link capacitor and are reflected in fluctuations of the DC link voltage. Thus, the reference active power (p_{refr}) at the side of the rectifier is the sum of the outer proportional-integral (PI) dc voltage controller and estimated active power in the inverter station (p_{i}).

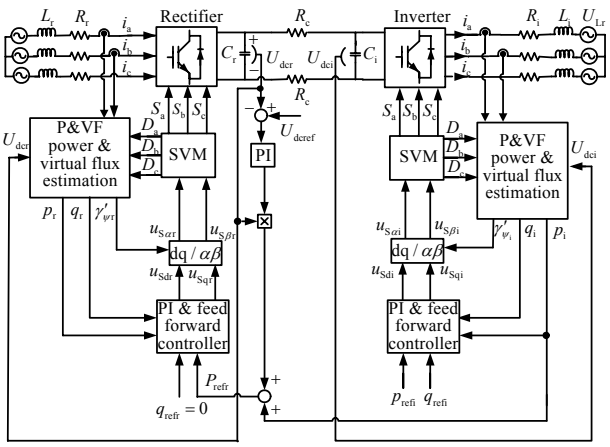

Fig.3 Control scheme for a VSC based HVDC system with the rectifier and inverter stations

According to the current direction, the line voltage $\boldsymbol{u}_{\mathrm{Lr}}$ can be expressed as the sum of the inductor voltage $\boldsymbol{u}_{\mathrm{Ir}}$, the resistor voltage $\boldsymbol{u}_{\mathrm{Rr}}$ and the rectifier voltage $\boldsymbol{u}_{\mathrm{Sr}}$ (Rahmati *et al.*, 2006):

$$\boldsymbol{u}_{\mathrm{Lr}}=\boldsymbol{u}_{\mathrm{Sr}}+\boldsymbol{u}_{\mathrm{Ir}}+\boldsymbol{u}_{\mathrm{Rr}}. \tag{6}$$

By considering Eq.(1), the estimated virtual fluxes are:

$$\psi_{\mathrm{Lr}\alpha(\mathrm{est})}=\int(u_{\mathrm{Sr}\alpha}+R_{\mathrm{r}}i_{\alpha})\mathrm{d}t+L_{\mathrm{r}}i_{\alpha}, \tag{7}$$

$$\psi_{\mathrm{Lr}\beta(\mathrm{est})}=\int(u_{\mathrm{Sr}\beta}+R_{\mathrm{r}}i_{\beta})\mathrm{d}t+L_{\mathrm{r}}i_{\beta}. \tag{8}$$

Inverter control design

In the inverter station, reference reactive power (q_{refi}) and reference active power (p_{refi}) are set to network demand. According to the current direction, the inverter voltage $\boldsymbol{u}_{\mathrm{Si}}$ can be expressed as the sum of the inductor voltage $\boldsymbol{u}_{\mathrm{Ii}}$, the resistor voltage $\boldsymbol{u}_{\mathrm{Ri}}$ and the line voltage $\boldsymbol{u}_{\mathrm{Li}}$ at the side of the inverter. The estimated virtual fluxes are (Rahmati *et al.*, 2006):

$$\psi_{\mathrm{Li}\alpha(\mathrm{est})}=\int(u_{\mathrm{Si}\alpha}-R_{\mathrm{i}}i_{\alpha})\mathrm{d}t-L_{\mathrm{i}}i_{\alpha}, \tag{9}$$

$$\psi_{\mathrm{Li}\beta(\mathrm{est})}=\int(u_{\mathrm{Si}\beta}-R_{\mathrm{i}}i_{\beta})\mathrm{d}t-L_{\mathrm{i}}i_{\beta}. \tag{10}$$

DSRF-PLL

Further improvements regarding DPC operation can be achieved by using careful sector detection with a PLL generator instead of a zero crossing voltage detector to guarantee a very stable and also disturbance free sector detection, even under operation with

distorted and unbalanced line voltages (Cichowlas *et al.*, 2005; Rodriguez *et al.*, 2005). In this case, a DSRF-PLL based on VF is used.

When the utility voltage is unbalanced, the VF estimated can be expressed on the α-β stationary reference frame as (Rodriguez *et al.*, 2005)

$$\boldsymbol{\Psi}_{(\alpha\beta)}=\boldsymbol{\Psi}^{+}+\boldsymbol{\Psi}^{-}=\left|\boldsymbol{\Psi}^{+}\right|\begin{bmatrix}\cos\gamma_{\psi}\\ \sin\gamma_{\psi}\end{bmatrix}+\left|\boldsymbol{\Psi}^{-}\right|\begin{bmatrix}\cos\gamma_{\psi}\\ -\sin\gamma_{\psi}\end{bmatrix}. \tag{11}$$

The virtual flux angle is

$$\gamma_{\psi}=\arctan(\psi_{\beta}/\psi_{\alpha}). \tag{12}$$

This VF vector is expressed on the double reference frame as shown in Fig.4. In this double reference frame, the d^+ and d^- axes are synchronized with $\boldsymbol{\Psi}^{+}$ and $\boldsymbol{\Psi}^{-}$, respectively. Also, dq^+ rotates in the positive direction and its angular position is γ'_{ψ}, and dq^- rotates in the negative direction and its angular position is $-\gamma'_{\psi}$. The expressions of $\boldsymbol{\Psi}$ on these reference frames are:

$$\boldsymbol{\Psi}_{(dq^{+})}=\begin{bmatrix}\psi_{d}^{+}\\ \psi_{q}^{+}\end{bmatrix}=\boldsymbol{T}_{dq}{}^{+}\boldsymbol{\Psi}_{(\alpha\beta)}=\begin{bmatrix}\cos\gamma'_{\psi} & \sin\gamma'_{\psi}\\ -\sin\gamma'_{\psi} & \cos\gamma'_{\psi}\end{bmatrix}\boldsymbol{\Psi}_{(\alpha\beta)}, \tag{13}$$

$$\boldsymbol{\Psi}_{(dq^{-})}=\begin{bmatrix}\psi_{d}^{-}\\ \psi_{q}^{-}\end{bmatrix}=\boldsymbol{T}_{dq}{}^{-}\boldsymbol{\Psi}_{(\alpha\beta)}=\begin{bmatrix}\cos\gamma'_{\psi} & -\sin\gamma'_{\psi}\\ \sin\gamma'_{\psi} & \cos\gamma'_{\psi}\end{bmatrix}\boldsymbol{\Psi}_{(\alpha\beta)}. \tag{14}$$

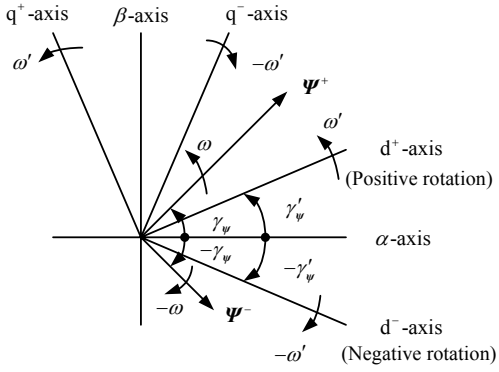

Fig.4 Representation of the flux vectors and reference axes

Using a PLL structure and adjusting properly its control parameters, it is possible to achieve $\gamma'_{\psi}\approx\gamma_{\psi}$. The selection of these PLL control parameters is based on a small signal analysis in which $\sin(\gamma_{\psi}-\gamma'_{\psi})\approx\gamma_{\psi}-\gamma'_{\psi}$, $\cos(\gamma_{\psi}-\gamma'_{\psi})\approx 1$ and $(-\gamma_{\psi}-\gamma'_{\psi})\approx -2\gamma_{\psi}$ are assumed. So, the flux components of Eqs.(11), (13) and (14) can be approximated by (Rodriguez *et al.*, 2005)

$$\psi_{d}{}^{+}\approx|\boldsymbol{\Psi}^{+}|+|\boldsymbol{\Psi}^{-}|\cos(2\gamma'_{\psi})-|\boldsymbol{\Psi}^{-}|(\gamma_{\psi}-\gamma'_{\psi})\sin(2\gamma'_{\psi}), \tag{15}$$

$$\psi_{d}{}^{-}\approx|\boldsymbol{\Psi}^{-}|+|\boldsymbol{\Psi}^{+}|\cos(2\gamma'_{\psi})-|\boldsymbol{\Psi}^{+}|(\gamma_{\psi}-\gamma'_{\psi})\sin(2\gamma'_{\psi}), \tag{16}$$

$$\psi_{q}{}^{+}\approx|\boldsymbol{\Psi}^{+}|(\gamma_{\psi}-\gamma'_{\psi})-|\boldsymbol{\Psi}^{-}|\sin(2\gamma'_{\psi})-|\boldsymbol{\Psi}^{-}|(\gamma_{\psi}-\gamma'_{\psi})\cos(2\gamma'_{\psi}), \tag{17}$$

$$\psi_{q}{}^{-}\approx-|\boldsymbol{\Psi}^{-}|(\gamma_{\psi}-\gamma'_{\psi})+|\boldsymbol{\Psi}^{+}|\sin(2\gamma'_{\psi})+|\boldsymbol{\Psi}^{+}|(\gamma_{\psi}-\gamma'_{\psi})\cos(2\gamma'_{\psi}). \tag{18}$$

In Eqs.(15)~(18), the constant values in the d^+-q^+ and d^--q^- axes correspond to the amplitude of $\boldsymbol{\Psi}^{+}$ and $\boldsymbol{\Psi}^{-}$, respectively, and oscillations with 2ω frequency appear as a consequence of the coupling between axes and vectors in opposite rotating direction. This low-frequency oscillation could be attenuated by means of a low-pass filter (LPF). But the dynamic response of the detection system would be too slow. To cancel these oscillations, a decoupling network (DN) is presented and described in the subsequent section. This DN obtains accurate results about the amplitude of $\boldsymbol{\Psi}^{+}$ and $\boldsymbol{\Psi}^{-}$. Therefore, the dynamic response of the detection system is improved.

1. Decoupling signals in the DSRF

In Eqs.(15) and (16), the amplitude of the signal oscillation in the d^+-q^+ axes depends on the mean value of the signal in the d^--q^- axes, and vice versa. To cancel the oscillations in the d^+-q^+ axes signals, the decoupling cell (DC) shown in Fig.5a is proposed. To cancel the oscillations in the d^--q^- axes signals, the same structure of the DC can be used but swapping '–' and '+' in the variables. Logically, for a correct operation of both DC's it is necessary to design some mechanism to determine the value of $\Psi_{d}{}^{+}$, $\Psi_{q}{}^{+}$, $\Psi_{d}{}^{-}$ and $\Psi_{q}{}^{-}$.

Keeping this goal in mind, the DN shown in Fig.5b is proposed. In this DN, the LPF block is a

low-pass filter (LPF(s)=$\omega_f/(s+\omega_f)$). The rate between the cut-off frequency of the LPF and the fundamental utility frequency (ω_f/ω) is defined as k. The higher the value assigned to k, the faster the response. Nevertheless, it is necessary to note that the transitory error in the system response will also be higher, which can give rise to unstable behavior of the detection system. This justifies why the value of k should not be too high, in order to reduce oscillations in the response, and makes the detection system more stable. This constraint in the maximum value of k is even more important when the utility voltages not only present an imbalance at the fundamental frequency but also high order harmonics. It seems logical to establish $k=1/\sqrt{2}$, since the dynamic response is fast enough and oscillations do not appear in the amplitude estimation of $\boldsymbol{\Psi}^+$.

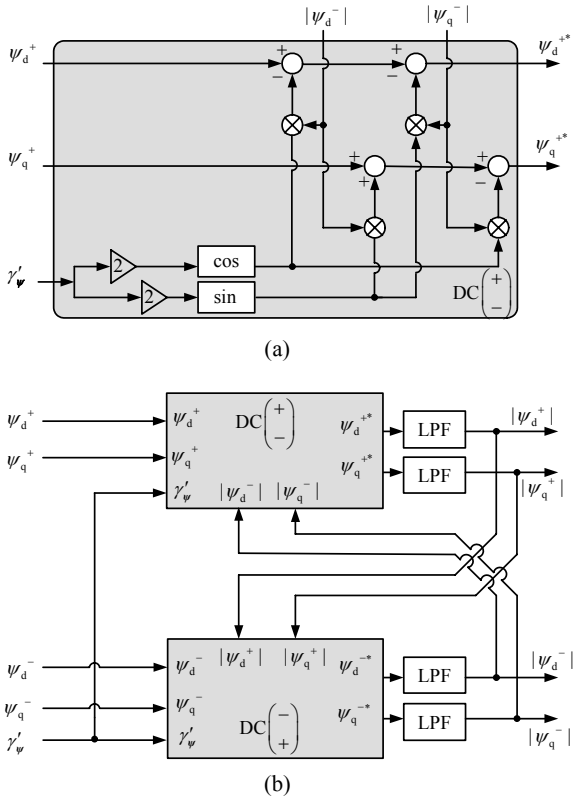

Fig.5 (a) Decoupling cell for cancelling the effect of ψ on the d^+-q^+ frame signals; (b) Decoupling network of d^+-q^+ and d^--q^- reference frames

The block diagram of the DSRF-PLL is shown in Fig.6. The tuning parameter for LPF is $k=1/\sqrt{2}$, and for PI controller the proportional and integral coefficients are k_p=2.22 and k_i=246.7, respectively. The selection of k_p and k_i is based on small signal analysis as reported in Rodriguez *et al.*(2002).

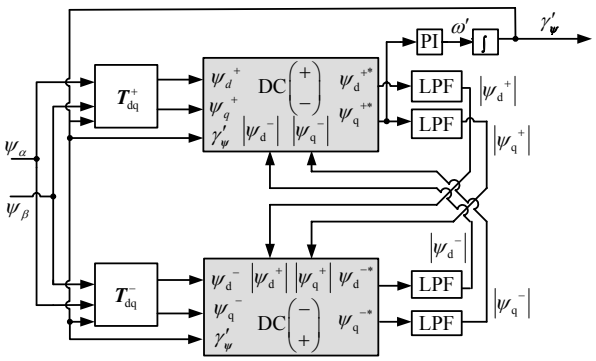

Fig.6 Block diagram of the DSRF-PLL

The virtual flux angle γ'_ψ is modified using DSRF-PLL and used for careful sector detection. The block diagram of the power and virtual flux estimator is shown in Fig.7.

Feed forward decoupled loop

The system response or dynamic behavior of the system can be accelerated by using a feed forward current decoupled loop. According to the following equations, instead of AC current feed forward decoupling, active and reactive power feed forward decoupling can be used for the converters.

Instantaneous active and reactive power in d-q coordinates can be expressed as (Song *et al.*, 2005)

$$p=u_{Ld}i_{Ld}+u_{Lq}i_{Lq}, \tag{19}$$

$$q=-u_{Lq}i_{Ld}+u_{Ld}i_{Lq}, \tag{20}$$

where u_{Ld} and u_{Lq} are the d- and q-axis components of the AC source voltage, respectively, and i_{Ld} and i_{Lq} are the d- and q-axis currents of the AC source voltage, respectively.

In the analysis, we align the d-q axis in such direction that the q-axis is in phase with the AC source voltage, i.e., $u_{Lq}=U_L=\sqrt{3/2}U_{Lm}$ and u_{Ld}=0. So, Eqs.(19) and (20) can be rewritten as

$$p=U_L i_{Lq}=\sqrt{3/2}U_{Lm}i_{Lq}, \tag{21}$$

$$q=-U_L i_{Ld}=-\sqrt{3/2}U_{Lm}i_{Ld}, \tag{22}$$

where u_{Lm} is the peak of the AC source voltage.

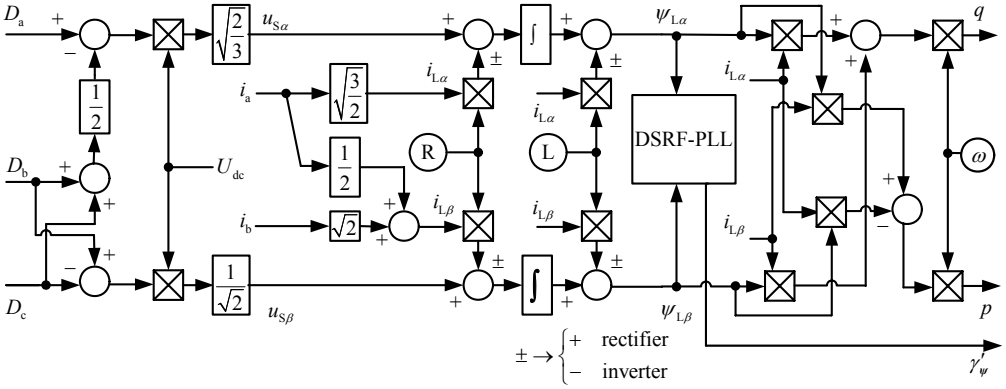

Fig.7 Block diagram of power and virtual flux (P&VF) estimator

According to Eqs.(21) and (22), the active and reactive powers are controlled by i_{Lq} and i_{Ld}, respectively.

For the rectifier (Fig.2), there are the following voltage equations in the d-q synchronous frame (Song *et al.*, 2005):

$$\begin{aligned} u_{Sd} &= -Ri_{Ld} - L\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t} + L\omega i_{Lq} + u_{Ld} \\ &= -Ri_{Ld} - L\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t} + L\omega i_{Lq}, \end{aligned} \tag{23}$$

$$\begin{aligned} u_{Sq} &= -Ri_{Lq} - L\frac{\mathrm{d}i_{Lq}}{\mathrm{d}t} - L\omega i_{Ld} + u_{Lq} \\ &= -Ri_{Lq} - L\frac{\mathrm{d}i_{Lq}}{\mathrm{d}t} - L\omega i_{Ld} + U_L. \end{aligned} \tag{24}$$

u_{Sd} and u_{Sq} are the converter voltages in d-q coordinates. R and L represent the equivalent resistance and inductance, respectively, and ω is the source angular frequency.

According to Eqs.(21) and (22), active and reactive power feed forward decoupling instead of AC current feed forward decoupling can be used for the converters. Note that the power loop uses two PI regulators in the rotation frame in these approaches. Now, assume that the VSC output voltage is determined by the following PI controller:

$$u_{Sd} = \left(K_P + \frac{K_I}{s}\right)(q_{ref} - q) + \frac{L\omega}{\sqrt{3/2}U_{Lm}}p, \tag{25}$$

$$u_{Sq} = -\left(K_P + \frac{K_I}{s}\right)(p_{ref} - p) + \frac{L\omega}{\sqrt{3/2}U_{Lm}}q + U_L, \tag{26}$$

where K_P and K_I are proportional and integral gains, respectively.

The q-axis components of the AC source voltage (u_{Lq}=U_L) are treated as a constant perturbation that must be compensated by the integral parts of the PI controllers (Li *et al.*, 2006).

Similarly, in the inverter station,

$$u_{Sd} = -\left(K_P + \frac{K_I}{s}\right)(q_{ref} - q) - L\omega i_{Lq}, \tag{27}$$

$$u_{Sq} = \left(K_P + \frac{K_I}{s}\right)(p_{ref} - p) + L\omega i_{Ld} + U_L. \tag{28}$$

Both VSC stations in VSC-HVDC use this power control strategy to improve the system response speed.

Fig.8 shows the structure of PI and feed forward controller for the rectifier and the inverter stations.

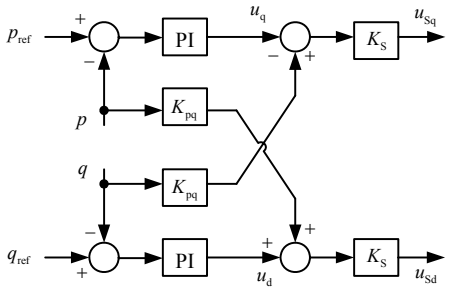

Fig.8 PI and feed forward controller

$K_{pq} = L\omega / (\sqrt{3/2}U_{Lm})$, K_S=1 for the rectifier and K_S=−1 for the inverter

Space vector modulation

At the rectifier station (Fig.3), the DC voltage and reactive power are controlled. To satisfy the unity power factor, the reference reactive power must be adjusted to zero. As mentioned before, the reference

active power (p_{refr}) is the sum of the outer PI DC voltage controller and estimated active power in the inverter station (p_i).

The active and reactive powers are controlled in the inverter station. Reference active and reactive powers at the side of the inverter are adjusted by network demand.

Then the commanded reactive power (q_{ref}) and active power (p_{ref}) values are compared with the estimated q and p values, respectively. The errors are delivered to the PI and feed forward controllers, which eliminate the steady state error and finally generate output signals u_{Sd} and u_{Sq}. The output signals from the PI and feed forward controllers after transformation to $u_{S\alpha}$ and $u_{S\beta}$ are delivered to the SVM block. D_a, D_b, D_c, S_a, S_b and S_c are the outputs of SVM.

SIMULATION RESULTS

The operation of this control strategy was verified in a SIMULINK/MATLAB simulation environment for steady state and active and reactive power variations at the rectifier and the inverter stations. The parameters of a VSC-HVDC system are presented in Table 1. Some cases were simulated to validate and demonstrate the performance of the proposed control strategy.

Table 1 Simulation parameters

Parameter	Value
Rectifier output DC voltage (kV)	20
Line voltage (kV)	10
Rectifier frequency (Hz)	50
Inverter frequency (Hz)	60
Sampling frequency (kHz)	10
Switching frequency (kHz)	10
Line resistance (Ω)	0.1
Line inductance (mH)	35
DC link capacitor (μF)	470

In case I, this system was simulated using a step change in the inverter reference active and reactive powers for DPC-SVM (Fig.9) and for DPC-SVM with feed forward (Fig.10). To satisfy the unity power factor, the reference active power of the rectifier was set to zero. Estimated active and reactive powers, the power factor and the output DC voltage of the rectifier under the step variation in p_{refi} and q_{refi} (Figs.9 and 10) are shown in Fig.11 for DPC-SVM and in Fig.12 for DPC-SVM with feed forward. Also, in Fig.13 inverter currents are presented.

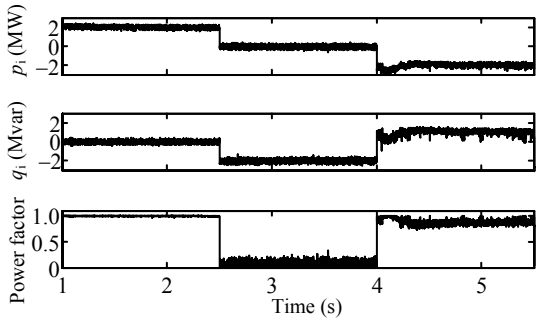

Fig.9 From up to down: step variation of inverter active and reactive powers and power factor in the DPC-SVM algorithm

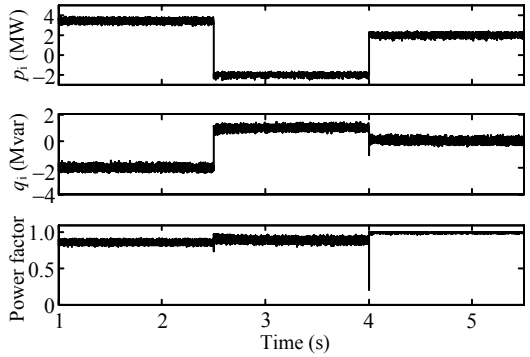

Fig.10 From up to down: step variation of inverter active and reactive powers and power factor in the DPC-SVM with feed forward algorithm

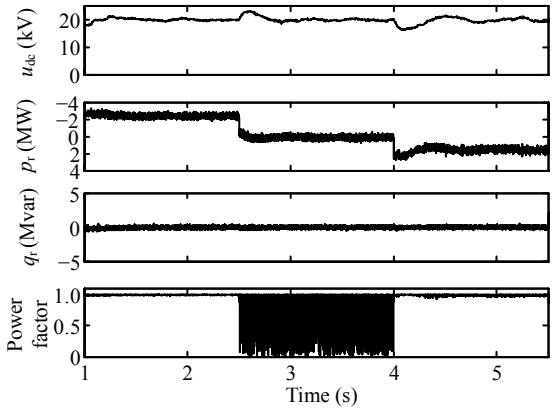

Fig.11 From up to down: rectifier DC voltage, active and reactive powers and power factor in transient state for the DPC-SVM algorithm

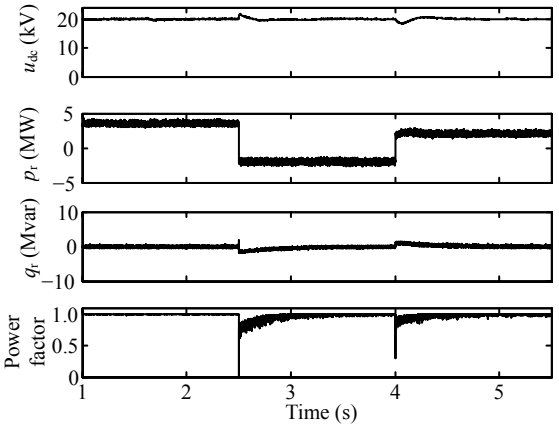

Fig.12 From up to down: rectifier DC voltage, active and reactive powers and power factor in transient state for the DPC-SVM with feed forward algorithm

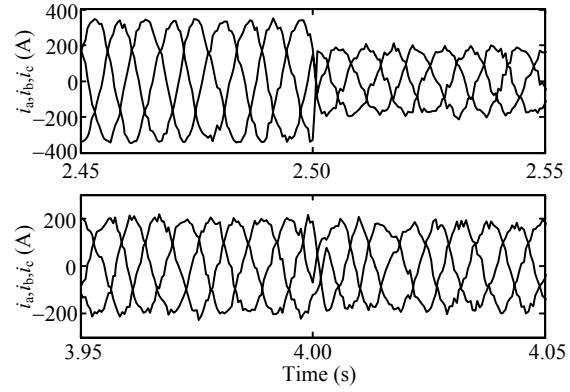

Fig.13 Inverter currents in a transient state

As shown in Figs.9 and 10, $\Delta p(|p-p_{\text{ref}}|)$ and $\Delta q(|q-q_{\text{ref}}|)$ were 14% for the DPC-SVM algorithm and 6.2% for the DPC-SVM with feed forward algorithm. Also, as shown in Fig.11, DC voltage overshoot was 18% for the DPC-SVM algorithm and 8% for the DPC-SVM with feed forward algorithm.

Fig.12 shows that the power factor rose very close to the ideal condition. Furthermore, DC voltage was regulated and the variations of active and reactive powers did not affect each other. Compared to the original controllers (Zhang *et al.*, 2002; Li GI *et al.*, 2005), the DC voltage rose to 1.05 p.u. and after 0.2 s it settled down. The comparison between the DPC-SVM algorithm and the DPC-SVM with feed forward algorithm is presented in Table 2.

In case II, the unbalanced sources were applied to the rectifier and the inverter stations during 0.1 s (from 1 to 1.1 s for the rectifier and 1.5 to 1.6 s for the inverter):

Table 2 Comparison between the DPC-SVM algorithm and the DPC-SVM with feed forward algorithm

Parameter	Value	
	DPC-SVM with feed forward	DPC-SVM
Δp and Δq	6.2%	14%
DC overshoot voltage	8%	18%
Rectifier power factor in the worst conditions	0.93	0.90
DC voltage settling time (s)	0.20	0.35
THD current	2.5%	11%

$$\begin{cases} u_{\text{La}} = U_{\text{Lm}}\sin(\omega t), \\ u_{\text{Lb}} = 1.25U_{\text{Lm}}\sin(\omega t - 2\pi/3), \\ u_{\text{Lc}} = 0.85U_{\text{Lm}}\sin(\omega t + 2\pi/3). \end{cases} \tag{29}$$

Fig.14 shows the rectifier output DC voltage, the rectifier estimated active and reactive powers and the rectifier power factor. As shown in this figure, the DC voltage and the active and the reactive powers were not affected by the unbalanced fault.

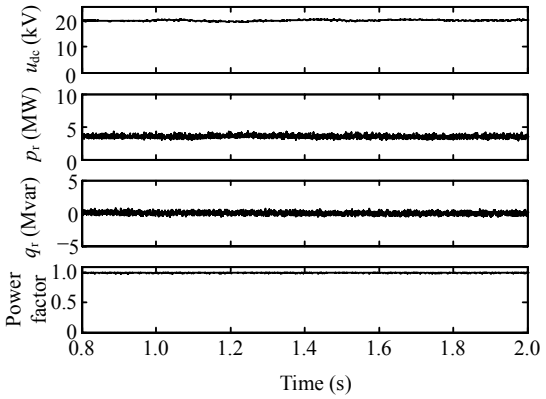

Fig.14 From up to down: rectifier DC voltage, active and reactive powers and power factor in the unbalanced fault

In case III, a single-line-to-ground fault was applied to the rectifier and the inverter stations during 0.1 s (from 1.5 to 1.6 s for the rectifier and 2.5 to 2.6 s for the inverter). As shown in Fig.15, the current in the faulted phase 'a' and also in the other phases was not changed. Fig.16 shows the responses of DC voltage, active and reactive powers at rectifier side. The DC voltage and active powers were increased very little during the fault.

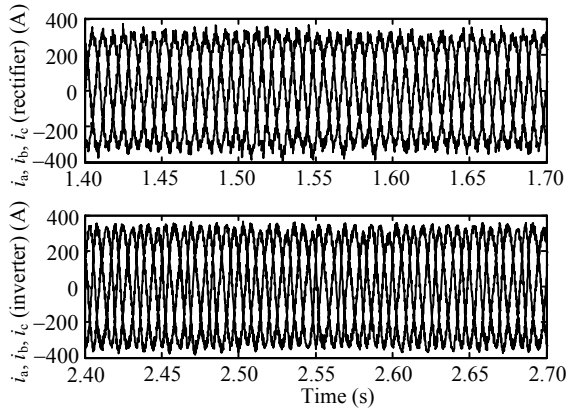

Fig.15 From up to down: rectifier and inverter currents in the single-line-to-ground fault

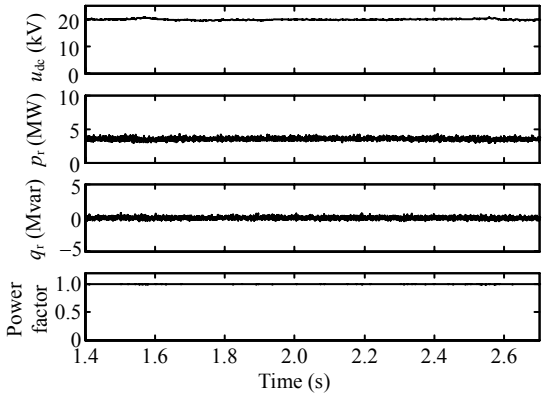

Fig.16 From up to down: rectifier DC voltage, active and reactive powers and power factor in the single-line-to-ground fault

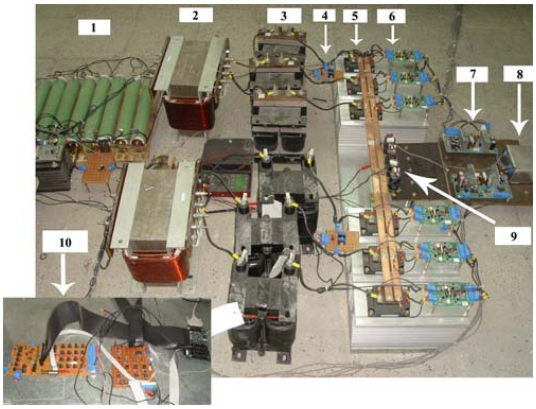

Fig.17 Laboratory setup: 1, load; 2, transformer; 3, inductor; 4, current sensors; 5, IGBTs; 6, IGBT driver; 7, IGBT driver power supply; 8, voltage sensor; 9, capacitors; 10, DSP board

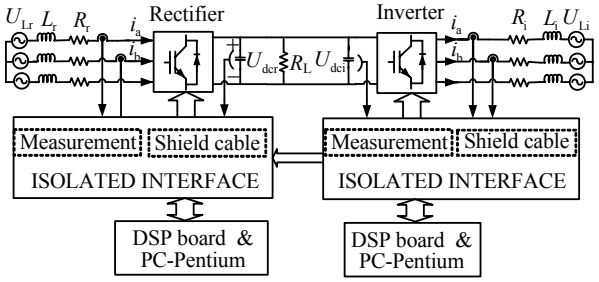

Fig.18 Simplified diagram of laboratory setup

Table 3 Experimental parameters

Parameter	Value
Rectifier output DC voltage (V)	300
Line voltage (V)	110
Rectifier frequency (Hz)	50
Inverter frequency (Hz)	50
Sampling frequency (kHz)	10
Switching frequency (kHz)	10
Line resistance (Ω)	0.1
Line inductance (mH)	16
DC link capacitor (μF)	330
Dead time of switches (μs)	10

EXPERIMENTAL RESULTS

The experimental setup and simplified diagram of laboratory setup (Figs.17 and 18) consisted of a 5 kV·A prototype system and two DSP boards (TMS320F2812-150 MHz), one for the rectifier and the other for inverter stations, which were programmed to implement the DPC-SVM algorithm. Also, two personal computers in the rectifier and inverter stations were used for data acquisition, drawing the output diagram and some calculations needed for the algorithm being used. The experimental parameters are shown in Table 3. The voltage sources at the rectifier and inverter station were distorted sources.

Fig.19 shows rectifier active and reactive powers in a transient state. As shown in Fig.19, the reactive power was close to zero, so the power factor rose very close to the ideal condition. Fig.20 shows the rectifier virtual flux. As shown in Fig.20, SDRL-PLL was efficient for abnormal and grid failure conditions. Figs.21 and 22 show DC output voltage (U_{dcr}) and current (i_a) of the rectifier, respectively. The current THD, the active and reactive deviations and the DC voltage overshoot were lowered by 12%, 16% and 20%, respectively. Also, the rectifier power factor in the worst condition was 0.9 and the DC voltage settling time was 0.3 s.

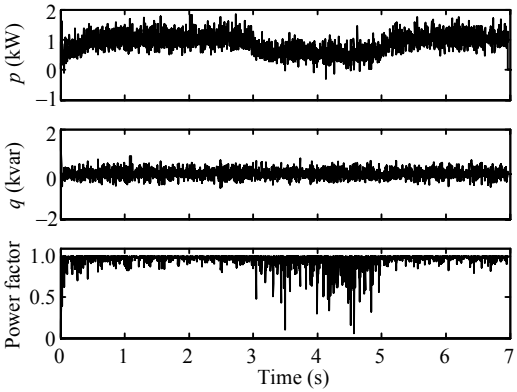

Fig.19 Active and reactive powers of the rectifier

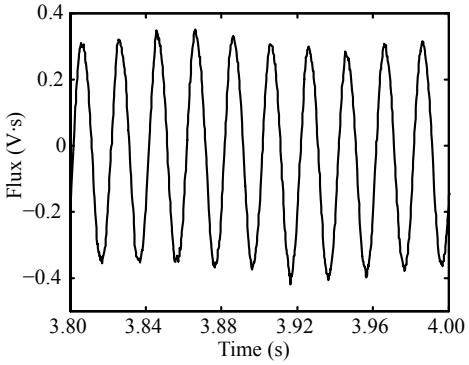

Fig.20 Rectifier virtual flux

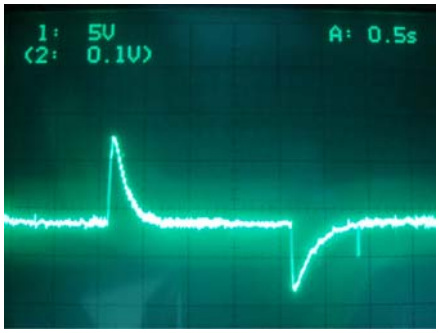

Fig.21 DC output voltage of the rectifier

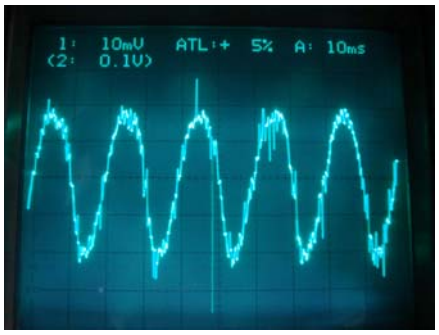

Fig.22 Rectifier current in a transient state

Despite distorted sources and a noisy laboratory environment, all of the results have shown good agreement between simulations and experiments.

CONCLUSION

This paper proposes a new method for controlling a VSC based HVDC system which has been connected between two distribution systems with different frequencies. This method is effective in damping system oscillations quickly, and enhances power quality when power flow is reversed. VF and DSRF-PLL cause this control system to be resistant to the majority of line voltage disturbances.

This method has such advantages as good dynamic response, suitable power quality under abrupt changes in active and reactive powers, a simple power estimation algorithm, sinusoidal line currents and also the unity power factor of the rectifier. Moreover, by this method no line voltage sensors are required.

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