Journal of Zhejiang University SCIENCE A
ISSN 1673-565X (Print); ISSN 1862-1775 (Online)
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Low-leakage diode-triggered silicon controlled rectifier for electrostatic discharge protection in 0.18-μm CMOS process*

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Received July 18, 2008; Revision accepted Oct. 20, 2008; Crosschecked Apr. 27, 2009

Abstract: A diode-triggered silicon controlled rectifier (DTSCR) is being developed as an electrostatic discharge (ESD) protection device for low voltage applications. However, DTSCR leaks high current during normal operation due to the Darlington effect of the triggering-assist diode string. In this study, two types of diode string triggered SCRs are designed for low leakage consideration; the modified diode string and composite polysilicon diode string triggered SCRs (MDTSCR & PDTSCR). Compared with the conventional DTSCR (CDTSCR), the MDTSCR has a much lower substrate leakage current with a relatively large silicon cost, and the PDTSCR has a much lower substrate leakage current with similar area and shows good leakage performance at a high temperature. Other DTSCR ESD properties are also investigated, especially regarding their layout, triggering voltage and failure current.

Key words: Electrostatic discharge (ESD) protection, Diode-triggered silicon controlled rectifier (DTSCR), Leakage current
doi:10.1631/jzus.A0820545 **Document code:** A **CLC number:** TN3; TN4; TN6

INTRODUCTION

Due to the superior electrostatic discharge (ESD) protection capabilities of silicon controlled rectifier (SCR) devices, it has been widely used to protect internal circuits from ESD damage (Liou *et al.*, 2007). But the SCR device still has a high switching voltage (i.e., triggering voltage, as much as 16 V in a 0.18-μm process), which is generally higher than the gate-oxide breakdown voltage of the input stages. The ESD susceptibility of the gate oxide is increasing at a rapid pace as technologies advance to thinner gate oxides. The low triggering voltage SCR called DTSCR was developed (Mergens *et al.*, 2003; 2005) to address the issue of the high triggering voltage problem of breakdown triggered SCR. In DTSCR, the triggering voltage is adjustable with the number of diodes. But high leakage current is still a major concern that restricts the use of DTSCR for low-power applications, such as for portable devices.

The main leakage current is due to the current flowing through the triggering-assist diode string and the leakage current is amplified because of the Darlington effect. Some modified designs on the diode string to reduce the leakage current have been previously reported; namely a diode string controlled by metal-oxide-semiconductor (MOS) transistor (Maloney and Dabral, 1996), a low-leakage polysilicon diode string (Ker *et al.*, 2001), and a modified diode string with emitter and base of parasitic bipolar junction transistor (BJT) tied together (Chen *et al.*, 2003).

Two kinds of diode strings are employed in DTSCR for low-leakage consideration in this study. Compared with the conventional DTSCR (CDTSCR), their layout structures, leakage current, triggering voltage, failure current are investigated.

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* Project partially supported by the Zhejiang Provincial Nature Science Fund of China (Nos. Y107055 and Y1080546), and the Semiconductor Manufacturing International Corp. (SMIC)

DIODE STRING AND ITS DTSCR STRUCTURE

Three main kinds of DTSCR with different triggering modes are shown in Fig.1 (Mergens *et al.*, 2003). When ESD stress is applied, an external triggering diode chain (N, N−1, N−2) is turned on and the current is injected into the SCR gates G_1 or G_2, then the parasitic BJT of the SCR turns on and the ESD current flows through the SCR path. Triggering can either be accomplished by forward biasing the inherent SCR G_1-cathode junction as shown in Fig.1a (Mergens *et al.*, 2003), or the G_2-anode diode as shown in Figs.1b and 1c (Mergens *et al.*, 2003), or both simultaneously (Brennan *et al.*, 2007). The high holding diode in Fig.1c increases the holding voltage of the SCR for improving latch-up immunity. These three type triggering modes are called types A, B, C respectively in this study.

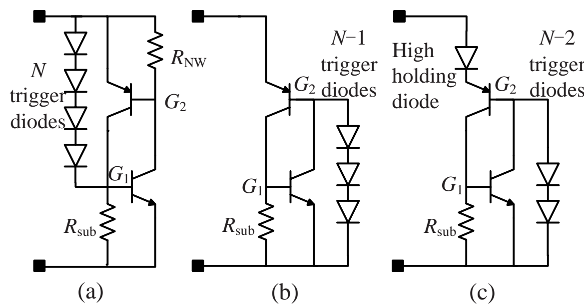

Fig.1 (a) G_1-triggered DTSCR forward biasing SCR G_1–cathode junction; (b) and (c) G_2-triggered DTSCR forward biasing SCR G_2-anode junction; (c) High holding diode in series with SCR for latch-up immunity consideration. R_{sub}, R_{NW} is resistance of substrate and N-well, respectively

A diode string should be thoughtfully designed for lower leakage and saving the silicon area. The conventional diode string with P+ diodes inside separated N-wells has high leakage current because of the Darlington amplification effect shown in Fig.2. A modified DTSCR is designed for lower leakage current in Fig.3. This modified DTSCR's Darlington effect is suppressed with emitter and base of parasitic BJT tied structure. But, a modified diode string requires much silicon area because the space between different deep N-wells is very large in the CMOS process. This SCR triggered by a modified diode string is named as MDTSCR.

We provide a novel design, called a composite diode string, aimed to decrease the DTSCR area and lower substrate leakage. This new structure shown in Fig.4 is comprised of polysilicon diodes in series with modified diodes mentioned above. A polysilicon diode is constructed with silicided P+ and N+ regions and separated with a silicide-block region used to prevent shorting of the P+ and N+ junctions. It is employed here to save the silicon area and suppress the substrate leakage current because the diodes are all realized by the polysilicon layer, and there is no parasitic vertical BJT in these diodes. SCR triggered by a composite polysilicon diode string is named as PDTSCR. PDTSCR is the novel DTSCR in this research.

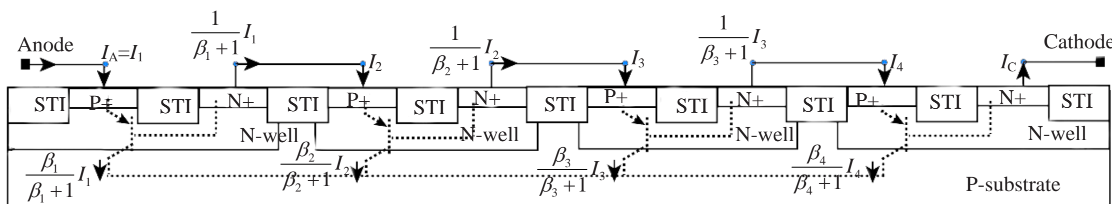

Fig.2 Cross-sectional of the conventional diode string with four stacked diodes in the standard CMOS technology
I_A and I_C are the current at the anode and cathode nodes, respectively; I_1, I_2, I_3 and I_4 are the current at stage 1~4 diode, respectively; β_1, β_2, β_3 and β_4 are the current gain of parasitic BJT of the stage 1~4 diode; STI is shallow trench isolation

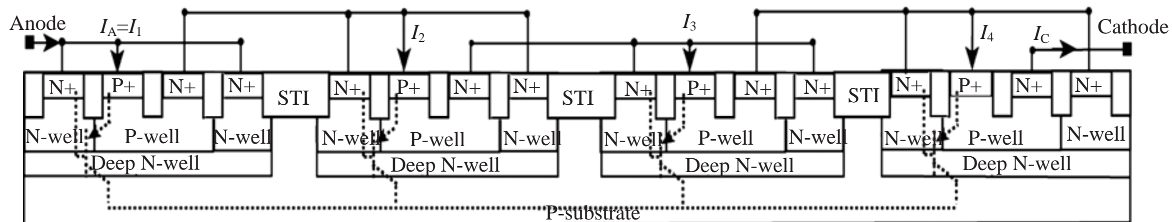

Fig.3 Cross-sectional of the four-stage modified diode string and its parasitic base-emitter tied PNP BJT in a triple-well CMOS process. I_A and I_C are the current at the anode and cathode nodes, respectively; I_1, I_2, I_3 and I_4 are the current at stage 1~4 diode; STI is shallow trench isolation

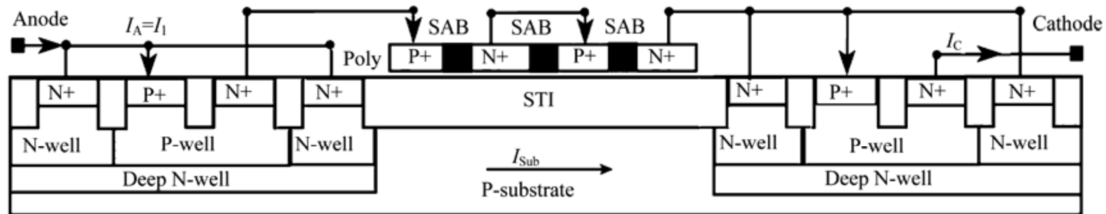

Fig.4 Cross-sectional of the four-stage diode string with two diodes implemented in isolated well and two polysilicon diodes. I_A and I_C are the current at the anode and cathode nodes, respectively; I_1 is the current at stage 1 diode; SAB is salicide block region; I_{Sub} is the current flowing to the substrate

The layout view of a four-stage diode string triggered CDTSCR, MDTSCR and PDTSCR is shown in Fig.5. All DTSCR is designed with single finger structure. SCR and triggering diodes have the same width of 50 μm.

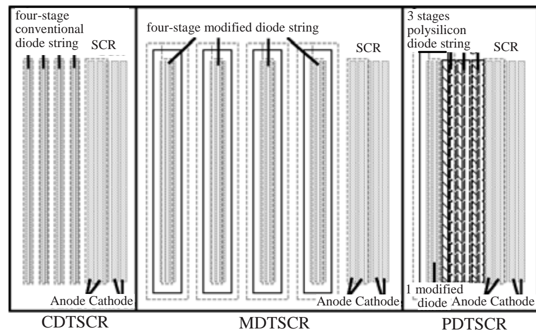

Fig.5 Layout view of four-stage diode triggered CDTSCR, MDTSCR, PDTSCR

Only type A trigger mode is shown. The triggering-assist diodes of PDTSCR are composed of one modified diode in series with three polysilicon diodes

For human body model (HBM) and machine model (MM) ESD pulses, the diode string just assists in triggering SCR and actually does not endure ESD stress. The width of the diode string has a minor effect on the robustness of the whole ESD protection device. But for very fast rise time ESD pulses, the SCR may not turn on fast enough and the current is discharged primarily through the trigger diodes. The voltage overshoot during the charged device model (CDM) event will depend on the size of the trigger diode and may have to be sized large enough to suppress the voltage overshoot. The total area of DTSCR is shown in Table 1. As the design rules in our process, the gap between the deep N-well and N-well is enough for placing three polysilicon diodes. The area of PDTSCR remains the same with an increasing diodes number because the length of polysilicon diodes with number variations is designed to just fill the gap. All DTSCRs are fabricated in a 0.18-μm CMOS process and their ESD behavior is measured by TLP (BARTH 4002, USA) tester.

Table 1 Silicon areas of CDTSCR, MDTSCR, PDTSCR with type A triggering mode

Number of diodes	Silicon area (μm^2)		
	CDTSCR	MDTSCR	PDTSCR
3	1013.968	2527.06	1280.86
4	1192.667	3186.52	1280.86
5	1368.134	3845.98	1280.86

LEAKAGE CURRENT CONSIDERATION

Leakage current test results

The leakage current of above-mentioned DTSCR are measured at a voltage of 1.98 V (10% higher than the normal operation voltage 1.80 V) at a room temperature of 29 °C using semiconductor characterization system (KEITHLEY 4200, USA). Fig.6 illustrates the leakage current of three types of DTSCR triggered by different diodes. With the diode strings stage increasing from 3 to 5, leakage current

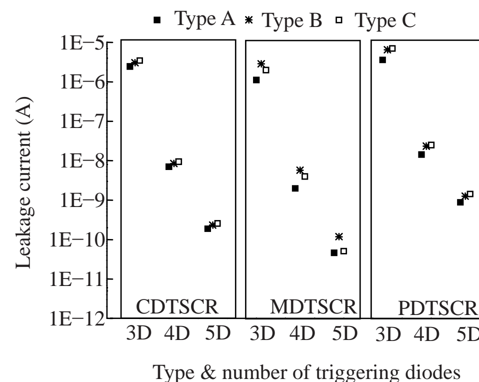

Fig.6 Leakage current at 1.98 V of different DTSCRs with different diode string numbers (3D, 4D and 5D). All DTSCRs are fabricated with 50-μm width

decreases. Type A has a little smaller leakage current than types B and C because type A DTSCR's diode string has one more stage (G_1-cathode diode) than the other two. The MDTSCR has a lower leakage current. However, PDTSCR has a similar leakage current as CDTSCR, but the substrate leakage current of PDTSCR is low.

The behavior of DTSCR under burn-in conditions at a high temperature (HT) 125 °C, together with the conditions at the room temperature (RT) 29 °C are both illustrated in Fig.7. *I-V* sweeping curves in Fig.7 are measured using KEITHLEY 4200. Because the leakage current behavior of types A, B, and C DTSCR are similar, only type C DTSCR is plotted. The leakage current of MDTSCR is notably lower than that of the CDTSCR both at RT and HT. For PDTSCR, when the bias voltage is high (for example, 2.7 V for RT/5D), the current of PDTSCR is extremely lower than these of both MDTSCR and CDTSCR, both at RT and HT. When the bias voltage is low, the leakage current of CDTSCR is higher than these of MDTSCR and CDTSCR.

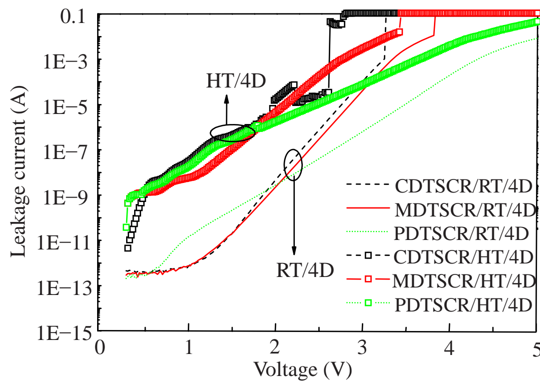

Fig.7 Leakage current at 125 °C (HT) and 29 °C (RT) of Type C DTSCR (CDTSCR, MDTSCR, PDTSCR) with 4 diodes (4D)

Leakage current discussion

For DTSCR, the leakage current is mainly attributed to the diode string, so the analysis of leakage current of the diode string and parasitic effect under function voltage is necessary. Fig.2 shows the cross sectional view of a four-stage conventional diode string, where a diode is formed by P+/N−well junction. The diode chain is electrically a PNP transistor chain. Each P+ diode forms a PNP vertical BJT with a substrate as their collector. The first stage BJT's emitter connects to the anode pad, the last stage BJT's base connects to the cathode pad, and the next BJT's emitter connects to the former stage BJT's base. The current decreases one by one, which is shown below (Voldman *et al.*, 1995):

$$I_1=I_A, \tag{1}$$

$$I_i=I_{i-1}\left(\frac{1}{\beta_{i-1}+1}\right)=I_A\prod_{j=2}^{i}\left(\frac{1}{\beta_{j-1}+1}\right), \tag{2}$$

where I_A is the current at the anode nodes; I_i is the current at stage i diode; β_j is the current gain of parasitic BJT of the stage j diode.

From the Shockley equation for a PN junction diode, a forward biased voltage is given by

$$V_D=nV_T\ln\frac{I_D}{I_S}. \tag{3}$$

where V_T is thermal voltage, I_D and I_S are diode current and saturation current, respectively.

For a PNP-based base-emitter (BE) junction diode as shown in Fig.2 and assuming all stages of BJT with the same current gain of β, the following equation holds:

$$V_{BEi}=V_{Di}=V_{D1}-nV_T\ln(1+\beta)^{i-1}. \tag{4}$$

When used as power clamp, a supply voltage V_{DD} is applied on the two terminals of an m-stage diode string, and the voltage on the first diode is V_{D1}:

$$V_{DD}=\sum_{i=1}^{m}V_{Di}=mV_{D1}-\frac{m(m-1)}{2}nV_T\ln(1+\beta), \tag{5}$$

$$\begin{aligned}V_{D1}&=\frac{1}{m}\left(V_{DD}+\frac{m(m-1)}{2}nV_T\ln(1+\beta)\right)\\&=\frac{V_{DD}}{m}+\frac{m-1}{2}nV_T\ln(1+\beta).\end{aligned} \tag{6}$$

As shown in Eq.(6), the voltage on the first stage diode V_{D1} is much higher than the average allocated voltage of the ideal, clean diode string (V_{DD}/m), and the same as its current, because of the Darlington amplification effect. And from Eq.(2), the current flowing through the N-well is I_C, taking four-stage diodes as example:

$$I_C = I_A \left(\frac{1}{\beta_1+1}\right)\left(\frac{1}{\beta_2+1}\right)\left(\frac{1}{\beta_3+1}\right)\left(\frac{1}{\beta_4+1}\right), \quad (7)$$

where I_C is the current at the cathode nodes.

For I_C is relatively low, most of the current ($I_A - I_C$) flows through the substrate and forms substrate leakage currents. Those leakage currents can easily cause some unexpected effects, such as the mistriggering of the P-substrate/N-well diode.

With regard to the MDTSCR, its Darlington effect is suppressed with emitter and base of the parasitic BJT tied structure which holds the parasitic bipolar BJT off. Thus, the voltage on the first diode is V_{DD}/m, and the leakage current is $I_A \approx I_C$, which is lower than that of DTSCR. The substrate current is nearly negligible on circuit's working status, $I_{sub} \approx 0$.

A novel PDTSCR is designed for low substrate leakage current and smaller area than MDTSCR. PDTSCR's triggering diodes are all realized by the polysilicon layer, thus there is no parasitic vertical BJT in these diodes, and this therefore will suppress the Darlington effect. In our process, polysilicon diode has a higher leakage current than a conventional diode at the same voltage. But the substrate leakage current of PDTSCR is negligible, $I_{sub} \approx 0$, and the P-substrate/N-well diode mistriggering effect will not be a concern for PDTSCR design. So PDTSCR has a trade-off between low substrate leakage current (like MDTSCR) and low area (like CDTSC). Moreover, its behavior under burn-in conditions at a high temperature is better than both CDTSCR and MDTSCR.

TRIGGERING VOLTAGE ANALYSIS

TLP plots measured by BARTH 4002 (USA), with 10 ns rise time and 100 ns pulse width, are shown in Fig.8. Only 5D DTSCR are shown and leakage current curves which have been analyzed above are removed for compact consideration. The second breakdown point is at the top end of the curves. The small graph at the top left corner shows the triggering voltage of different DTSCRs. The triggering voltage of all these devices is listed in Fig.9. Obviously, the triggering voltage increases with more diodes. It can be approximately estimated that the triggering voltage increases 1 V by adding one more diode.

Different types of diode strings have different triggering voltages. The triggering voltage of CDTSCR is the lowest. It is obvious because the triggering current of a conventional diode string is much higher than these of MDTSCR and PDTSCR at the same voltage, which is analyzed in Section 3.

A different triggering mode has an obvious effect on its triggering voltage. In DTSCR types B & C, besides triggering the PNP parasitic BJT, the leakage current of the substrate will also trigger the NPN BJT, which will decrease the triggering voltage. DTSCR A is the most difficult to be triggered. We can see from the schematic of DTSCR in Fig.1a that when ESD stress is applied, the diode string turns on and injects enough current into the SCR gates G_2. The NPN BJT will turn on when the voltage between G_2 and cathode junction turns on. But in Figs.1b and 1c, PNP BJT turns on as soon as the four-stage diode string forward turns on. It means one more diode needs to be turned on for DTSCR A, so the triggering voltage is higher.

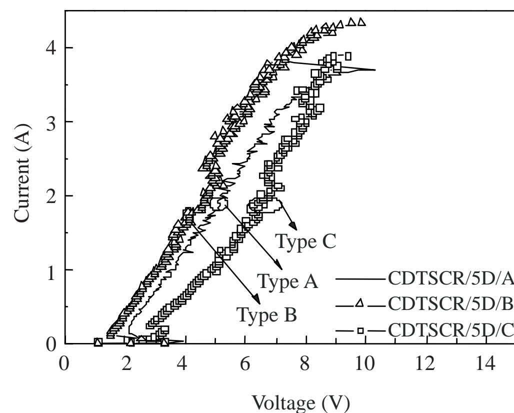

Fig.8 TLP *I-V* curves of types A, B & C CDTSCRs with 5D

The leakage current curves are removed for compact consideration; the second breakdown point is at the top end of the curves

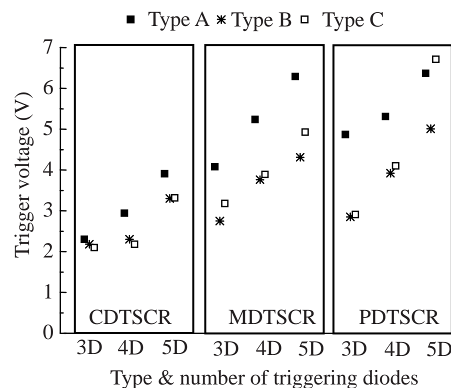

Fig.9 Triggering voltage V_{t1} of different DTSCRs with different diode string numbers (3D, 4D and 5D)

FAILURE CURRENT EVALUATION

The failure current (I_{t2}) is determined at the point where the leakage current is 10^3 higher than its normal value. I_{t2} of 5D DTSCR is shown in Fig.8, and summarized in Fig.10. As mentioned above, these DTSCR are fabricated with a single SCR and the width of triggering-assist diodes and SCR is 50 μm. The metal routings of types A, B, C are sketched in Fig.11. Only a 4D CDTSCR is cited, the metal routings of MDTSCR and PDTSCR are the same with the CDTSCR. When SCR is in latch-up state, most of the ESD current flows through the SCR path for its small turn-on resistor. So I_{t2} among DTSCR with different types and a different diode number of diode string is similar for 10 ns rise time TLP testing. On the other hand, when operating in the high current mode, the parasitic BJT of all three types of diode string are in saturation, and this path will afford some of the ESD current.

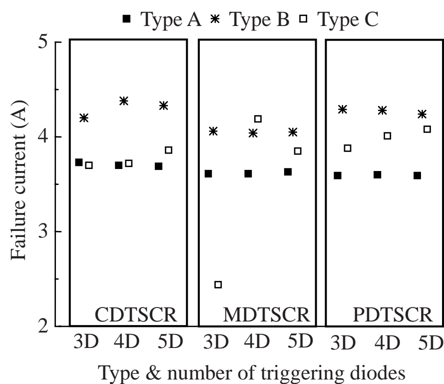

Fig.10 Failure current I_{t2} of different DTSCRs with different diode string numbers (3D, 4D and 5D)

As shown in Fig.10, expect the unexpected points for 3 stage modified diode string triggered SCR type C (will be studied in further work), I_{t2} of DTSCR type A is the lowest. This is determined by its layout (shown in Fig.11). For DTSCR types B and C, the trigger diodes are distributed on both sides of the P-well, the direction of most substrate leakage current is opposite to the current of the main SCR, while for type A all four diodes are on one side and the directions of the diode leakage current and the main SCR current are the same, so types B and C can afford more ESD current for good uniformity. Since the high holding diode of DTSCR type C has relatively enough width of 50 μm to afford the ESD current, DTSCR type C has lower I_{t2} than B just because of its high holding voltage. For the same type of DTSCR, a different diode string type shows a minor difference in failure current. This is expected because with high ESD current, the parasitic BJT of all three types of diode string is in saturation, and the current flowing through the diode string will not show a significant difference.

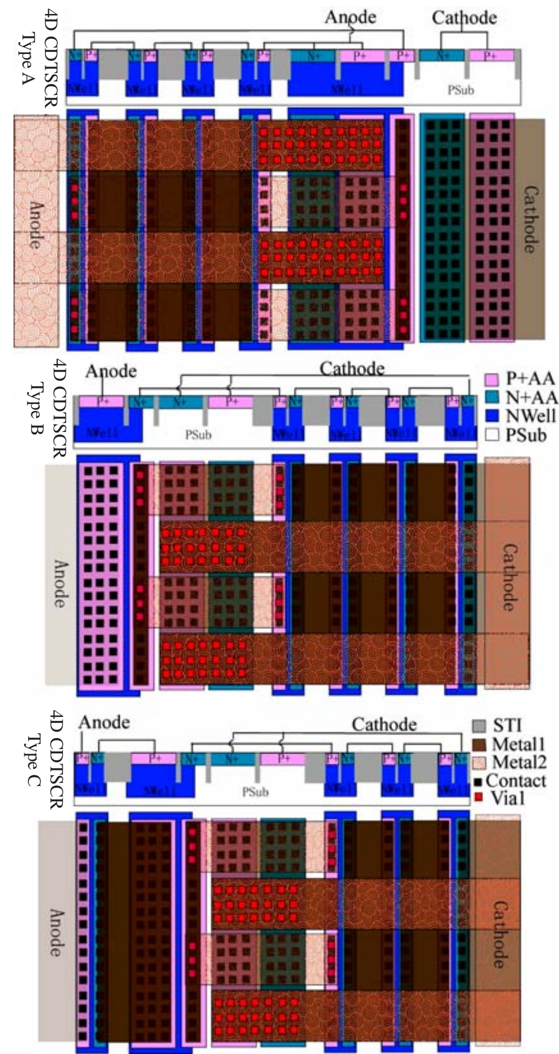

Fig.11 Metal routing of 4D triggered CDTSCRs with type A, type B and type C

DISCUSSION AND FUTURE WORK

The discussion of DTSCR is focused on the analysis of leakage current in this study. But for the inherently slow turn-on speed, the effectiveness evaluation of SCR—whether it can really protect a

sensitive circuit—is a challenging work. The voltage overshoot in particular at the start of the CDM like pulse is a main concern. In the design of DTSCR, the SCR will conduct the current predominantly and the trigger diodes will not have a significant current through it for HBM and MM ESD pulse. But the voltage overshoot during the CDM event will depend on the size of the trigger diode and it may have to be sized large enough to suppress the voltage overshoot (Di Sarro *et al.*, 2006). In this research, a 50-μm width diode is employed to increase the robustness for CDM pulses.

In the future, a gate oxide monitor, typically a drain and source shorted MOS transistor, should be in parallel to the ESD protection devices to verify the effectiveness of these DTSCR. TLP measurements should be performed with a very fast rise time of 200 ps. The turn-on time of DTSCR should be extracted from a VFTLP test curve.

CONCLUSION

DTSCR triggered by three kinds of diode strings with three different kinds of diode trigger modes and different diode stages are investigated.

An MDTSCR has the lowest leakage current both at room and high temperatures, the highest trigger voltage and largest device area. Composited PDTSCR has lower leakage current than a conventional one at high temperature and similar leakage current as a CDTSCR but much lower substrate leakage current at room temperature. Also, PDTSCR has a lower trigger voltage and smaller area than MDTSCR. So PDTSCR has a trade-off between CDTSCR (large substrate leakage current) and MDTSCR (large silicon cost). Three types of DTSCR have similar I_{t2}.

More triggering-assist diodes have lower leakage current and higher triggering voltage and I_{t2} holds stable.

When considering the DTSCR types A, B and C with the same triggering-assist diodes, type A has the lowest leakage current, failure current I_{t2} and the highest triggering voltage. Type C DTSCR has a higher holding voltage for latch-up immunity consideration. The study provides useful information for the design and optimization of DTSCR ESD protection solutions for modern and future CMOS technologies.

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