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Efficient design of rotary traveling wave oscillator array via geometric programming*

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Abstract: This paper presents an efficient method for globally optimizing and automating component sizing for rotary traveling wave oscillator arrays. The lumped equivalent model of transmission lines loaded by inverter pairs is evaluated and posynomial functions for oscillation frequency, power dissipation, phase noise, etc. are formulated using transmission line theory. The resulting design problem can be posed as a geometric programming problem, which can be efficiently solved with a convex optimization solver. The proposed method can compute the global optima more efficiently than the traditional iterative scheme and various design problems can be solved with the same circuit model. The globally optimal trade-off curves between competing objectives are also computed to carry out robust designs and quickly explore the design space.

Key words: Rotary traveling wave oscillator array (RTWOA), Clock distribution, Transmission line resonator, Global optimization, Geometric programming (GP)

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INTRODUCTION

The global clock distribution network has a significant impact on the performance of modern multi-gigahertz synchronous VLSI systems. As the frequency continues to increase, the skew and jitter introduced by the clock network must be reduced proportionally with the clock period (Restle *et al*., 2001). Meanwhile, the clock network can dissipate up to 40% of the total chip power (Duarte *et al*., 2002). These factors all call for innovative clock structures.

The rotary traveling wave oscillator array (RTWOA) is one of the novel techniques proposed for the global clock distribution of multi-gigahertz microprocessors (Wood *et al*., 2001). The rotary traveling wave oscillator (RTWO), which produces gigahertz multiphase square waves with uniform amplitude, is based on the principle of wave-traveling in transmission lines. It is reported that by using RTWOA for global clock distribution, up to 70% of power dissipation can be saved compared with conventional buffered H-trees (Yu and Liu, 2005). An implementation of a voltage controlled oscillator based on RTWO using the standard 0.18 μm CMOS process shows that it can work properly at 18 GHz (Mercey, 2003).

Due to high complexity and various constraints, it is very hard to optimize all design parameters to meet multiple specifications simultaneously. The first reported optimization scheme for RTWOA was a heuristic methodology based on the partial element equivalent circuit (PEEC) method (Yu and Liu, 2007). Such an approach uses an improved binary search to optimize the design variables one by one and requires multiple iterations to reach a near-optimal solution. This method is time consuming and requires human intervention, which limits the scope of its application.

In this paper, we propose a novel scheme based on geometric programming (GP) for computing the

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globally optimal solutions to meet all design specifications simultaneously. Our approach is to formulate the design problem of RTWOA as a special convex optimization problem. Our previous work has proved the effectiveness of GP on a single RTWO loop (Zhuo *et al*., 2007) and in this paper, we make the following improvements. First, the lumped equivalent model of transmission lines loaded by inverter pairs is improved through electromagnetic simulation. Moreover, the design specifications may include not only oscillation frequency and chip area, which were the only two constraints considered by Yu and Liu (2007), but also power dissipation, loop gain, phase noise, etc. The process of formulating posynomial models for performance measures of RTWOA is introduced in detail. With posynomial models for all the specifications, we can choose any of them as the objective function to be minimized to meet different design requirements.

BACKGROUND

Rotary traveling wave oscillator array

Fig.1 shows the typical structure of an RTWOA comprised of 16 RTWO rings. The differential lines of each ring are cross-connected to ensure a reversed feedback. Cross-coupled inverter pairs are distributed around the ring to compensate for the energy losses due to the resistivity of interconnects. These inverter pairs switch when the wave travels by and act like amplifiers to restore the wave distortion. The cross-coupled inverters also enforce the odd mode operation for the differential lines and sustain the phase locking. The adjacent rings are coupled together by hard links so that all the rings are synchronized to a single oscillation frequency. Novel clock distribution techniques based on RTWOA have the advantages of low-power and low-jitter (Wood *et al*., 2001).

Geometric programming

Geometric programming (GP) is a special form of convex optimization problem whose objectives and constraints are either posynomial functions or monomial functions (Boyd *et al*., 2006). Let $x_1, x_2, \ldots, x_n$ be n positive variables, and $\boldsymbol{x}=(x_1, x_2, \ldots, x_n)$ a vector with components x_i. A monomial function is a special posynomial with the form

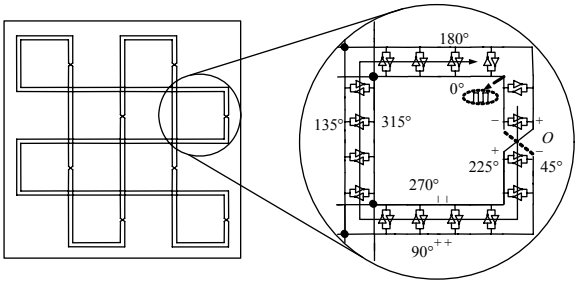

Fig.1 Circuit diagram of the rotary traveling wave oscillator array (RTWOA)

$$g_k(\boldsymbol{x}) = c_k x_1^{a_{1k}} x_2^{a_{2k}} \ldots x_n^{a_{nk}} ,$$

where $c_k>0$ and $a_{ik}\in\mathbb{R}$. A posynomial function is a sum of monomials:

$$f_i(\boldsymbol{x}) = \sum_k g_k(\boldsymbol{x}) .$$

The standard form of a GP problem is expressed as follows:

$$\min f_0(\boldsymbol{x}),$$

subject to

$$\begin{cases} f_i(\boldsymbol{x}) \le 0, & i = 1, 2, \ldots, m, \\ g_j(\boldsymbol{x}) = 0, & j = 1, 2, \ldots, p, \end{cases}$$

where $f_i(\boldsymbol{x})$ are posynomials and $g_j(\boldsymbol{x})$ are monomials. It is shown that a wide variety of circuit performance measures of the design variables are posynomial functions; thus, GP can be used in the design process of various CMOS analog circuits (Hershenson *et al*., 1999; Hershenson, 2004). Noting that the objective function should only be minimized and the constraint functions are of specific forms, the key process of using GP is to formulate the design problem in a standard GP form.

POSYNOMIAL MODELS FOR RTWOA

Design variables

Our goal is to pose RTWOA design problems as GP problems. Fig.2 shows the basic structure of RTWOA. Here we suppose the number of rings distributed on each side of the square chip is $N_r=2n_r$, where $n_r=1, 2, 3, \ldots$. Thus, there are $4n_r^2$ rings in the array in total. Fig.3 is the geometry of differential transmission lines. In a specific process, the dielectric

height H and the thickness of metal lines T_c are usually constants. In this paper, we use the SMIC 0.18 μm process and these constants are H=6.52 μm, T_c=2.17 μm. Table 1 summarizes the design variables and their constraints.

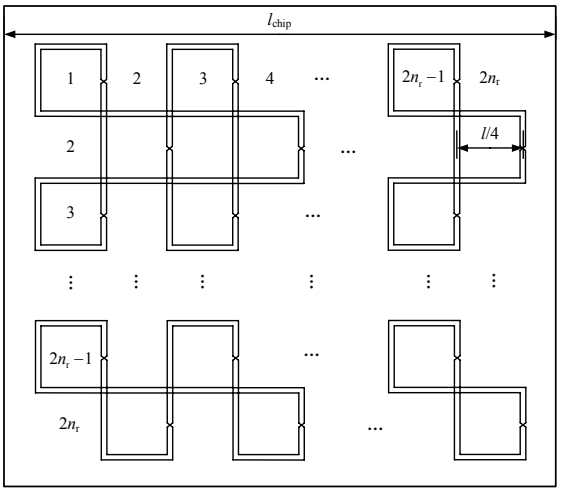

Fig.2 Structure of the rotary traveling wave oscillator array (RTWOA)

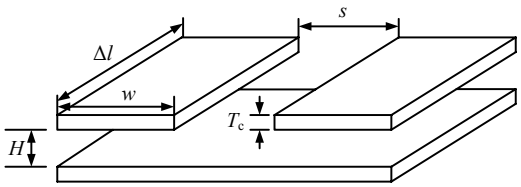

Fig.3 Structure of differential transmission lines

Table 1 Design variables of the rotary traveling wave oscillator array (RTWOA)

Component	Design variable	Constraint
Chips	Number of rings, $2n_r$	$2\le n_r\le 20$
Transmission line	Width, w (μm)	$3\le w\le 10$
	Separation, s (μm)	$5\le s\le 25$
Inverter pair	NMOS finger width, w_n (μm)	$0.5\le w_n\le 2.5$
	PMOS finger width, w_p (μm)	$0.5\le w_p\le 10$
	Finger of MOSFET, nfin	$2\le$nfin≤ 20
	Number of pairs, N	$8\le N\le 32$

Physical constraints

The array is distributed to cover a square chip with area $A_{chip}=l_{chip}\times l_{chip}$, and the total area of all the rings (A_{cover}) should never exceed the area of the chip. Meanwhile, we would like the array to cover a certain percentage of the total chip area, e.g., 80%. These lead to the following two monomial constraints:

$$0.8A_{chip}\le A_{cover}=(2n_r)^2\times(l_{chip}/4)^2\le A_{chip}. \quad (1)$$

In addition, we limit the die area of the inverter pairs (A_{MOS}) and the metal area of the transmission lines (A_{tran}) with the following posynomial constraints:

$$A_{MOS}=N\times 2\times(l_{MOS}w_p+l_{MOS}w_n)\le A_{MOS\_max}, \quad (2)$$

$$A_{tran}=l\times(2w+s)\le A_{tran\_max}, \quad (3)$$

where l_{MOS} is the channel length of NMOS and PMOS.

Transmission line parameters

Fig.4a shows the lumped equivalent model of transmission lines loaded by inverter pairs. L_s and L_m are the self inductance and mutual inductance per unit length, respectively, R_0 is the effective resistance per unit length, and C_{11} and C_{12} are the self capacitance and mutual capacitance per unit length, respectively. For transmission lines working at the odd mode, the equivalent inductance and capacitance per unit length are as follows (Hsieh *et al*., 2007):

$$L_0=L_s-L_m, \quad (4)$$

$$C_0=C_{tran\_perlen}+C_{inv\_perlen}=C_{11}+2C_{12}+2C_{inv}/\Delta l, \quad (5)$$

where C_{inv} is the equivalent capacitance of one inverter pair. According to Fig.4b, we can obtain the expression of C_{inv}:

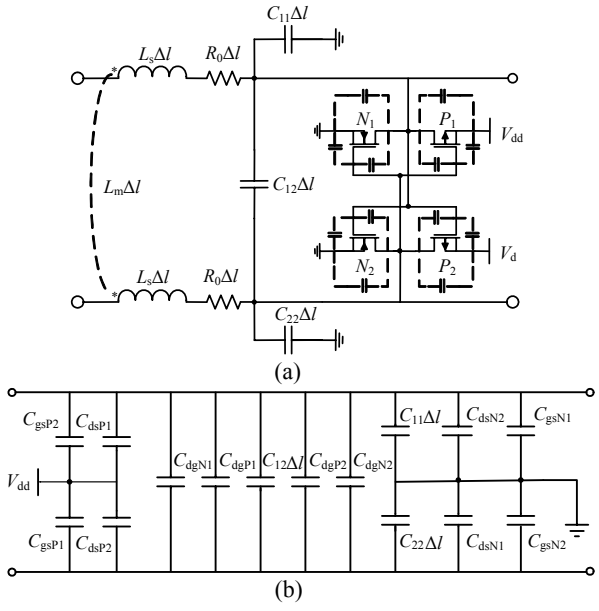

Fig.4 (a) Lumped equivalent circuit of loaded transmission line with length Δ*l*; (b) Equivalent capacitance circuit

$$\begin{aligned}C_{\text{inv}} &= (C_{\text{gsP2}} + C_{\text{dsP1}}) \,||\, (C_{\text{gsP1}} + C_{\text{dsP2}}) \\ &\quad + (C_{\text{gsN2}} + C_{\text{dsN1}}) \,||\, (C_{\text{gsN1}} + C_{\text{dsN2}}) \\ &\quad + C_{\text{dgN1}} + C_{\text{dgP1}} + C_{\text{dgP2}} + C_{\text{dgN2}} \\ &= (C_{\text{gsP2}} + C_{\text{dsP1}} + C_{\text{gsP1}} + C_{\text{dsP2}} \\ &\quad + C_{\text{gsN2}} + C_{\text{dsN1}} + C_{\text{gsN1}} + C_{\text{dsN2}}) / 4 \\ &\quad + C_{\text{dgN1}} + C_{\text{dgP1}} + C_{\text{dgP2}} + C_{\text{dgN2}},\end{aligned} \tag{6}$$

where C_{gs} is the gate-to-source overlap capacitance, C_{ds} is the drain-to-source capacitance, and C_{dg} is the drain-to-gate overlap capacitance.

The analytic expressions of L_{s} and L_{m} given by Delorme *et al*.(1996) are as follows:

$$L_{\text{s}} = \frac{\mu_0}{2\pi} \ln\left(\frac{2H_{\text{eq}}}{r_{\text{eq}}} + 1\right), \tag{7}$$

$$L_{\text{m}} = \frac{\mu_0}{4\pi} \ln\left[\frac{(s_{\text{eq}} + 2r_{\text{eq}})^2 + (3r_{\text{eq}} + 2H_{\text{eq}} + h_{\text{eq}})^2}{(s_{\text{eq}} + 2r_{\text{eq}})^2 + (3r_{\text{eq}} + h_{\text{eq}})^2}\right], \tag{8}$$

where $H_{\text{eq}}=H+(T_{\text{c}}-w)/4$, $r_{\text{eq}}=(w+T_{\text{c}})/4$, $h_{\text{eq}}=-(w+T_{\text{c}})/2$ and $s_{\text{eq}}=s+(w-T_{\text{c}})/2$. Eqs.(7) and (8) are neither posynomials nor monomials, so we use the following monomial to fit L_0 within the specified ranges of w and s:

$$L_0=L_{\text{s}}-L_{\text{m}}=0.4955\times10^{-6}\times w^{-0.4166}\times s^{0.1266}. \tag{9}$$

The analytic expressions for C_{11} and C_{12} given by Delorme *et al*.(1996) are as follows:

$$\begin{aligned}C_{11}/\varepsilon_{\text{ox}} &= 1.11w/H + [0.79(w/H)^{0.1} + 0.59(T_{\text{c}}/H)^{0.53}] \\ &\quad + [0.52(w/H)^{0.01} + 0.46(T_{\text{c}}/H)^{0.17}](1 - 0.87\text{e}^{-s/H}),\end{aligned} \tag{10}$$

$$\begin{aligned}C_{12}/\varepsilon_{\text{ox}} &= T_{\text{c}}/s + 1.21(T_{\text{c}}/H)^{0.1}(s/H + 1.15)^{-2.22} \\ &\quad + 0.25\ln(1 + 7.17w/s)(s/H + 0.54)^{-0.64}.\end{aligned} \tag{11}$$

Similarly, we use monomials to fit the special functions in Eqs.(10) and (11). Finally, we obtain the posynomial expression of the transmission line capacitance as follows:

$$\begin{aligned}C_{\text{tran\_perlen}} &= C_{11} + 2C_{12} = \varepsilon_{\text{ox}}[1.11w/H + 0.79(w/H)^{0.1} \\ &\quad + 2(s/T_{\text{c}})^{-1} + 0.748(w/H)^{0.417}(s/H)^{-0.844} \\ &\quad + 0.504(s/H)^{-0.813} + 0.63(s/H)^{0.292} + 0.2306].\end{aligned} \tag{12}$$

According to the analytic expressions for the MOS capacitances provided by the foundry provider, the lumped equivalent capacitance of the inverter pair could be fitted as a monomial function of w_{n} and w_{p}. Since we usually have $\mu_{\text{n}}C_{\text{oxn}}w_{\text{n}}=\mu_{\text{p}}C_{\text{oxp}}w_{\text{p}}$ (μ_{n}, μ_{p} and C_{oxn}, C_{oxp} are electron mobility and silicon dioxide capacitance for NMOS and PMOS, respectively) for typical push-pull inverters, we write the monomial expression in this special case as follows:

$$C_{\text{inv}} = 11.5\times10^{-15}\times w_{\text{n}}^{\,0.9313}\times \text{nfin}^{0.9433}. \tag{13}$$

Substituting Eqs.(12) and (13) into Eq.(5), we can obtain the posynomial expression of C_0.

Start-up condition and oscillation frequency

Each inverter pair can be treated as a transconductor with negative differential transconductance equal to G_{m} (Fig.5). According to our earlier study (Zhuo *et al*., 2007), the RTWO could be treated as a closed-loop feedback system, whose transfer function is

$$\begin{aligned}H(\text{j}\omega) &= (1 - G_{\text{m}}Z_0)^N \text{e}^{-N\gamma\Delta l} \\ &= (1 - G_{\text{m}}Z_0)^N \text{e}^{-N\alpha\Delta l}\text{e}^{-\text{j}N\beta\Delta l},\end{aligned} \tag{14}$$

where $Z_0 = \sqrt{L_0 / C_0}$ is the characteristic impedance and $\gamma=\alpha+\text{j}\beta$ is the complex propagation constant. The transconductance of the inverter pair around the trip point is (Zhuo *et al*., 2007)

$$G_{\text{m}} = -k_{\text{n}}/2\times(V_{\text{dd}} - V_{\text{thn}} - V_{\text{thp}}), \tag{15}$$

where $k_{\text{n}}=\mu_{\text{n}}C_{\text{oxn}}w_n/l_{\text{MOS}}$, and V_{thn} and V_{thp} denote the threshold voltages for NMOS and PMOS, respectively. For a stabilized oscillator, the transfer function must meet the following requirements:

$$\left|H(\text{j}\omega)\right| \geq 1, \tag{16}$$

$$\angle H(\text{j}\omega) = (2k+1)\pi,\ k = 0,1,2,\ldots. \tag{17}$$

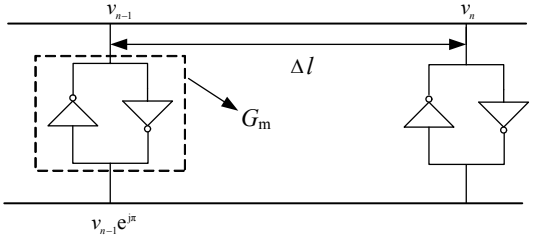

Fig.5 A short section of the transmission line

This leads directly to the following start-up condition and oscillation frequency of RTWO:

$$-G_{\mathrm{m}}Z_0 \geq \mathrm{e}^{\alpha\Delta l}-1 \approx \alpha\Delta l = \eta\,, \tag{18}$$

$$f_{\mathrm{osc}} \approx \frac{1}{2l\sqrt{L_0C_0}}\,. \tag{19}$$

For a low-loss transmission line, the attenuation factor α is usually small. As a conservative approach, we use a positive constant η as the lower bound to ensure that the design can always oscillate in the worst case. Therefore, the start-up condition can be written as the following posynomial constraint:

$$\left[\frac{2\eta l_{\mathrm{MOS}}}{\mu_{\mathrm{n}}C_{\mathrm{oxn}}w_{\mathrm{n}}(V_{\mathrm{dd}}-V_{\mathrm{thn}}-V_{\mathrm{thp}})}\right]^2 L_0^{-1}C_0 \leq 1\,. \tag{20}$$

For oscillation frequency, we can enforce a lower and an upper bound ($f_{\min}\leq f\leq f_{\max}$), respectively, to obtain the following posynomial constraints:

$$4f_{\min}^2 l^2 L_0 C_0 \leq 1\,, \tag{21}$$

$$(2f_{\max})^{-2} l^{-2} L_0^{-1} C_{\mathrm{inv\_perlen}}^{-1} \leq 1\,. \tag{22}$$

Since $C_{\mathrm{inv\_perlen}}>>C_{\mathrm{tran\_perlen}}$, here we relax C_0 to $C_{\mathrm{inv\_perlen}}$ to evaluate the upper bound of the oscillation frequency.

Power dissipation

The major power dissipation of RTWO is due to the resistivity of the transmission lines (Wood *et al*., 2001). It is reported that the power dissipated by the transmission lines accounts for more than 80% of the total power dissipation (Yu and Liu, 2005). Therefore, it is crucial to restrict the power dissipation on the transmission lines to achieve low-power clock distribution. The power dissipated in the transmission lines of a single loop can be estimated using the following posynomial:

$$P_{\mathrm{r}} = V_{\mathrm{dd}}^2 / Z_0^2 \times R_{\mathrm{loop}} = V_{\mathrm{dd}}^2 L_0^{-1} C_0 \rho \times 2l/(wT_{\mathrm{c}}), \tag{23}$$

where R_{loop} is the loop resistance and ρ is the resistivity (Wood *et al*., 2001).

Phase noise

Assuming that white noise is the dominant source of noises, according to Hajimiri's linear time variant theory (Hajimiri *et al*., 1999), the phase noise of RTWO is given by

$$L(\Delta f) = \frac{\Gamma_{\mathrm{rms}}^2}{q_{\max}^2}\frac{N(\overline{i}_{\mathrm{t}}^2/\Delta f)}{2\times(2\pi\Delta f)^2}\,, \tag{24}$$

where $\overline{i}_{\mathrm{t}}^2/\Delta f = (\overline{i}_{\mathrm{n}}^2+\overline{i}_{\mathrm{p}}^2)/(2\Delta f)$ is the total single side band noise density of the inverter pair in each stage, $q_{\max}\approx C_{\mathrm{inv\_perlen}}\times 2l\times V_{\mathrm{dd}}/N$ is the maximum charge swing in each stage, and once again we use $C_{\mathrm{inv\_perlen}}$ instead of C_0 to make $q_{\max}$ a monomial. Γ_{rms}^2 is the RMS value for the impulse sensitivity function (ISF) of RTWO. For the push-pull inverters, $\overline{i}_{\mathrm{n}}^2/\Delta f$ and $\overline{i}_{\mathrm{p}}^2/\Delta f$ are monomials:

$$\overline{i}_{\mathrm{n}}^2/\Delta f = 4kT\gamma\times\mu_{\mathrm{n}}C_{\mathrm{ox}}w_{\mathrm{n}}/l_{\mathrm{MOS}}\times(V_{\mathrm{dd}}-V_{\mathrm{thn}}), \tag{25}$$

$$\overline{i}_{\mathrm{p}}^2/\Delta f = 4kT\gamma\times\mu_{\mathrm{p}}C_{\mathrm{ox}}w_{\mathrm{p}}/l_{\mathrm{MOS}}\times(V_{\mathrm{dd}}-V_{\mathrm{thp}}), \tag{26}$$

where k is the Boltzman constant, T is the standard noise temperature, and γ is the process constant, which is usually 2/3 for long channel devices and 2~3 times larger for short channel devices (Razavi, 2001). Thus, $\overline{i}_{\mathrm{t}}^2/\Delta f$ is formulated as a posynomial.

Assuming the oscillator is a second-order system and f is the function of oscillating waveform, the ISF is defined as (Hajimiri and Lee, 1998)

$$\Gamma(x) = f'/(f'^2+f''^2)\,. \tag{27}$$

A square wave can be expressed as a Fourier function:

$$y(t) = \frac{2}{\pi}\sum_{k=0}^{n}\frac{(-1)^k}{2k+1}\cos[(2k+1)2\pi f_0 t]\,, \tag{28}$$

where f_0 is the oscillation frequency and n is the number of harmonics, which is restricted by the number of stages in the loop as (Mercey, 2004)

$$n = \lfloor N/\pi - 0.5 \rfloor\,. \tag{29}$$

The root mean square of ISF is related to n as (Mercey, 2004)

$$\Gamma_{\mathrm{rms}}^2 = \frac{\pi^2}{8}\frac{1}{(n+1)^3}. \tag{30}$$

Thus, we can use a monomial to fit Γ_{rms}^2:

$$\Gamma_{\mathrm{rms}}^2 = \pi^2/8 \times 11.67 \times N^{-2.656}. \tag{31}$$

Finally, we posed the phase noise of RTWO given in Eq.(24) as a posynomial.

METHODOLOGY FOR RTWOA DESIGN

Since we have posed all constraints as posynomial or monomials, we can set any of them as the objective function to be minimized. For example, the GP form design problem aiming to minimize the power dissipation of a single loop in RTWOA can be written as

$$\min P_{\mathrm{r}},$$

subject to

$$\begin{cases} |H(\mathrm{j}\omega)| \geq 1, f_{\min} \leq f_{\mathrm{osc}} \leq f_{\max}, 0.8A_{\mathrm{chip}} \leq A_{\mathrm{cover}} \leq A_{\mathrm{chip}}, \\ A_{\mathrm{MOS}} \leq A_{\mathrm{MOS\_max}}, A_{\mathrm{tran}} \leq A_{\mathrm{tran\_max}}, L(\Delta f) \leq L_{\max}, \\ u_{\mathrm{n}} C_{\mathrm{oxn}} w_{\mathrm{n}} = u_{\mathrm{p}} C_{\mathrm{oxp}} w_{\mathrm{p}}. \end{cases}$$

Note that the constraints of design variables are not listed here. One hurdle of applying GP into the design of RTWOA is that the variables N, nfin and n_{r} are actually natural numbers, which would be recognized by the GP solver as real numbers. To deal with that, we first ignore the integer essence of N, nfin and n_{r} and solve the resulting GP directly. Then, we round the solution of N, nfin and n_{r} and evaluate the design again to obtain a final solution with integer results. Specifically, we use the following methodology for applying GP to the RTWOA design:

1. Set the possible ranges for each design variable in accordance with the specific process technology.

2. Establish the posynomial models and use fitted analytic expressions when necessary. Pose the design problem as a GP problem.

3. Relax N, nfin and n_{r} to real numbers and solve the equivalent GP problem with specific convex solvers.

4. For the real number solutions of N, nfin and n_{r}, round them to obtain two-integer sets $N'=\{\lfloor N \rfloor, \lceil N \rceil\}$, $\mathrm{nfin}'=\{\lfloor \mathrm{nfin} \rfloor, \lceil \mathrm{nfin} \rceil\}$ and $n_{\mathrm{r}}'=\{\lfloor n_{\mathrm{r}} \rfloor, \lceil n_{\mathrm{r}} \rceil\}$.

5. For each of the combination of N', nfin and n_{r}', solve the GP problem with monomial equation constraints $N=N'$, nfin=nfin′ and $n_{\mathrm{r}}=n_{\mathrm{r}}'$, respectively, instead of the former inequality constraints.

6. Compare and choose the design with the best performance.

DESIGN EXAMPLES

We have applied our GP-based methodology to four design cases. All designs were under SMIC 0.18 μm technology with a 1.8 V power supply. The first three cases all aimed to minimize the power dissipation with different oscillation frequencies. For the last case, we chose the phase noise as the objective function with constraints of physical dimensions, oscillation frequency and start-up condition. The GP solver we used was the GGPLAB package from GGPLAB (2006). The circuit simulation tool was Agilent Advanced Design System (ADS) 2006A.

Effectiveness of fitted analytic expressions

1. Posynomial models of transmission line parameters

First, we investigated the effectiveness of the fitted analytic monomial and posynomial expressions. Fig.6 depicts the relative errors of our models. The horizontal and vertical axes correspond to the relative error and the fraction of the data beyond a specific error, respectively, expressed as a percentage. It can be seen that more than 90% of the errors for the inductance model were less than 4%. Similarly, the relative errors for the transmission line capacitance and MOS capacitance models were less than 5% and 10%, respectively, for 90% of nodes.

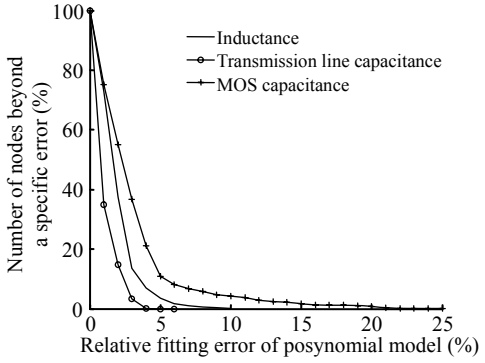

Fig.6 The relative errors of posynomial models

2. Monomial model of $\Gamma_{\rm rms}$

Table 2 shows the $\Gamma_{\rm rms}$ calculated using the original Eq.(30) and the fitted monomial Eq.(31). Since the geometry of a single RTWO in our implementation is square, the number of inverter pairs we chose here was multiples of 4. The results showed that the monomial model of $\Gamma_{\rm rms}$ fits the original expression well at the specific points of our case.

Table 2 Effectiveness of monomial model for $\Gamma_{\rm rms}$

N	$\Gamma_{\rm rms}$ ($\times10^{-2}$)		N	$\Gamma_{\rm rms}$ ($\times10^{-2}$)	
	Eq.(30)	Eq.(31)		Eq.(30)	Eq.(31)
12	13.80	14.00	24	4.91	5.57
16	9.93	9.55	28	4.11	4.54
20	7.56	7.10	32	3.51	3.80

N: number of pairs

RTWOA design examples

All of the four cases were designed to cover a square chip with area of 5 mm×5 mm and the upper bounds were $A_{\rm tran\_max}=10^5$ μm^2, $A_{\rm MOS\_max}=500$ μm^2. The offset frequency of phase noise was 1 MHz. The target frequency varied from 8 to 10 GHz. We set a margin of 20% on target oscillation $f_{\rm osc}$, which meant $f_{\rm min}=0.9f_{\rm osc}$ and $f_{\rm max}=1.1f_{\rm osc}$. We compared our GP-based optimization results (GP) with the initialization routine (INIT) and the tune_wire routine (TUNE) of Yu and Liu (2007). The results showed that our GP method reduces power dissipation more than TUNE does. Moreover, all the design parameters can be generated automatically in less than 20 s using GP, while TUNE always takes over 10 ADS simulations to finish. Also, in contrast to TUNE, the results of our GP method are completely independent of the starting point. Several INIT parameters must be chosen based on empirical data, which greatly affects the results using TUNE. It is obvious that the efficiency of GP is much higher than that of the traditional heuristic method.

Table 4 shows the details of GP designs. It is obvious that the optimized designs have large separations and small widths, which helps to reduce the power dissipation. It is well known that the greater the distance between two lines, the higher the magnetic coupling. Eq.(23) also shows that minimizing the power dissipation maximizes inductive storage energy within the lines. The simulated frequencies from ADS (Sim.) and predicted frequencies from our model (Pred.) were in close agreement. The simulated phase noises and predicted phase noises also agreed very well (Table 4).

Trade-off analysis

In the trade-off analysis we varied the constraints to observe the impacts on the optimal value. This meant that many constraints were not fixed and could be changed according to the practical requirements. By repeatedly solving optimal design problems,

Table 3 Comparison of simulation frequency, power dissipation and phase noise among INIT, TUNE and GP

Case	Frequency spec. (GHz)	Simulation frequency			Power dissipation (mW)				PN (dBc/Hz)			
		INIT	TUNE	GP	INIT	TUNE	GP		INIT	TUNE	GP	
							Spec.	Achieved			Spec.	Achieved
1	7.2~8.8	8.10	8.15	8.13	113.0	97.1	Min.	79.4	−117.0	−117.3	≤−116	−117.1
2	8.1~9.9	9.23	9.06	8.92	87.0	77.8	Min.	65.4	−116.9	−117.0	≤−116	−116.9
3	9~11	10.20	10.10	9.83	85.5	69.5	Min.	56.3	−116.6	−117.1	≤−116	−116.4
4	9~11	10.20	9.87	10.25	85.5	77.0	≤70.0	70.0	−118.2	−118.5	Min.	−118.1

INIT: initialization routine; TUNE: tune_wire routine; GP: geometric programming; spec.: specification; PN: phase noise

Table 4 Details of the GP designs

Case	Design parameters								Frequency (GHz)		Frequency deviation (%)	PN (dBc/Hz)	
	w (μm)	s (μm)	l (μm)	$w_{\rm n}$ (μm)	$w_{\rm p}$ (μm)	nfin	N	$n_{\rm r}$	Sim.	Pred.		Sim.	Pred.
1	4.30	11.56	4962.4	1.03	4.02	7	12	2	8.13	7.80	4.05	−117.1	−116.8
2	4.73	12.72	4508.6	0.91	3.56	7	12	2	8.92	8.75	1.90	−116.9	−117.0
3	4.80	12.75	4472.1	1.03	4.06	5	12	2	9.83	9.73	1.01	−116.4	−116.6
4	10.00	24.72	2236.1	1.38	5.42	8	16	4	10.25	10.06	1.85	−118.1	−118.0

Sim.: simulated frequencies from ADS; Pred.: predicted frequencies from our model; PN: phase noise

we could obtain globally optimal trade-off curves of power dissipation and phase noise (Fig.7a). The horizontal axis gives the maximal phase noise allowed, and the vertical axis shows the minimum achievable power dissipation. A stricter phase noise constraint resulted in higher power dissipation. These curves give us an insight into the level of minimum power dissipation that would be obtained with a specific phase noise. The trade-off curves for other competing objectives were also computed. Fig.7b illustrates the trade-offs between power dissipation and chip area. Within a certain range, longer transmission lines led to less power dissipation. The trade-off curves between phase noise and the number of inverter pairs are plotted in Fig.7c. It appears that a greater number of inverter pairs gave better phase noise performance. However, all of the numbers of inverter pairs in Table 4 are below 20 because of the presence of other constraints, such as power dissipation. All of the curves mentioned above give us an overview of the circuit design.

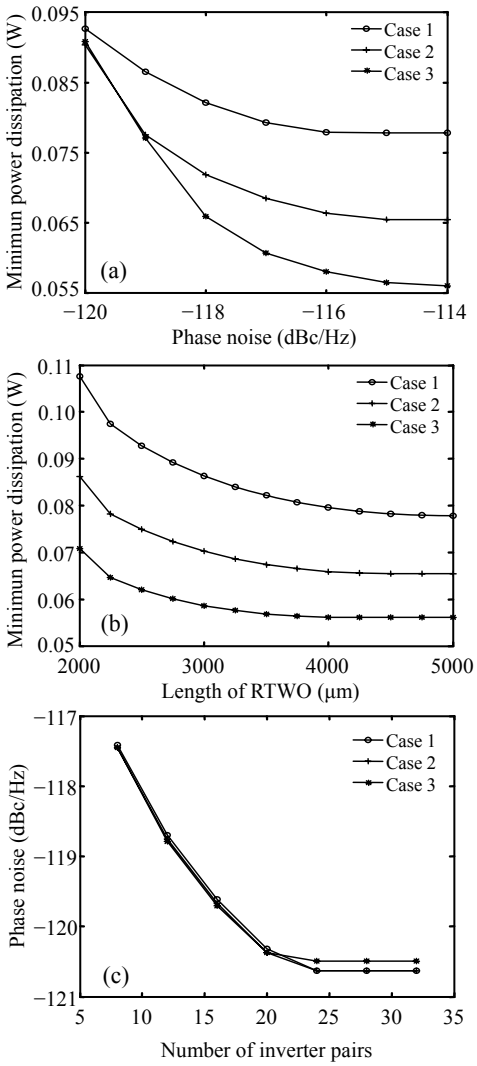

Fig.7 Trade-off curves of (a) power dissipation vs. phase noise, (b) power dissipation vs. length of RTWO, and (c) phase noise vs. the number of inverter pairs

CONCLUSION

In this paper, we propose a systematic methodology for the design of RTWOA. We first establish the posynomial models of various constraints based on fitted analytic expressions. The designer can choose to minimize any constraints to meet different design requirements. The design examples show that all the design variables can be optimized simultaneously at low computational cost. A large variety of circuit design problems can be solved using our proposed method.

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