Journal of Zhejiang University SCIENCE A
ISSN 1673-565X (Print); ISSN 1862-1775 (Online)
www.zju.edu.cn/jzus; www.springerlink.com
E-mail: jzus@zju.edu.cn

On-chip boost regulator with projected off- and on-time control*

Xiao-ru XU, Meng-lian ZHAO†‡, Xiao-bo WU

(*Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China*)

†E-mail: zhaoml@vlsi.zju.edu.cn

Received Mar. 19, 2009; Revision accepted June 12, 2009; Crosschecked June 17, 2009

Abstract: The boost type power supplies are widely used in portable consumer electronics to step up the input voltage to adapt for the high voltage applications like light-emitting diode (LED) driving and liquid crystal display (LCD) biasing. In these applications, a regulator with small volume, fewer external components and high efficiency is highly desired. This paper proposes a projected off- and on-time boost control scheme, based on which a monolithic IC with an on-chip VDMOS with 0.2 Ω on-state resistance $R_{DS\text{-}ON}$ was implemented in 1.5 μm bipolar-CMOS-DMOS (BCD) process. A 12 V, 0.3 A boost regulator prototype is presented as well. With projected off-time and modulated on-time in continuous conduction mode (CCM), a quasi fixed frequency, which is preferred for ripple control, is realized. With projected on-time and modulated off-time in discontinuous conduction mode (DCM), pulse frequency modulation (PFM) operation, which is beneficial to light load efficiency improvement, is achieved without extra control circuitry. Measurement results show that an efficiency of 3% higher than that of a conventional method under 0.5 W output is achieved while a step load transient response comparable to that of current mode control is maintained as well.

Key words: Boost regulator, Integrated circuits, Pulse frequency modulation, Projected off-time, Projected on-time
doi:10.1631/jzus.A0920160 **Document code:** A **CLC number:** TN4; TN86

INTRODUCTION

Boost dc-dc voltage regulators are widely used in portable consumer electronics systems, like light-emitting diode (LED) drivers and liquid crystal display (LCD) bias circuits. In these applications, a voltage regulator with fewer external components is desired for reducing the product size. High efficiency, which is closely related to battery life, is also an important consideration. Boost type power converters are intrinsically unstable as there are two conjugate poles and one right half plane (RHP) zero in the duty cycle to output transfer function (Erickson and Maksimovic, 2001). A conventional type III compensator needs a cross over frequency higher than the LC resonant frequency; otherwise, the filter will ring. But the RHP zero restricts the achievable crossover frequency. In 1978, the current mode control was introduced into power converters design (Deisch, 1978). A major drawback of the constant frequency current mode control is the well-known subharmonic oscillation. Inductor current slope compensation was proposed to solve this issue (Deisch, 1978). Unfortunately, this slope compensation significantly complicates the system analysis and controller design. Insufficient slope compensation will reduce the stable margin or even make it unstable when system parameters fluctuate. On the other hand, over designed slop compensation will degrade the current mode control to voltage mode control (Ridley, 1990).

Recently, hysteretic control has become popular in power converter design for its fast load transient response and no need for loop compensation. The discontinuous output current in a boost converter makes the hysteretic control more complex than that for a buck one. Several implementations of hysteretic control have been reported, but all solutions need additional external components (Nabeshima *et al*., 2005; Keskar and Rincon-Mora, 2008). Constant on-time control (COT) (Cardoso *et al*., 1992; Ling, 2007), an improved hysteretic control, is now developed for buck voltage regulator design, for it features

‡ Corresponding author

* Project (No. 90707002) supported by the National Natural Science Foundation of China

easy control to maintain frequency stability. Its counterpart for a boost converter has also been developed (Xu *et al*., 2008), but with the drawback of a certain number of equivalent serial resistors (ESRs) at the output capacitor which increases the output voltage ripple.

On the basis of the COT boost converter (Xu *et al*., 2008), this paper presents a projected off- and on-time control method without external ESR requirements. With the projected off-time control, the switch off-time is calculated based on the input and output voltage aiming at quasi fixed frequency operation in continuous conduction mode (CCM) as fixed frequency operation is preferred for ripple control. In consideration of efficiency in discontinuous conduction mode (DCM) operation, the projected on-time combined with modulated off-time enables the converter to run in pulse frequency modulation (PFM) operation automatically without additional control circuits.

PROPOSED CONTROL SCHEME

System block diagram

Fig.1 shows the system block diagram of the proposed boost regulator. Figs.2a and 2b are control waveforms in CCM and DCM, respectively. In CCM operation, e.g., with proposed projected off-time control, the switch off period T_{OFF} is prefixed at T_{POFF} by an on-chip timer. The output voltage programming signal V_P is subtracted by the inductor current information V_{IS} to generate a new control signal, V_{CTRL}. Then V_{CTRL} is compared with the feedback voltage to generate the boost switch on-time. In reference to Fig.2a, the switch off-time T_{OFF} of the previous switching cycle finishes at t_1, from where a new on period begins. Between t_1 and t_2, it is the projected on-time T_{PON}, but the actual on-time T_{ON} will last till V_{CTRL} reaches V_{FB}. It is always longer than T_{PON} in CCM just as its name—modulated on-time—indicates. Then, the V_{OC} will go high, and consequently the switch on-time is terminated and a new projected off-time will be triggered. Once the off period of the boost switch begins and the sensed voltage V_{IS} goes zero, V_{CTRL} will return to V_P abruptly, which helps to improve noise immunity. When T_{POFF} finishes, another modulated on-time will start as long as the output of the comparator remains low.

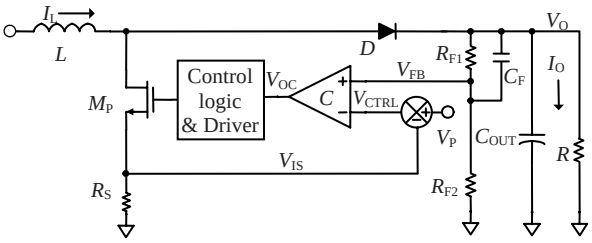

Fig.1 System block diagram of the proposed boost regulator

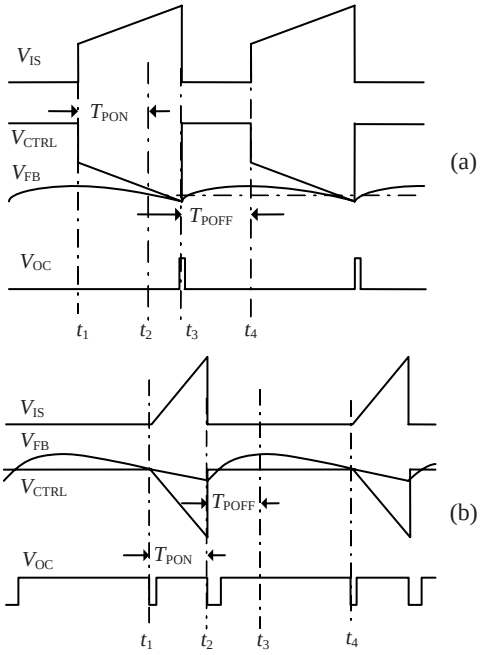

Fig.2 Control waveforms in CCM (a) and DCM (b)

Compared with conventional hysteretic control, the main advantage of this control method is that the inductor current needs sampling only during the boost switch on period. It can be simply implemented in a boost converter. As mentioned above, projected off-time is related to input and output voltage to reduce the frequency variation under CCM operation. Its implementation will be discussed in the following section.

As the load decreases, the power stage will finally run in DCM, and T_{ON} will also decrease. The relationship between load current I_O, off-time T_{OFF} and on-time T_{ON} in DCM is

$$T_{ON}=\frac{1}{V_{IN}^2}\left\{I_O L(V_O-V_{IN})+\left[I_O^2L^2(V_O-V_{IN})^2+2V_{IN}^2 I_O L T_{OFF}(V_O-V_{IN})\right]^{1/2}\right\}. \quad (1)$$

As shown in Eq.(1), assuming T_{OFF} is kept constant at about T_{POFF} (i.e., the projected off-time), T_{ON} becomes smaller and smaller as the load current I_O decreases. Hence, the converter efficiency will deteriorate since the switching frequency increases. In order to maintain high efficiency under light load condition, T_{ON} is clamped to T_{PON} while T_{OFF} is modulated in DCM to keep the charge balance of the external capacitor C_{OUT} (Fig.2b). The design criteria for projected on-time T_{PON} and projected off-time T_{POFF} will be discussed in the next section.

As a result, another advantage of the proposed control method is that, under light load condition, the minimum on-time T_{ON} is clamped to T_{PON} and the off-time will be modulated by the output ripple. In other words, the PFM operation under light load condition is realized, which increases the system efficiency without additional control circuitry.

Initial accuracy analysis

In power regulator design, the output voltage should be precisely regulated; that is to say, the relationship between program signal V_P and output voltage V_O should be well defined. However, there is a control error due to the coupling of V_O and inductor current V_{IS} in the feedback voltage.

When the load current is decreased, input current will be reduced correspondingly. Hence, the current signal in V_{CTRL} decreases as well. Consequently, V_{FB} will rise to fill the headroom, as shown in Fig.3. This phenomenon is like ripple induced load regulation. In Fig.1, with feedback programming resistors R_{F1} and R_{F2}, the relationship between the dc component of the feedback voltage V_{FBDC} and the output voltage V_O under CCM operation is given by

$$V_O = \frac{R_{F1} + R_{F2}}{R_{F2}} \times V_{FBDC}. \quad (2)$$

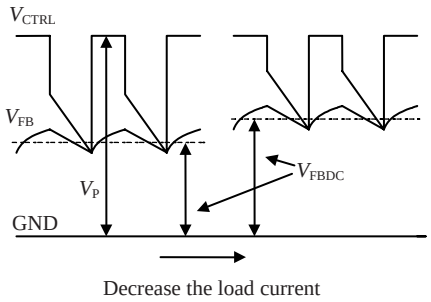

Fig.3 Feedback node waveforms with ripple induced load regulation

With conventional amplifier based feedback structure, V_{FBDC} should be equal to a precise reference voltage (e.g., V_P in Fig.1) in order to get an accurate output voltage. In the proposed control method, however, V_{FBDC} in CCM operation is given by

$$V_{FBDC} = V_P - V_{ISP} + V_R, \quad (3)$$

where V_{ISP} is the peak value of V_{IS}, and V_R is the dc component of the output voltage ripple. V_R is given by

$$V_R = \frac{T_{ON}}{12C_O}\left(\frac{T_{ON}(V_O - V_{IN})^3}{V_O L} + \frac{6I_O V_{IN}}{V_O - V_{IN}}\right). \quad (4)$$

From Eqs.(3) and (4), the relationship between V_P and V_O is predicted, and the load dependent V_{ISP} and V_R will introduce an error component between V_P and V_{FBDC}. This error voltage will be further amplified by the voltage divider composed of R_{F1} and R_{F2}, as demonstrated in Eq.(2). So programming voltage V_P is not appropriate to be the reference signal. For accurate output voltage regulation, an outer voltage loop is needed.

Outer voltage loop design

In order to overcome the problem of ripple induced load regulation, an external voltage loop is added to the basic boost regulator, as shown in Fig.4. An operational transconductance amplifier (OTA) senses the feedback voltage and compares it with an accurate reference voltage V_{REF}. The difference between them is then amplified as the error signal, which acts as the V_P signal in Fig.1. The new control waveforms are shown in Fig.5. By the negative feedback of the output voltage, V_P will be adjusted to keep the V_{FBDC} equal to V_{REF}. Thus the output voltage V_O is precisely controlled as in Eq.(2).

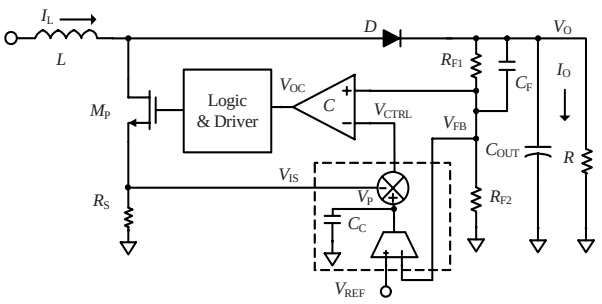

Fig.4 Proposed boost regulator with precise output voltage regulation

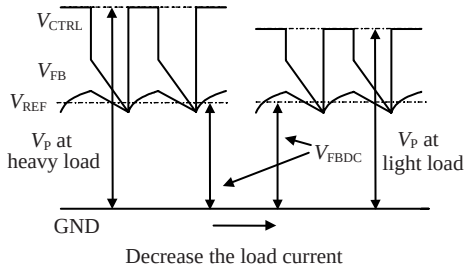

Fig.5 Feedback node waveforms without ripple induced load regulation

Parameters of the integrator should be chosen properly for keeping the converter stable. According to (Sable *et al*., 1990), the small signal control law at the boost switch prior to open instant is

$$\hat{V}_P - \hat{V}_{IS} = \hat{V}_O . \tag{5}$$

Based on the equivalent small signal model of current program control (Erickson and Maksimovic, 2001), the transfer function of inductor current to the output voltage is

$$\frac{\hat{V}_O}{\hat{V}_{IS}} = D' \times \frac{1 - \dfrac{sL}{(D')^2 R}}{2 + sRC_{OUT}} \times \frac{R}{R_S} . \tag{6}$$

Substituting Eq.(6) into Eq.(5) gives the transfer function from programming voltage V_P to V_O as

$$\frac{\hat{V}_O}{\hat{V}_P} = \frac{1 - s\dfrac{L}{(D')^2 R}}{1 + 2\dfrac{R_S}{R} + s\left(\dfrac{R_S C_{OUT}}{D'} - \dfrac{L}{(D')^2 R}\right)} . \tag{7}$$

Typically, for an on-chip boost regulator, load resistor R is much larger than R_S in Eq.(7). Thus, the dc gain from V_P to V_O is approximately equal to one. To keep the system stable, the current sensing resistor R_S should be larger than $L/(D'RC_{OUT})$ to keep the dominant pole located at the left half plane. For a physical understanding, the down slope of the current sensing signal should be larger than the capacitor voltage discharging slope during the switch on-time. Otherwise, V_{CTRL} will not cross over V_{FB} during on-time modulation.

Based on Eq.(7), setting the compensation pole, which is equal to $g_m/(2\pi C_C)$, below the dominant pole will secure sufficient phase margin and acceptable bandwidth of the system as the right half plane zero is typically located beyond the unit gain frequency.

Under light load DCM operation, compared with conventional current mode control, the error amplifier in the proposed control scheme never falls into the saturation region since its output contains a certain dc voltage to balance V_{FBDC}. This merit improves the dynamics of the transient response from extremely light load to heavy load since the control loop maintains a high loop gain and wide bandwidth.

CIRCUIT DESIGN

Control logic

According to the control logic described previously, the state-chart diagram of projected off- and on-time control is shown in Fig.6a. There are four states in a normal operation. During CCM operation, the state 'off-time modulation' will not occur, and the system runs in a sequence of S_1-S_3-S_4-S_1. While in PFM operation, the state S_4, on-time modulation, will not occur, and the system runs with S_1-S_2-S_3-S_1.

The synthesized control logic corresponding to the state chart is shown in Fig.6b. There are two timers, one for the projected off-time and the other for projected on-time. Take the T_{POFF} timer as an example. Once Q of L_2 is set low and the switch S_{OFF} is open, the controlled current source I_{OFF} will charge the capacitor C_{OFF}. When the voltage on C_{OFF} reaches the charging threshold voltage V_{THOFF}, the comparator outputs a low signal, which is applied on S of L_2, and S_{OFF} will be set high to terminate the T_{POFF} timing. T_{PON} is with the same structure. T_{POFF} and T_{PON} are controlled by the input and output voltage.

Projected off- and on-time generator

With fixed off-time duration, the switching frequency varies under different input and output voltage conditions. Power converters are typically designed to operate at a constant frequency in compliance with the usual industrial standards (Tan *et al*., 2008). A phase lock loop (PLL) is always needed to synchronize the switching frequency of the hysteretic controlled power converter with a reference clock (Grant, 2002; Tso and Wu, 2003), but on-chip PLL will complicate the circuit design and increase the die area. In this study, projected off-time control (Redl and

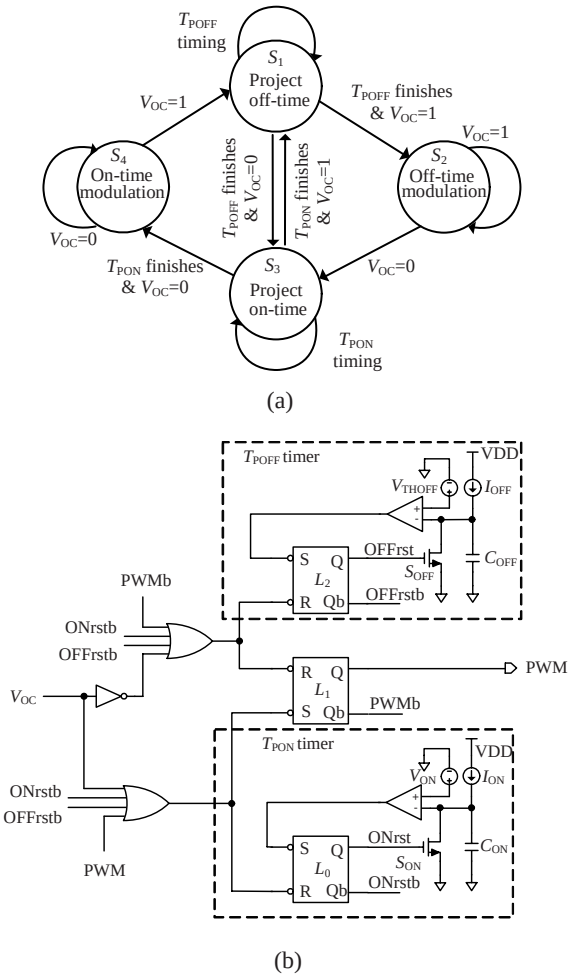

Fig.6 Logic design of the proposed control method
(a) State-chart diagram; (b) Synthesized finite state machine

Sokal, 1986) is adopted for CCM frequency stabilization. Besides, as frequency reduction is always employed in a power converter to improve the light load efficiency (Deng *et al*., 2005; Ferguson, 2006; Chen H.M. *et al*., 2007; Chen H. *et al*., 2008), projected on-time control is proposed during DCM to turn the converter into PFM operation.

Theoretically, for a boost converter with fixed switching period T_S in CCM operation, the boost switch off period T_{OFF} and on period T_{ON} should be

$$T_{ON} = T_S \times \frac{V_O - V_{IN}}{V_O}, \tag{8}$$

$$T_{OFF} = T_S \times \frac{V_{IN}}{V_O}, \tag{9}$$

which means that T_{OFF} is proportional to the input voltage while inversely proportional to the output voltage. One embodiment to generate the T_{POFF} and T_{PON} is shown in Fig.7. The instantaneous input and output voltages are converted into current signals, and then the voltage subtraction in Eq.(8) is implemented by the subtraction of their corresponding currents. As a result, the charging threshold for the off-timer shown in Fig.7 is given by

$$V_{THOFF} = \frac{V_{IN}}{K_1}. \tag{10}$$

And the charging current I_{OFF} will be

$$I_{OFF} = \frac{K_2 V_O}{K_1 R_T}. \tag{11}$$

Finally the timing constant T_{POFF} of the off-timer is calculated:

$$T_{POFF} = \frac{V_{THOFF} C_{OFF}}{I_{OFF}}. \tag{12}$$

Substituting Eqs.(10) and (11) into Eq.(12) yields

$$T_{POFF} = \frac{R_T C_{OFF}}{K_2} \times \frac{V_{IN}}{V_O}. \tag{13}$$

Comparing Eq.(13) with Eq.(8), if the term $R_T C_{OFF}/K_2$ is set equal to T_S, then the designed converter will operate at the quasi fixed frequency under CCM operation.

The projected on-time is implemented in a similar way. In Fig.7, the timing constant T_{PON} of the on-timer is

$$T_{PON} = \frac{K_4 R_T C_{ON}}{K_3} \times \frac{V_O - V_{IN}}{V_O}. \tag{14}$$

The on-time should be modulated in CCM operation to avoid subharmonic oscillation. Thus, T_{PON} in Eq.(14) is designed smaller than T_{ON} in Eq.(8). In other words, $K_4 R_T C_{ON}/K_3$ is set equal to $K_5 T_S$ with K_5 smaller than one. Since a small K_5 degrades the PFM performance, in this design, a coefficient of 0.8 was used to avoid subharmonic oscillation and to ensure acceptable PFM performance.

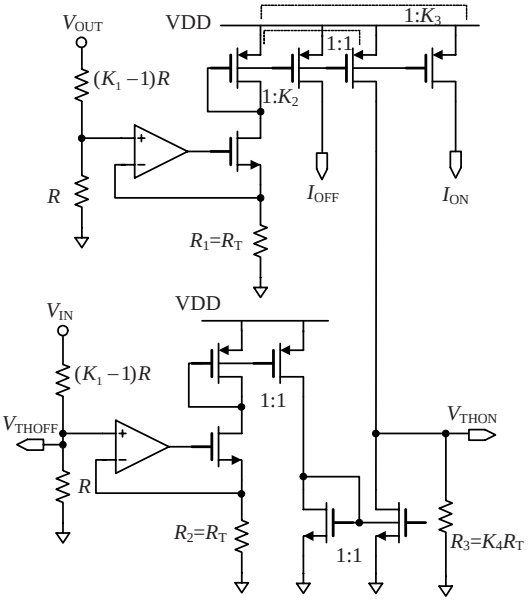

Fig.7 T_{POFF} and T_{PON} generator

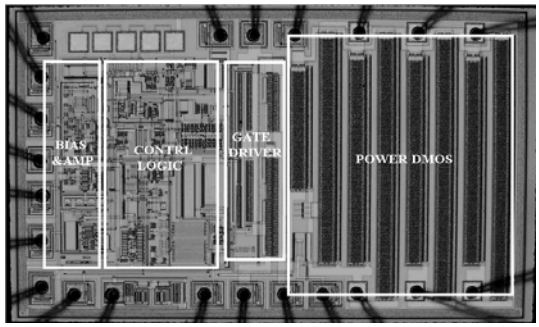

Fig.8 The microphotography of the fabricated chip

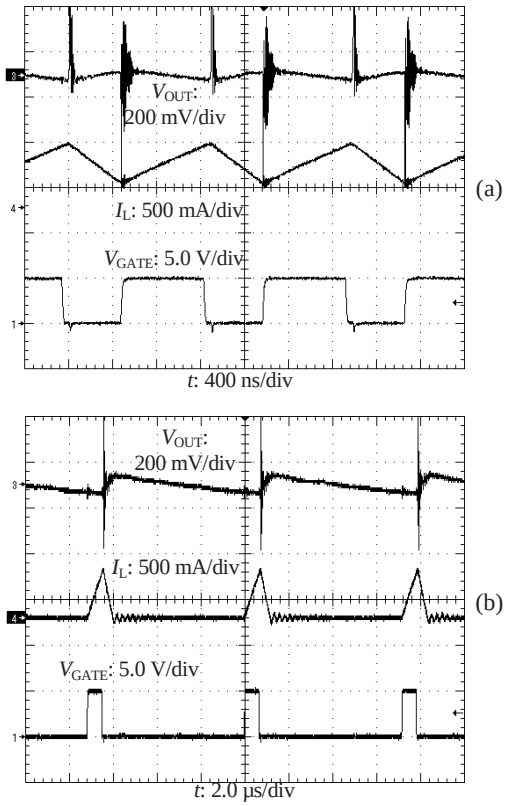

Fig.9 Switching node waveforms in CCM operation (a) and DCM operation (b)

EXPERIMENTAL RESULTS

Based on the proposed control scheme, a boost voltage regulator with a power MOSFET on chip was fabricated in 1.5 μm BCD process. An on-chip DMOS with 5400 cells or 200 mΩ $R_{DS\text{-}ON}$ was used as the boost power switch. Fig.8 shows the microphotography of the fabricated chip. Two demo boards were built with the final chip. One was with the proposed solution. The other was with a current mode boost controller, LM3488, from National Semiconductor (LM3488 Datasheet, 2009). Both of them employed the on-chip DMOS (its source, drain, and gate are all bonded out for external connection). System parameters for the proposed design are listed in Table 1.

Table 1 Summary of parameters used in measurements

Parameter	Value	Parameter	Value
V_{IN} (V)	5	C_{OUT} (μF)	2.8
V_{OUT} (V)	12	L (μH)	10.0
I_O (A)	0.3	R_S (Ω)	0.3
f_S (kHz)	780		

Steady state

Fig.9 gives the steady-state switching node waveforms. Under heavy-load condition, the boost regulator will run in CCM and the corresponding waveforms are presented in Fig.9a. The upper trace is the output voltage ripple, the middle trace is the inductor current, and the bottom trace is the gate drive signal. The switching period in CCM was measured to be about 1.28 μs with T_{OFF} of 496 ns (equal to T_{POFF}) and T_{ON} of 784 ns. Decreasing the load current will turn the operation mode to DCM and PFM will occur as shown in Fig.9b. The switching period was about 7 μs, and T_{OFF} was about 6.38 μs, much longer than T_{POFF}. T_{ON} in PFM was clamped at about 620 ns, approximately 0.8 times the 784 ns T_{ON} in CCM,

which is just as expected. As mentioned previously, in PFM operation, the off-time was modulated to keep the charge balance of the output capacitor.

Fig.10 gives the frequency control performance under CCM operation. The solid lines are with the proposed projected off-time control while the dashed lines are with a fixed 340 ns off-time. With projected off-time control, the operation frequency under different input and output voltages are much more stable.

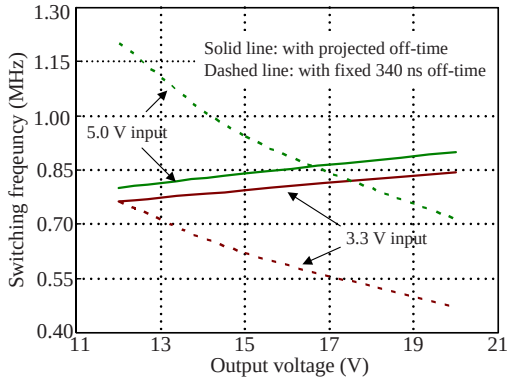

Fig.10 Frequency control performance with proposed projected off-time

Transient response

Fig.11a shows the load transient response of the proposed solution compared with the reference design. The reference design was with C_C and R_C of 16 nF and 2.2 kΩ respectively, which resulted in a 30 kHz crossover frequency and roughly 60° of phase margin. For the proposed design, the time constant of $g_m/(2\pi C_C)$ was set to about 30 kHz, which is a little lower than the dominant pole in Eq.(7). The load step was realized by an electronics load with current steps of 0.03-0.27-0.03 A. As shown by the output voltage and inductor current waveforms, the transient response of the proposed method is better than that of LM3488. This improvement mainly benefits from the linearly operated error amplifier. Another load transient from no-load condition to full load is shown in Fig.11b. And PFM operation in light load of the proposed solution is much more obvious compared with that in Fig.11a.

Efficiency

The comparison of efficiency between the proposed boost regulator and the reference design is shown in Fig.12. The LM3488 was with a minimum

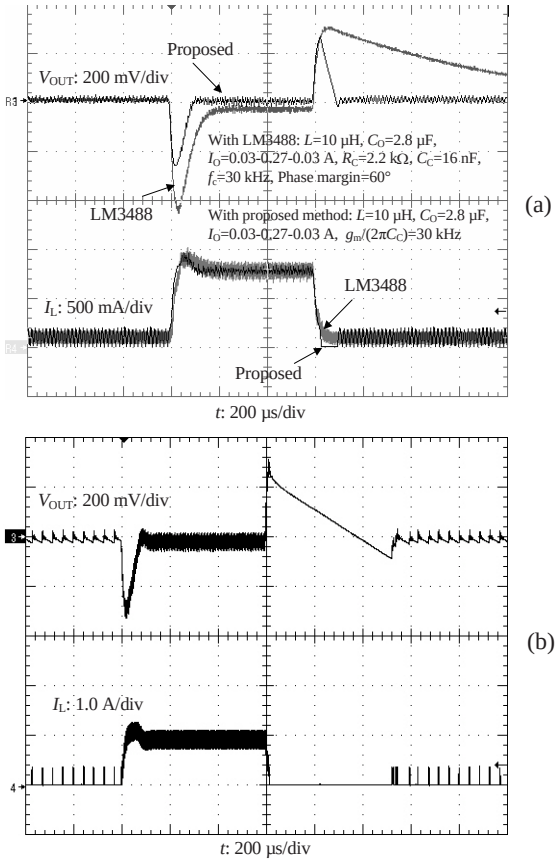

Fig.11 Load transient response compared with LM3488 based current mode control (a) and with zero to full load step test (b)

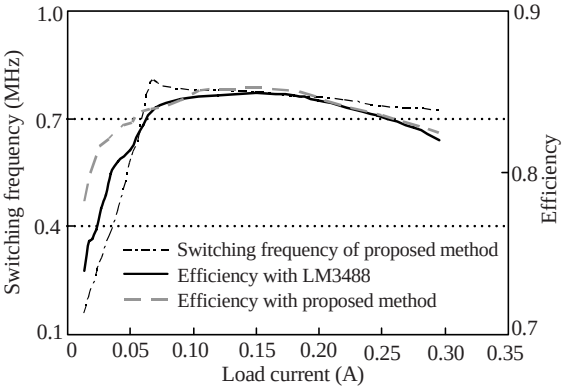

Fig.12 Efficiency comparison of the proposed method and LM3488

of about 325 ns on-time. If the output load was below 5%, due to the intermittent saturation of the error amplifier, the pulse skip mode will also occur. However, this mode was achieved at the expense of lower loop gain and worse load step transient response as shown in Fig.11a.

Back to the efficiency comparison, if the load was higher than 65 mA, both the two systems ran in CCM operation and the frequencies were all around 750 kHz. As a result, the two systems show the similar curve of efficiency vs load. However, for the load condition between 15 and 65 mA, the proposed system ran in PFM operation and the frequency decreased linearly with load current, and its efficiency performance was better than that in the reference design which still ran at a fixed frequency.

CONCLUSION

This paper presents a novel boost regulator based on projected off- and on-time control. Projected off-time of the regulator in CCM was implemented to keep the converter run at a quasi fixed frequency. Under light load condition, the projected on-time adaptively clamped the switch on-time to a minimum value to realize a highly efficient PFM operation. The proposed control method was applied to an on-chip boost voltage regulator with a die area of 2.54 mm× 1.52 mm. With the chip, a 5 V input, 12 V, 0.3 A output demo board was built. Experimental results showed that the proposed on-chip boost regulator works well in both CCM and DCM. The load transient response better than that of the conventional current mode control was achieved. Besides, the light load efficiency of the proposed regulator was much higher than that with fixed frequency current mode control.

References

Cardoso, B.J., Moreira, A.F., Menezes, B.R., Cortizo, P.C., 1992. Analysis of Switching Frequency Reduction Methods Applied to Sliding Mode Controlled DC-DC Converters. Proc. IEEE Applied Power Electronics Conf. and Expo, p.403-410. [doi:10.1109/APEC.1992.228382]

Chen, H., Zhao, M.L., Wu, X.B., Yan, X.L., 2008. Multi-mode controller IC for soft-switched flyback converter with high efficiency over the entire load range. *J. Zhejiang Univ. Sci. A*, **9**(10):1411-1419. [doi:10.1631/jzus.A0820142]

Chen, H.M., Chang, R.C., Huang, C.L., 2007. Low-voltage Zero Quiescent Current PFM Boost Converter for Portable Devices. IEEE Int. SOC Conf., p.177-180. [doi:10.1109/SOCC.2007.4545453]

Deisch, C.W., 1978. Simple Switch Control Method Changes Power Converter into a Current Source. Proc. IEEE Power Electronics Specialists Conf., p.300-306.

Deng, H.F., Duan, X.M., Sun, N., Huang, A.Q., Chen, D., 2005. Monolithically integrated boost converter based on 0.5-μm CMOS process. *IEEE Trans. Power Electr.*, **20**(3):628-638. [doi:10.1109/TPEL.2005.846551]

Erickson, R.W., Maksimovic, D., 2001. Fundamentals of Power Electronics (2nd Ed.). Kluwer Academic Publishers, Norwell, Massachusetts, p.193-302, 439-454.

Ferguson, B.R., 2006. Dual-mode PFM Boost Converter. US Patent, 7 102 340.

Grant, D., 2002. Frequency Control of Hysteretic Power Converter by Adjusting Hysteresis Levels. US Patent, 6 348 780.

Keskar, N.A., Rincon-Mora, G.A., 2008. A fast, sigma-delta (ΣΔ) boost DC-DC converter tolerant to wide LC filter variations. *IEEE Trans. Circuits-II: Expr. Briefs*, **55**(2):198-202. [doi:10.1109/TCSII.2007.910801]

Ling, H.S., 2007. Apparatus and Method for Flywheel Current Injection for a Regulator. US Patent, 7 221 134.

LM3488 Datasheet, 2009. National Semiconductor. Available from: http://www.national.com/ds/LM/LM3488.pdf [Accessed 18/03/09].

Nabeshima, T., Sato, T., Nishijima, K., Yoshida, S., 2005. A Novel Control Method of Boost and Buck-boost Converters with a Hysteretic PWM Controller. Proc. IEEE European Conf. on Power Electronics and Application, p.1-6. [doi:10.1109/EPE.2005.219398]

Redl, R., Sokal, N.O., 1986. Frequency Stabilization and Synchronization of Free-running Current-mode-controlled Converters. Proc. IEEE Power Electronics Specialists Conf., p.519-530.

Ridley, R.B., 1990. A New Continuous-time Model for Current-mode Control with Constant Frequency, Constant On-time, and Constant Off-time, in CCM and DCM. 21st Annual IEEE Conf. on Power Electronics Specialists, p.382-389. [doi:10.1109/PESC.1990.131213]

Sable, D.M., Cho, B.H., Ridley, R.B., 1990. Elimination of the Positive Zero in Fixed Freqeuncy Boost and Flyback Converters. Fifth Annual Proc. on Applied Power Electronics Conf. and Exposition, p.205-211. [doi:10.1109/APEC.1990.66413]

Tan, S.C., Lai, Y.M., Tse, C.K., 2008. General design issues of sliding-mode controllers in DC-DC converters. *IEEE Trans. Ind. Electron.*, **55**(3):1160-1174. [doi:10.1109/TIE.2007.909058]

Tso, C.H., Wu, J.C., 2003. A ripple control buck regulator with fixed output frequency. *IEEE Power Electron. Lett.*, **1**(3):61-63. [doi:10.1109/LPEL.2003.819643]

Xu, X.R., Wu, X.B., Yan, X.L., 2008. A Quasi Fixed Frequency Constant on Time Controlled Boost Converter. Proc. IEEE Int. Symp. on Circuits and Systems, p.2206-2209. [doi:10.1109/ISCAS.2008.4541890]