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Discrete-time charge analysis for a digital RF charge sampling mixer*

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Abstract: This paper presents an approach for analyzing the key parts of a general digital radio frequency (RF) charge sampling mixer based on discrete-time charge values. The cascade sampling and filtering stages are analyzed and expressed in theoretical formulae. The effects of a pseudo-differential structure and CMOS switch-on resistances on the transfer function are addressed in detail. The DC-gain is restrained by using the pseudo-differential structure. The transfer gain is reduced because of the charge-sharing time constant when taking CMOS switch-on resistances into account. The unfolded transfer gains of a typical digital RF charge sampling mixer are analyzed in different cases using this approach. A circuit-level model of the typical mixer is then constructed and simulated in Cadence SpectreRF to verify the results. This work informs the design of charge-sampling, infinite impulse response (IIR) filtering, and finite impulse response (FIR) filtering circuits. The discrete-time approach can also be applied to other multi-rate receiver systems based on charge sampling techniques.

Key words: Digital RF, Charge sampling, Discrete-time, Pseudo-differential, Switch-on resistance
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1 Introduction

CMOS technology has greatly improved the degree of integration within a single chip (Abidi, 2004). Compared with a full digital system-on-chip (SoC), RF analog circuits are incompatible with digital baseband parts usually operated by distributed multi-processors when designing SoCs for reconfigurable wireless application (Muhammad *et al.*, 2005). It is extremely challenging to achieve the high integration for mixed-signal SoC most often used in wireless applications. A fully digitized solution for the conventional software radio system is difficult to achieve for deep-submicron CMOS technologies currently available. A number of alternative mixed-signal circuit architectures have been proposed to solve this issue. A novel RF receiving technique named digital RF involving digital features has been proposed by Texas Instruments (Muhammad and Staszewski, 2004; Staszewski *et al.*, 2004). Direct RF charge sampling techniques used in the generation of commercial single-chip Bluetooth radio allow a greater flexibility to configure sampling and filtering features. A wideband software-defined radio receiver has become reconfigurable multi-band and multi-channel benefited from the similar charge sampling and switch-capacitor approaches (Bagheri *et al.*, 2006). An approach for integrating complex FIR and IIR filtering into a sampler of receiver has been presented by Karvonen *et al.* (2006). Digital RF techniques based on digital signal processing can improve high integration, as well as reconfiguration and flexibility, but also reduce cost and power consumption.

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Based on recent fundamental theories of digital RF working principles, some attractive advantages of charge sampling over voltage sampling have been discussed by Xu and Yuan (2000). Staszewski *et al*. (2005) and Ho *et al.* (2006) presented the ideal formulae for some parts of the digital RF charge sampling mixer. They did not, however, consider the impact of CMOS switch-on resistances when analyzing the filtering functions. Xu and Yuan (2005) included the factor of CMOS switch-on resistances between drain and source when analyzing circuit noise performance during the charge sampling process. Chen *et al.* (2007) analyzed the incomplete charge sharing problem based on the work of others (Staszewski *et al.*, 2005; Xu and Yuan, 2005; Ho *et al.*, 2006) who analyzed various aspects of digital RF circuits using continuous-time domain or frequency-domain methods of traditional analog RF analysis. Digital RF techniques have special properties, however, compared to analog RF. Digital circuits are used in RF design to help reduce the complexity of the receiver system, and improve the flexibility of reconfiguration. Therefore, the mixed architecture of digital RF requires new approaches to support circuit analysis. Discrete-time signal processing in down-sampling and filtering is one of the most important features of digital RF, different from traditional RF.

In this paper, an approach based on discrete-time charge signal processing is presented to analyze digital RF charge sampling mixers. Discrete-time charge signals, instead of continuous-time voltages, are used for analyzing the characteristics of digital RF mixers. This approach provides the basic theory for analyzing RF front-end including integration, sampling, and filtering in digital domain. Hence, the whole system of software-defined receivers, including digital RF front-end with baseband, can be described easily in unified digital form, which is helpful for architecture optimization, evaluation, and reconfiguration of receivers. The effects of the pseudo-differential structure and CMOS switch-on resistances on unfolded transfer gains are addressed in detail using this discrete-time method. Furthermore, the unfolded transfer gain of a typical digital RF mixer is also achieved through a mixed-signal circuit model constructed in Cadence SpectreRF to verify the proposed approach.

2 Digital RF charge sampling mixer architecture

A typical architecture of digital RF charge sampling mixers can be summarized as four circuit parts composed of a low-noise trans-conductance amplifier (LNTA), a sampling switch, a switch-capacitor (SC) filter and a digital control unit (DCU) (Fig. 1). The RF voltage signal received is amplified by the LNTA and consequentially converted to RF current signal. Then the current signal is split into I/Q paths and integrated on a sampling capacitor at the local oscillator (LO) rate. The sampling rate of the charge signal is decreased to intermediate frequency (IF) through successive decimations under the control of the DCU. The SC filter provides necessary anti-aliasing filtering to guarantee receiving specifications. In general, the SC is reset and pre-charged to a desired voltage to compensate DC-offset at the beginning of charge sampling. A group of multi-rate and multi-phase clocks generated by the DCU are used to control the SC to implement right decimating and filtering functions. The values of the capacitors and clock frequencies are determined by a trade-off analysis of anti-aliasing specifications, receiving bandwidth, sampling rates, noise figures and so on.

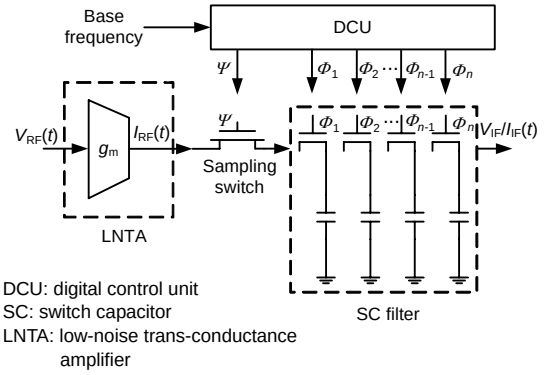

Fig. 1 Architecture of a general digital RF charge sampling mixer

3 Discrete-time charge value analysis approach

As Fig. 1 shows, the received, desired signals of a digital RF charge sampling mixer are transmitted and handled mainly in the form of charges stored in capacitors. The charge values at any sampling instant

are important for analyzing and evaluating the transfer functions of the digital RF receiver. At any other time they are not too much a concern. Analysis of the received charge signals is based on discrete-time at the sampling instant. According to sampling theorems, this approach reduces the complexity of evaluating the transfer function in continuous-time domain while keeping the same results. In this section, an analysis is carried out for pseudo-differential integration and sampling, and switch-capacitor filtering. Then, the unfolded transfer gain of a typical digital RF charge sampling mixer is presented.

3.1 Pseudo-differential charge integration and sampling

The signal processing of pseudo-differential charge integration and sampling is composed of the LNTA with the sampling switch, the former two stages of the general digital RF charge sampling mixer shown in Fig. 1. The typical architecture in real circuits for the implementation of this signal processing is shown in Fig. 2 where g_m is the trans-conductance gain, C_s is the sampling capacitor and $V_{RF}(t)$ is the received RF voltage.

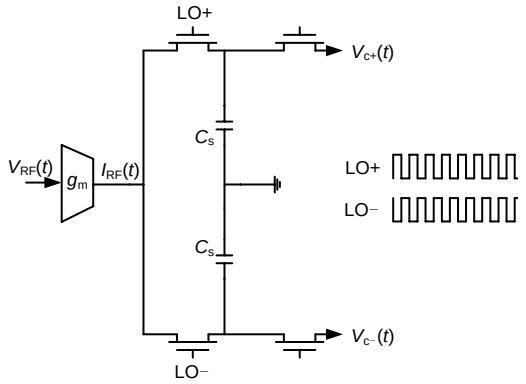

Fig. 2 Typical architecture of the pseudo-differential charge integration and sampling

Let T_s be the LO period, and σ be the continuous integration time in a sampling period. The output voltage $V_{c+}(t)$ of the positive half-circuit can be expressed as

$$V_{c+}(nT_s+\sigma)=\frac{g_m}{C_s}\int_{nT_s}^{nT_s+\sigma}V_{RF}(t)\mathrm{d}t,\ 0\le\sigma\le T_s. \quad (1)$$

The discrete-time method mentioned above is used to analyze the circuit. The values of the accumulated charge on the sampling capacitor needed to be concerned are only located at each sampling instant nT_s. An impulse train $V_{nc+}(t)$ with the coefficient amplitudes of the impulses equal to the samples of $V_{c+}(t)$ at any sampling instant nT_s is constructed. It means $V_{nc+}(t)$ has contains all useful charge information of $V_{c+}(t)$ in discrete-time domain. Therefore, from Eq.(1), $V_{nc+}(t)$ can be expressed as

$$V_{nc+}(t)=\frac{g_m}{C_s}\left(V_{RF}(t)\otimes h(t)\right)\sum_{n=-\infty}^{+\infty}\delta(t-nT_s), \quad (2)$$

where $h(t)$ is the intermediate variable, which is given by

$$h(t)=\begin{cases}1, & 0\le t\le\sigma,\\ 0, & \text{elsewhere.}\end{cases} \quad (3)$$

As the same principle, the output voltage $V_{nc-}(t)$ of the negative half-circuit can be expressed as

$$V_{nc-}(t)=\frac{g_m}{C_s}\left(V_{RF}(t-T_s/2)\otimes h(t)\right)\sum_{n=-\infty}^{+\infty}\delta(t-nT_s). \quad (4)$$

Therefore, the output voltage of the pseudo-differential charge integration and sampling can be expressed as

$$V_{pseudo}(t)=\frac{g_m}{C_s}\left(V_{RF}(t)\otimes h_p(t)\right)\sum_{n=-\infty}^{+\infty}\delta(t-nT_s), \quad (5)$$

where $h_p(t)$ is given by

$$h_p(t)=h(t)-h(t-T_s/2). \quad (6)$$

The transfer function in frequency-domain is

$$H_p(f)=\frac{(1-\mathrm{e}^{-\mathrm{j}2\pi f\sigma})^2}{\mathrm{j}2\pi f}, \quad (7)$$

where $\sigma=T_s/2$. The output charge at discrete-time sampling instants can be expressed in frequency-domain as

$$V_{pseudo}(f)=\frac{g_m}{T_sC_s}\sum_{k=-\infty}^{+\infty}V_{RF}(f-kf_s)H_p(f-kf_s), \quad (8)$$

where $f_s=1/T_s$.

Considering the base-band frequency when k=0 in Eq. (8), the transfer gain in frequency-domain is shown in Fig. 3. The maximum gain is located at $0.74f_s$. As Fig. 3 shows, the amplification rate of the transfer gain from zero frequency to −3 dB frequency is close to 20 dB/dec, while the attenuation rate for the envelop curve of the side-band peak is equal to −20 dB/dec. The charge integration and sampling pre-provides partial anti-alias filtering for the digital RF charge sampling mixer besides sampling and mixing. Compared with the analysis by Xu and Yuan (2005), the DC-gain is reduced by about 60 dB as the result of the pseudo-differential architecture, and the bandwidth of −3 dB is about $0.8f_s$.

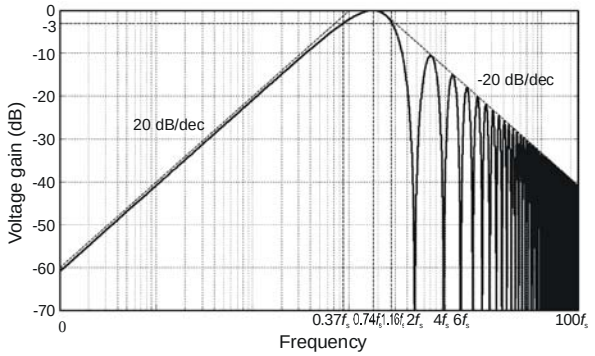

Fig. 3 Transfer gain of the pseudo-differential charge integration and sampling

3.2 Switch-capacitor filter with switch-on resistances

The SC filter is the main part of a general digital RF charge sampling mixer, which provides anti-alias filtering and decimating through transmitting charges stored on one capacitor to another sequentially under the control of the DCU. The CMOS switches of the SC filter circuit have switch-on resistances between drain and source (Xu and Yuan, 2005; Chen *et al.*, 2007). However, the effects of CMOS switch-on resistances are generally omitted for the complexities of analysis and computation. The FIR and IIR filtering processes described by Staszewski *et al.* (2005) and Ho *et al.* (2006) should be re-formulated when the switch-on resistances are not negligible. We also adopt this analysis method in discrete-time domain to reduce analysis complexities, and achieve more precise results by considering the effects of CMOS switch-on resistances, because only the charge at each sampling instant is useful for the final output of the SC filter.

3.2.1 Temporal moving average circuit

The typical SC filter of a general digital RF charge sampling mixer is composed of the temporal moving average (TMA) circuit and the spatial moving average (SMA) circuit. A typical positive half-circuit with corresponding switch control timing of TMA circuits is shown in Fig. 4. The charge and readout operations are cyclically rotated on m rotating capacitors. The switches are turned on one-by-one from Φ_1 to Φ_m. This architecture guarantees that a certain rotating capacitor will be in the operation of integration and readout every N LO cycles. The whole operation is repeated every mN LO cycles. Let C_H, C_R, and R_{on} be the history capacitor, the rotating capacitor, and the CMOS switch-on resistance, respectively. Let $Q_{CH}(t)$ and $Q_{CR}(t)$ be the charge values of the history capacitor and the rotating capacitor. The period of LO in Fig. 4 is T_s.

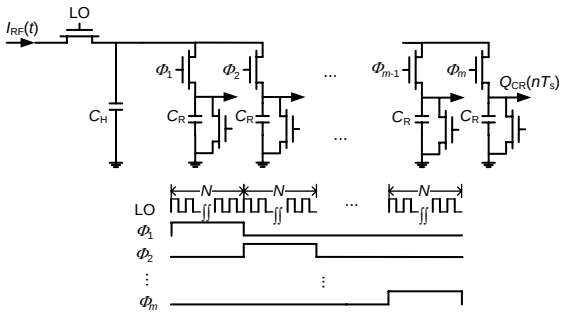

Fig. 4 Typical positive half-circuit of temporal moving average (TMA)

According to the Kirchhoff theorem, the circuit shown in Fig. 4 has a set of equations as follows:

$$Q_{CH}(nT_s+\sigma)=\int_{nT_s}^{nT_s+\sigma}\lambda(nT_s+\sigma-t)I_{RF}(t)\mathrm{d}t + \lambda(nT_s+\sigma)[Q_{CH}(nT_s)+Q_{CR}(nT_s)], \tag{9}$$

$$Q_{CR}(nT_s+\sigma)=\int_{nT_s}^{nT_s+\sigma}\beta(nT_s+\sigma-t)I_{RF}(t)\mathrm{d}t + \beta(nT_s+\sigma)[Q_{CH}(nT_s)+Q_{CR}(nT_s)], \tag{10}$$

$$\lambda(t)=\frac{C_H}{C_H+C_R}\left(1+\frac{C_R}{C_H}\mathrm{e}^{-t/\tau}\right), \tag{11}$$

$$\beta(t)=\frac{C_R}{C_H+C_R}(1-\mathrm{e}^{-t/\tau}), \tag{12}$$

where the time constant of charge sharing τ is given by $\tau=C_HC_RR_{on}/(C_H+C_R)$, and $I_{RF}(t)$ is the

received RF current. Let $q_{CH}(t)$ and $q_{CR}(t)$ be the charges accumulated on C_H and C_R during one sampling period, respectively. From Eqs. (9) and (10), they can be expressed as

$$q_{CH}(nT_s+\sigma)=\int_{nT_s}^{nT_s+\sigma}\lambda(nT_s+\sigma-t)I_{RF}(t)\mathrm{d}t, \quad (13)$$

$$q_{CR}(nT_s+\sigma)=\int_{nT_s}^{nT_s+\sigma}\beta(nT_s+\sigma-t)I_{RF}(t)\mathrm{d}t. \quad (14)$$

Because the charges stored on the capacitors are calculated at sampling instants, the accumulated charges during one sampling period, when $\sigma=T_s/2$, can be rewritten in frequency-domain as

$$q_{CH}(f)=\sum_{k=-\infty}^{+\infty}I_{RF}(f-kf_s)H_\lambda(f-kf_s), \quad (15)$$

$$q_{CR}(f)=\sum_{k=-\infty}^{+\infty}I_{RF}(f-kf_s)H_\beta(f-kf_s), \quad (16)$$

where

$$H_\lambda(f)=\frac{C_H}{C_H+C_R}\left(h(f)+\frac{C_R}{C_H}h\left(f-\frac{\mathrm{j}}{2\pi\tau}\right)\right), \quad (17)$$

$$H_\beta(f)=\frac{C_R}{C_H+C_R}\left(h(f)-h\left(f-\frac{\mathrm{j}}{2\pi\tau}\right)\right), \quad (18)$$

$$h(f)=\frac{1-\mathrm{e}^{-\mathrm{j}2\pi f\sigma}}{\mathrm{j}2\pi f}. \quad (19)$$

Therefore, from Eqs. (9) and (10), the charges on the history capacitor and rotating capacitor of TMA in discrete-time domain is expressed as

$$Q_{CH}(j)=\sum_{i=0}^{N-1}q_{CH}(j-i)+\lambda(NT_s)Q_{CH}(j-1), \quad (20)$$

$$Q_{CR}(j)=\sum_{i=0}^{N-1}q_{CR}(j-i)+\beta(NT_s)Q_{CH}(j-1). \quad (21)$$

Considering the baseband frequency when k=0, the transfer gain of the typical TMA is

$$H_{TMA}(f)=H_C(f)H_{FIR\text{-}T}(f)H_{IIR\text{-}T}(f), \quad (22)$$

where

$$H_C(f)=\mathrm{e}^{-\mathrm{j}2\pi fNT_s}[\beta(NT_s)H_\lambda(f)-\lambda(NT_s)H_\beta(f)]+H_\beta(f), \quad (23)$$

$$H_{FIR\text{-}T}(f)=\frac{1-\mathrm{e}^{-\mathrm{j}2\pi fNT_s}}{1-\mathrm{e}^{-\mathrm{j}2\pi fT_s}}, \quad (24)$$

$$H_{IIR\text{-}T}(f)=\frac{1}{1-\lambda(NT_s)\mathrm{e}^{-\mathrm{j}2\pi fNT_s}}. \quad (25)$$

Obviously, the filtering of the typical TMA can be regarded as the cascade of the amendatory charge sampling, and FIR and IIR filtering.

3.2.2 Spatial moving average circuit

Fig. 5 shows the typical positive half-circuit SMA of a general charge sampling mixer. The input charge is cyclically integrated on M rotating capacitors after being cleared in a row every time Ψ is at a low level. When Ψ is at a high level, M rotating capacitors place their stored charges into the buffer capacitor together, under the control of IF. Analysis of this circuit in discrete-time domain is similar in principle to that of the TMA.

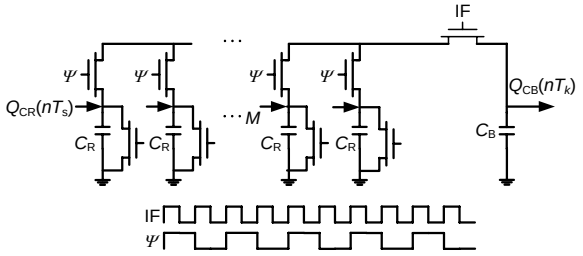

Fig. 5 Typical positive half-circuit of spatial moving average (SMA)

In Fig. 5, C_R and C_B indicate the rotating capacitor and the buffer capacitor, respectively. The equivalent rotating capacitor $C_{MR}=MC_R$ represents the parallelism of M rotating capacitors. Let $Q_{CR}(t)$ and $Q_{CB}(t)$ be the charge values of C_{MR} and C_B, respectively. The period of IF in Fig. 5 is T_k. Similar to the TMA formulated as Eqs. (9)–(19), the charges on the equivalent rotating capacitor and buffer capacitor are

$$Q_{CR}(j)=\chi(T_k/2)\left(Q_{CB}(j-1)+\sum_{i=0}^{M-1}Q_{CR}(j-i)\right)+\nu(T_k/2)\left(\sum_{i=0}^{M-1}Q_{CR}(j-i)-MQ_{CB}(j-1)\right), \quad (26)$$

$$Q_{CB}(j)=\gamma(T_k/2)\left(Q_{CB}(j-1)+\sum_{i=0}^{M-1}Q_{CR}(j-i)\right)+\nu(T_k/2)\left(MQ_{CB}(j-1)-\sum_{i=0}^{M-1}Q_{CR}(j-i)\right), \quad (27)$$

$$\chi(t)=\frac{MC_{\mathrm{R}}}{MC_{\mathrm{R}}+C_{\mathrm{B}}}\left(1-\frac{C_{\mathrm{R}}-C_{\mathrm{B}}}{C_{\mathrm{R}}(M+1)}\mathrm{e}^{-t/\mu}\right), \quad (28)$$

$$\gamma(t)=\frac{C_{\mathrm{B}}}{MC_{\mathrm{R}}+C_{\mathrm{B}}}\left(1-\frac{M(C_{\mathrm{B}}-C_{\mathrm{R}})}{C_{\mathrm{B}}(M+1)}\mathrm{e}^{-t/\mu}\right), \quad (29)$$

$$\nu(t)=\frac{1}{M+1}\mathrm{e}^{-t/\mu}, \quad (30)$$

where the time constant $\mu=\dfrac{(M+1)C_{\mathrm{B}}C_{\mathrm{R}}R_{\mathrm{on}}}{MC_{\mathrm{R}}+C_{\mathrm{B}}}$.

Therefore, the transfer gain of the typical SMA, which can be considered as the cascade FIR and IIR filtering, is

$$H_{\mathrm{SMA}}(f)=H_{\mathrm{FIR\text{-}S}}(f)H_{\mathrm{IIR\text{-}S}}(f), \quad (31)$$

$$H_{\mathrm{FIR\text{-}S}}(f)=\frac{1-\mathrm{e}^{-\mathrm{j}2\pi fT_k}}{1-\mathrm{e}^{-\mathrm{j}2\pi fT_k/M}}, \quad (32)$$

$$H_{\mathrm{IIR\text{-}S}}(f)=\frac{\gamma(T_k/2)-\nu(T_k/2)}{1-\left(\gamma(T_k/2)+M\nu(T_k/2)\right)\mathrm{e}^{-\mathrm{j}2\pi fT_k}}. \quad (33)$$

3.3 Transfer gain for a typical digital RF charge sampling mixer

The typical digital RF mixer proposed by Muhammad *et al.* (2005) and Staszewski *et al.* (2005) can be divided into three parts (Fig. 6). During a sampling period of C_{B}, every C_{R} needs to be charged, read out and reset in sequence. Therefore, we have $T_k=MNT_{\mathrm{s}}$. Using the discrete-time analysis method, the complete unfolded transfer function for this mixer can be derived from Eqs. (7) and (8) for pseudo-differential structure, Eqs. (22)–(25) for TMA, and Eqs. (31)–(33) for SMA.

Let g_{m}=30 ms and f_{s}=2.4 GHz. Fig. 7 shows the complete unfolded transfer gains in three different cases calculated from the formulae derived above, using the discrete-time approach. In case 1, the capacitors are C_{H}=15.425 pF, C_{R}=0.5 pF, C_{B}=13.925 pF, and the switch-on resistances are negligible. In this case, the half-circuit transfer gain, excluding the pseudo-differential effect, is the same as that presented by Ho *et al.* (2006). In cases 2 and 3, the capacitors and switch-on resistances are C_{H}=15.425 pF, C_{R}=0.5 pF, C_{B}=13.925 pF, R_{on}=1 kΩ, and C_{H}=20 pF, C_{R}=1 pF, C_{B}=17 pF, R_{on}=2 kΩ, respectively. Because of the switch-on resistances, the time constant τ and μ are not equal to zero in these two cases. As Fig. 7 shows, the transfer gains located at the center frequency 2.4 GHz are 42.10 dB and 36.08 dB in case 1 and case 2, respectively. The transfer gains of 3 MHz away from the center frequency 2.4 GHz are

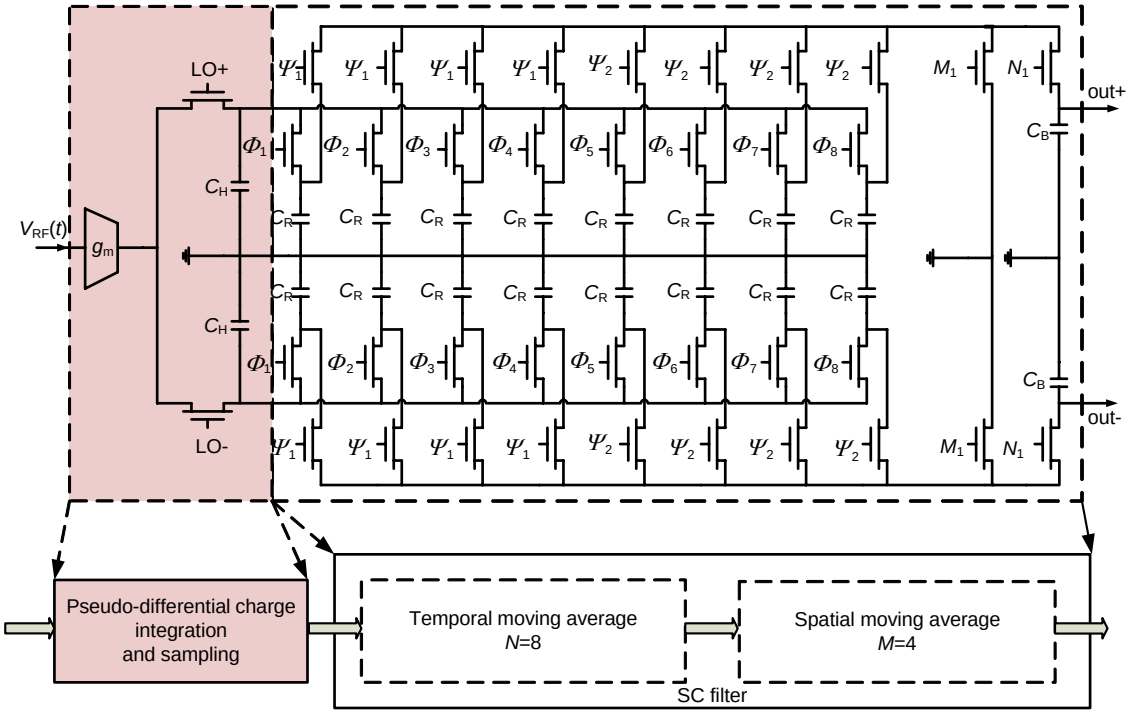

Fig. 6 Signal processing of a typical digital RF mixer

attenuated to 28.26 dB and 22.95 dB in cases 1 and 2, respectively. The calculation results suggest that the larger the time constants are, the more the transfer gains are reduced. Therefore, CMOS switch-on resistances need to be considered when analyzing the transfer gains. Because of the pseudo-differential structure, DC gains are reduced to −20 dB effectively while the transfer gain located at around the carrier frequency remains unchanged.

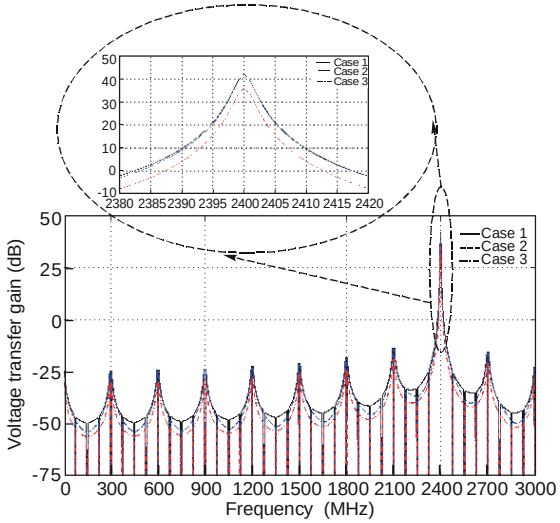

Fig. 7 Unfolded transfer gains of a typical digital RF mixer in three different cases using the discrete-time analysis method

4 Circuit-level simulation and analysis

The charge values in the equations formulated above using the discrete-time analysis method carry enough information to analyze a digital RF circuit. In order to verify the approach further, we implemented a circuit-level simulation for the typical digital RF charge sampling mixer in continuous-time domain. A circuit-level model for the mixer is established in Cadence SpectreRF. A group of multi-phase and multi-frequency clocks for controlling switches are described by Verilog-A language. Because of the switch-on resistances, the time constants τ and μ are increased with the augmentation of the capacitors and switch-on resistances. Fig. 8 shows the voltages on the history capacitor and the rotating capacitor in transient time in cases 2 and 3 when the received carrier frequency is 2.401 GHz. In IIR filtering, the charge reserved on the history capacitor in the last interval will be transferred partially to the connected rotating capacitor in the current interval. The time needed to finish the charge sharing process between the history capacitor and the rotating capacitor is dependent on the time constants. The charge shared from the history capacitor by the rotating capacitor in Fig. 8b is less than that in Fig. 8a because of the larger time constant.

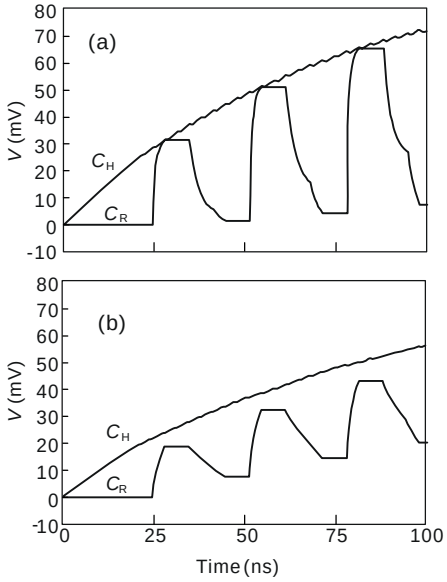

Fig. 8 Transient response of the voltages on the history capacitor and a certain rotating capacitor in case 2 (a) and case 3 (b)

The circuit-level simulation utilizes RF-oriented simulation algorithms in SpectrRF. The unfolded transfer gains can be obtained by combining the PSS (periodic steady-state analysis) and the PXF (periodic transfer function analysis) after solving the hidden state problem (Kundert, 2003; Kundert and Zinke, 2004) of Verilog-A in SpectrRF environment. Fig. 9 shows the unfolded transfer gains from 2025 MHz to 2625 MHz in both case 2 and case 3. The transfer gains in baseband are restrained to below −80 dB because of the pseudo-differential structure. Comparison of Fig. 9 and Fig. 8 shows that the calculation results from the discrete-time analysis approach and the circuit-level simulation results match well in both zeroes and poles. They have the same capabilities at frequency spectrum removal and anti-alias filtering. Therefore, the approach presented above and corresponding formulae can be used to evaluate different structures and transfer functions of

digital RF charge sampling mixers rapidly at a high level. The circuit-level simulation also verifies some results derived from discrete-time analysis. The capacitors and switch-on resistances with smaller values are beneficial for the transfer gain in the design of a charge sampling mixer.

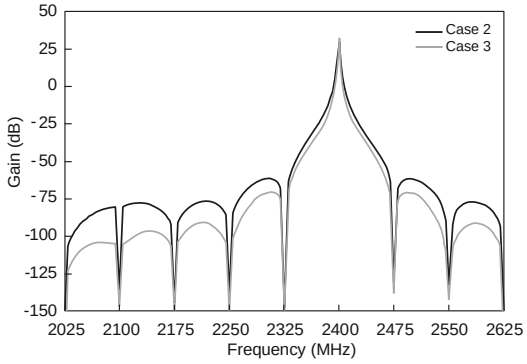

Fig. 9 Unfolded transfer gains of the digital RF charge sampling mixer by simulating at circuit-level in cases 2 and 3, respectively

5 Conclusion and future work

This paper presents an approach based on discrete-time charge values to analyze digital RF charge sampling mixers. Because of the characteristics of digital RF techniques, the approach utilizes the charge values at any sampling instant to calculate and evaluate the general formulae for some key blocks of a general digital RF mixer, including the pseudo-differential structure and the switch-capacitor filter with switch-on resistances. The pseudo-differential structure brings 60 dB attenuation for DC-gain compared with the single-end structure. The unfolded transfer gain and anti-alias filtering of a typical digital RF charge sampling mixer can be easily achieved through the approach promptly. The larger the switch-on resistances are, the more the transfer gains are reduced. The simulation of the circuit-level model constructed in SpectreRF has the same results, and further proves the validity of the approach used in fast simulation and evaluation. The discrete-time analysis now focuses mainly on the behaviors of pseudo-differential and anti-aliasing filtering. In future work, more general parameters could be taken into account for various cases of digital RF mixers and filters. This approach could be further applied in other aspects of digital RF techniques such as clock jitter and skew, noise performance, image-rejecting capability, nonlinearity and so on.

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