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Effect of chip rate on the ranging accuracy in a regenerative pseudo-noise ranging system*

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Abstract: The ranging accuracy of a pseudo-noise ranging system is mainly decided by range jitter and time delay discrimination. Many factors can affect the ranging accuracy, one of which is the chip rate. In digital signal processing, the time delay discrimination and autocorrelation function of sampled ranging sequences of different chip rates are very different. An approximation simulation model is established according to an in-phase quadrature (I/Q) correlator which is used to evaluate the time delay. Simulation results of the range jitter and time delay discrimination show that the chip rate which provides a non-integer sample-to-chip rate ratio can achieve a higher ranging accuracy, and some test results validate the simulation model. In some design missions, the simulation results may help to select an optimum sample-to-chip rate ratio to satisfy the design requirement on the ranging accuracy.

Key words: Ranging accuracy, Range jitter, Time delay discrimination, Sample-to-chip rate ratio, Integration time, Autocorrelation function, Fractional chip period delay

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1 Introduction

There are many factors affecting ranging accuracy in a regenerative pseudo-noise (PN) ranging system. Many documents from the Consultative Committee for Space Data Systems (CCSDS) (CCSDS 414.0-G-1, 2010), European Space Agency (ESA) (Boscagli et al., 2007; Massey *et al.*, 2007; Holsters *et al.*, 2008), and National Aeronautics and Space Administration (NASA) (Berner *et al.*, 1999; Ruggier *et al.*, 2004) mainly discuss the factors that affect the standard deviation of range jitter, such as regenerative process clock, bandwidth of chip tracking loop, signal-to-noise ratio (SNR) of uplink and downlink, and integration time. The regenerative PN ranging system is usually implemented in digital hardware; therefore, the effects of different sample-to-chip rate ratios must be considered. When the other conditions are constant, different chip rates will have different range jitters. It is very difficult to explain the difference in theory and there is not enough discussion on this topic.

The time delay discrimination, which usually limits the ranging accuracy, is another object we must pay attention to. Suppose the standard deviation of measurement ranges is only 1 cm and the time delay discrimination is 1 ns which corresponds to 0.3 m. This means that the PN ranging system can distinguish the range movement only when the relative motion range is larger than 0.15 m. Although the standard deviation of measurement ranges is small, the ranging accuracy is also limited to 0.15 m by the time delay discrimination. Therefore, it is essential to discuss the time delay discrimination of the PN ranging system.

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Until now, there have been many documents discussing non-commensurate sampled systems (Quirk and Srinivasan, 2006; Ding *et al.*, 2009b; Liu *et al.*, 2009b), some of which analyze mainly the performance of multi-rate sampled systems using multi-innovation stochastic gradient algorithms (Ding and Chen, 2007; Ding *et al.*, 2008; 2010; Han and Ding, 2009) or its auxiliary model (Ding *et al.*, 2009a; Liu *et al.*, 2009a; Wang and Ding, 2010). However, there is no algorithm to explain how to select an optimum sample-to-chip rate ratio for a PN ranging system. In this paper, we establish an approximation simulation model to create a qualitative analysis of the effects of different chip rates on the range jitter and time delay discrimination.

2 Time delay discrimination

Time delay discrimination can directly limit the ranging accuracy of a PN ranging system. When the sample-to-chip rate ratio is an integer, the position relationships between the digital samples and the chip's falling edges or rising edges are constant. To distinguish time delay between the received ranging sequence and the local reference sequence, the time delay must be up to one sample period (Fig. 1). The sample-to-chip rate ratio is 4, and the actual time delay is smaller than one sample period. However, the time delay evaluated from these two sampled sequences is one sample period. For any time delay that is smaller than one sample period, the time delay evaluated by these two sampled sequences is always one sample period. It is obvious that the time delay discrimination is limited by the sample rate when the sample-to-chip rate ratio is an integer.

Time delay discrimination can be improved by increasing the sample rate. However, this method also increases the process power consumption and needs much more steady peripheral circuits to ensure the quality of the clock resource, and thus is not optimal. A non-integer sample-to-chip rate ratio can be considered, as depicted in Fig. 2. The sample-to-chip rate ratio is 19/6. The position relationships between the digital samples and the chip's falling edges or rising edges are no longer constant, which repeat after 19 sample points. The potential to distinguish these two sampled sequences is created, which will improve the time delay discrimination.

To discover the realizable time delay discrimination, we must consider the minimum time delay, which will lead to a difference in these two digital sequences. Assume the time delay between the received ranging sequence and the local reference sequence is τ, and the sample positions relative to the chip's falling edges or rising edges repeat after L samples. This implies that the position relationships between the digital samples and the chip's falling edges or rising edges repeat after L samples (Fig. 2). In order to have different sample points in these two sampled sequences, one pair of sample points are sampled from contiguous ranging chips at any rate. This occurs when the accumulated time delay $L\tau$ is greater than one chip period. The smallest time delay is the chip period T_c divided by L. There may be a relationship between the sample period and chip period as follows:

$$mT_s=nT_c, \tag{1}$$

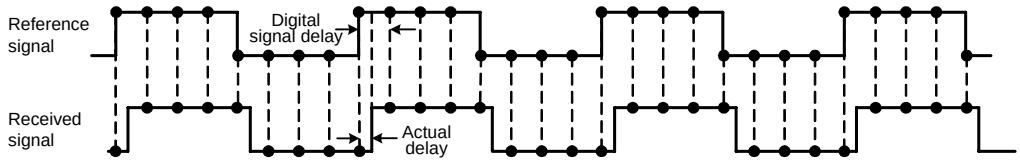

Fig. 1 Uniform sampling at a sample-to-chip rate ratio of 4

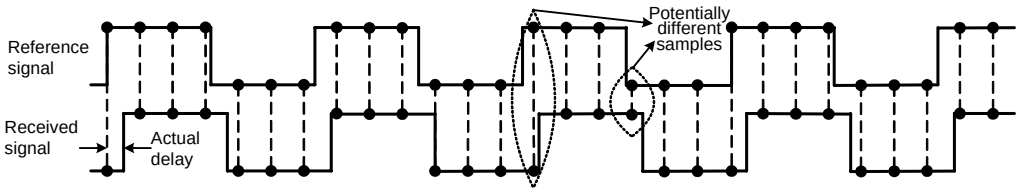

Fig. 2 Non-uniform sampling at a sample-to-chip rate ratio of 19/6

where m and n are both integers and T_s is the sample period. When m is the smallest integer that satisfies Eq. (1), the time delay discrimination is T_c/m. If m is an irrational number, the sampled sequence will never repeat. It will provide infinite time discrimination in theory (Quirk and Srinivasan, 2006).

3 Autocorrelation function

The PN ranging sequence possesses very strong correlation properties that can be found from the correlation results with shifted or un-shifted probing sequences (Massey *et al*., 2007). When a high ranging accuracy is required, the evaluation of fractional chip period must be more accurate. A non-integer sample-to-chip rate ratio leads to a new sampled sequence that does not have the same autocorrelation properties with respect to the original ranging sequence. Therefore, it is necessary to calculate the autocorrelation function with different fractional chip period delays.

Consider a PN ranging sequence $c(t)$ as

$$c(t)=c_n p(t-nT_c-\tau), \tag{2}$$

where $p(t)$ is a square waveform signal with period T_c, c_n is the value (+1 or −1) of the nth chip code, and τ is the fractional chip period delay. For time delays τ_1 and τ_2, the autocorrelation function is given as

$$r(\tau_1,\tau_2)=\frac{1}{T_{\text{corr}}}\sum_{\tau_2-\tau_1=-T_c}^{T_c}\left(c_n p(t-nT_c-\tau_1)\cdot c_m p(t-mT_c-\tau_2)\right), \tag{3}$$

where T_{corr} is the correlation integration time, and values of $m-n$ are −1, 0, and 1. If we use the total sampled sequence to calculate its autocorrelation properties, the result must be close to that of the original ranging sequence. Nevertheless, the period of the sampled sequence is too large, and partial correlation is mostly used. Under these situations, much more care should be taken to choose the sample-to-chip rate ratio and the correlation integration time to ensure that the result of partial correlation closely approximates that of the original PN sequence. For example, consider an actual design condition: sample rate is 19.2 MHz, integration time is 0.85333 ms which corresponds to 16384 sample points, and PN sequence is JPL1999. The chip rates are 0.96 and 1.2 MHz (which correspond to integer sample-to-chip rate ratios), and 1.0 and 1.1 MHz (which correspond to non-integer sample-to-chip rate ratios). Their autocorrelation functions are as shown in Fig. 3.

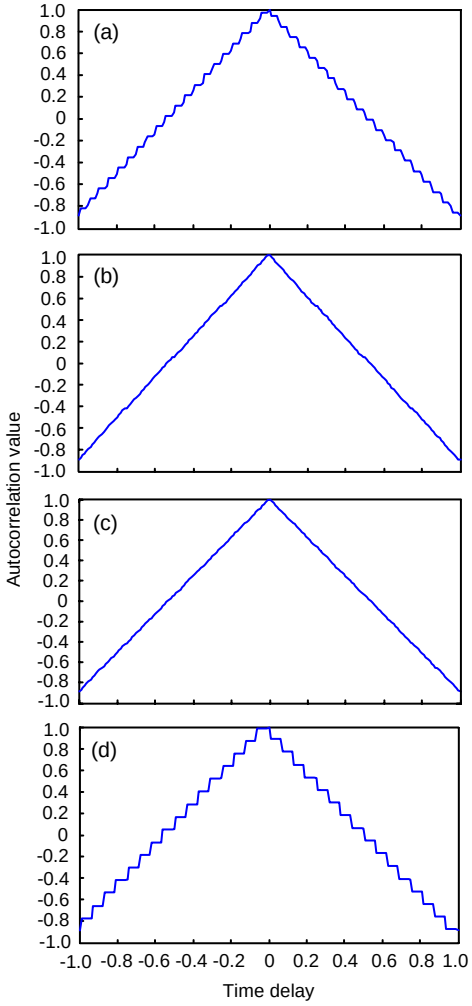

Fig. 3 Autocorrelation functions of different sample-to-chip rate ratios

Chip rates of (a)–(d) are 0.96, 1.0, 1.1, and 1.2 MHz, respectively; sample-to-chip rate ratios of (a)–(d) are 20, 96/5, 192/11, and 16, respectively

The x-axis time delay $\tau_2-\tau_1$ in Fig. 3 is accumulated from $-T_c$ to $+T_c$ with a step length of $T_c/100$, and the y-axis autocorrelation values correspond to $r(\tau_1, \tau_2)$ in Eq. (3). The autocorrelation function with an integer sample-to-chip rate ratio is not very good as shown in Fig. 3a or Fig. 3d. The correlation values

may be the same for some different time delays, which mean these time delays are not discernible. However, the autocorrelation function with a non-integer sample-to-chip rate ratio has a superior performance. Especially for 1.1 MHz one time delay uniquely corresponds to one correlation value. As the sampled sequence's correlation properties can influence the ranging accuracy, we should pay much more attention in selecting an optimum sample-to-chip rate ratio to ensure better autocorrelation properties of the sampled sequence.

4 Simulation of the in-phase quadrature (I/Q) correlator

At the ground station the time delay can be obtained from the phase difference between received and local reference ranging sequences. The two-way roundtrip time delay can be evaluated as follows (Boscagli *et al.*, 2007; Holsters *et al.*, 2008):

$$T_{\text{delay}} = \sum_{i=1}^{6} \alpha_i d_i T_{\text{c}} + \tau, \tag{4}$$

where α_i is evaluated using the Chinese remainder theorem (Hamkins, 1999; Wang, 2004) as α_1=504 735, α_2=721 050, α_3=642 390, α_4=134 596, α_5=850 080, and α_6=175 560 for JPL1999, and d_i is the estimated phase for probing sequence C_i, which is evaluated in chip period. Therefore, the first term of Eq. (4) is the coarse time delay. The more accurate time delay is decided by τ, which represents the fractional chip period delay as $0<\tau<T_{\text{c}}$. As the strong correlation properties of a PN sequence, τ is evaluated by an I/Q correlator (Boscagli *et al.*, 2007; Holsters *et al.*, 2008) as shown in Fig. 4.

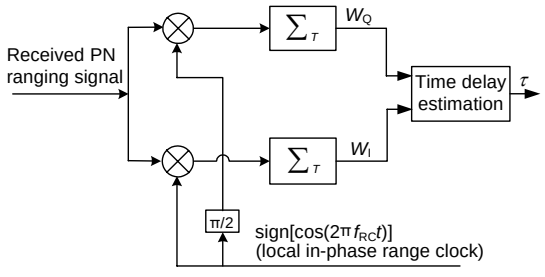

Fig. 4 I/Q correlator for time delay evaluation

Generally, the front-end of a receiver has a narrowband filter. Then the received PN ranging signal at the I/Q correlator input can be approximately given by (Kinman and Berner, 2003)

$$r(t) = \sqrt{2}\sin(2\pi f_{\text{RC}} t), \tag{5}$$

where f_{RC} is frequency of the range clock. Local reference signal is a square waveform signal with period $T_{\text{RC}}=1/f_{\text{RC}}$. The integration time is T, which is K multiple of T_{RC}. The fractional chip period time delay is τ. Without considering the effects of other noises, the correlation gives

$$\begin{cases} W_{\text{I}} = \dfrac{1}{T}\left(\displaystyle\sum_{i=0}^{K-1}\int_{iT_{\text{RC}}}^{(i+\frac{1}{2})T_{\text{RC}}} r(t-\tau)\mathrm{d}t - \sum_{i=0}^{K-1}\int_{(i+\frac{1}{2})T_{\text{RC}}}^{(i+1)T_{\text{RC}}} r(t-\tau)\mathrm{d}t\right), \\ W_{\text{Q}} = \dfrac{1}{T}\left(\displaystyle\sum_{i=0}^{K-1}\int_{(i+\frac{1}{4})T_{\text{RC}}}^{(i+\frac{3}{4})T_{\text{RC}}} r(t-\tau)\mathrm{d}t - \sum_{i=0}^{K-1}\int_{(i+\frac{3}{4})T_{\text{RC}}}^{(i+\frac{5}{4})T_{\text{RC}}} r(t-\tau)\mathrm{d}t\right). \end{cases} \tag{6}$$

It gives

$$\begin{cases} W_{\text{I}} = \dfrac{2\sqrt{2}}{\pi}\cos(2\pi f_{\text{RC}}\tau), \\ W_{\text{Q}} = \dfrac{2\sqrt{2}}{\pi}\sin(2\pi f_{\text{RC}}\tau). \end{cases} \tag{7}$$

The derivation of Eq. (7) is given in the Appendix. The time delay τ can be evaluated by W_{I} and W_{Q} as

$$\tau = \frac{1}{2\pi f_{\text{RC}}}\arctan\left(\frac{W_{\text{Q}}}{W_{\text{I}}}\right). \tag{8}$$

Using the I/Q correlator to evaluate the time delay is based on the correlation properties of a PN ranging sequence. However, different sample-to-chip rate ratios have different correlation properties, as shown in Fig. 3. The effects of different chip rates on the range jitter can be simulated according to the structure of Fig. 4 without considering other noises. The simulation flow chart is shown in Fig. 5.

In order to validate the rationality of the simulation model, some results from simulation and experiments are compared. As mentioned in Kinman and Berner (2003), Ruggier *et al.* (2004), Boscagli *et al.* (2007), and CCSDS 414.0-G-1 (2010), the integration time T can affect the range jitter. In the

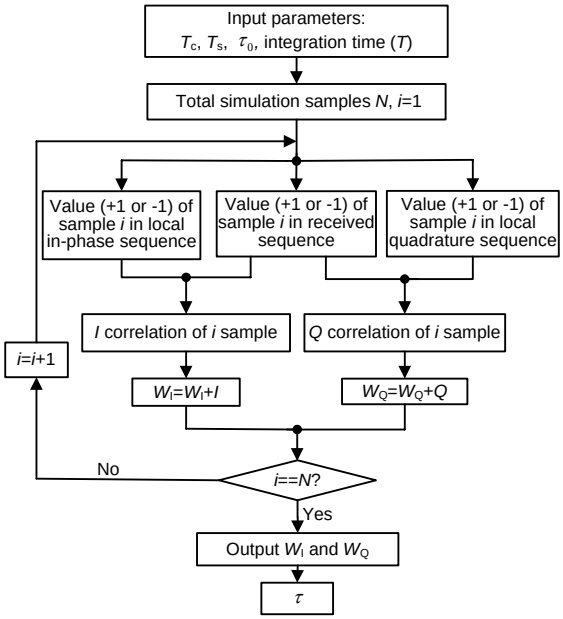

Fig. 5 Flow chart of I/Q correlator simulation model

simulation model, the input parameters are: chip rate is 1.1 MHz, sample rate is 19.2 MHz, and τ_0 is T_c/100. For a certain integration time T, we obtain 5000 simulation time delay τ values. Then these time delay values are converted to range values. Finally, the standard deviations of these 5000 range values are obtained. In actual experiments we use the regenerative PN ranging system test-board developed by our own research group to test the range jitter. The parameters are the same as the simulation parameters: chip rate is 1.1 MHz and sample rate is 19.2 MHz. The transmitted power of uplink and downlink is constant and sufficiently high. The SNR of received ranging signal is changed by changing the integration time. For a certain integration time, we obtain 15000 range values. Finally, the standard deviations of these 15000 range values are obtained and compared to the simulation results with the same integration time. The integration times of simulation and experiment are 0.01333, 0.10667, 0.85333, 13.65333, and 109.2267 ms. The standard deviations of range jitter from simulation and test are shown in Fig. 6.

In the process of testing, there are many other factors that affect the results, especially the phase noise of the oscillator. The frequency accuracy of the oscillator used is only $\pm 20\times10^{-6}$. The trend curve of the simulation results is coincident with that of the test results. This means that the simulation model is rational to some extent.

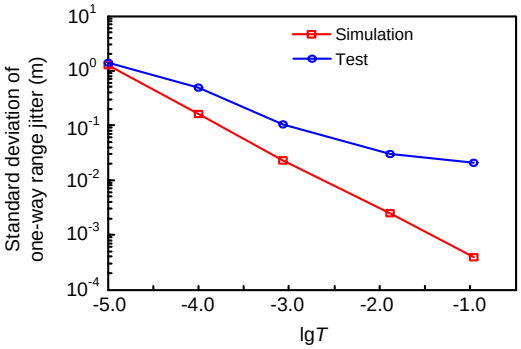

Fig. 6 Standard deviations of range jitter in different integration times for a chip rate of 1.1 MHz

Then we can use this simulation model to obtain a qualitative analysis on the effects of different chip rates to the range jitter. The parameters used in the simulation are as follows: sample rate is 19.2 MHz, integration time is 13.65333 ms, and the number of simulation τ values is 5000. The simulation chip rates are 0.9, 0.96, 1.0, 1.1, and 1.2 MHz. For a certain chip rate, the standard deviations of 5000 simulation range values are obtained. We also use the same parameters to do some actual experiments with our own test-board: sample rate is 19.2 MHz, integration time is 13.65333 ms, and the number of tested range values is 5000. The transmitted power of uplink and downlink is constant and sufficiently high. The tested chip rates are also 0.9, 0.96, 1.0, 1.1, and 1.2 MHz. For a certain chip rate, the tested result is compared to the simulation result. The standard deviations of range jitter simulated and tested are shown in Fig. 7.

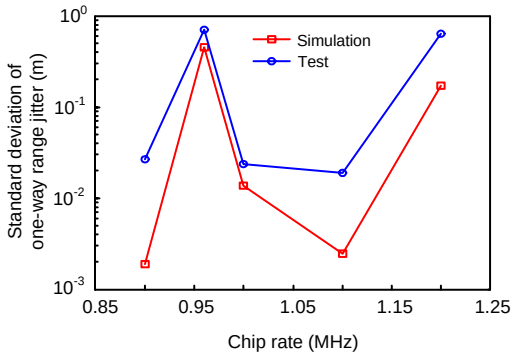

Fig. 7 Standard deviations of one-way range jitter for different chip rates

The standard deviation of measurement ranges with non-integer sample-to-chip rate ratios is better than that with integer sample-to-chip rate ratios from

Fig. 7. Also, the curves of simulation and test results have the same change trend. By comparing Figs. 3 with 7, the conclusion can be drawn that the standard deviation of measurement ranges is better when the chip rate has better autocorrelation properties. In some design missions, the simulation can be done first to analyze the range jitter of different chip rates.

5 Simulation of time delay discrimination

In the final ranging accuracy, time delay discrimination is another object that must be considered apart from the range jitter. The 1.1 MHz has the best correlation properties as seen from Fig. 3. However, the step length of accumulated time delay is $T_c/100$, which is approximately 9.1 ns for 1.1 MHz, and the corresponding one-way range is approximately 1.36 m. This means that the PN ranging system can distinguish this change when the relative motion range between two objects is larger than 1.36 m. What is the reflection of the PN ranging system when the relative motion range is smaller than 1.36 m? The autocorrelation properties of 1.1 MHz need to be known in a shorter accumulated step length. Consider the step length is $T_c/300$, and other parameters are the same as in Fig. 3c. The autocorrelation function is shown in Fig. 8. For observation, the *x*-axis of amplificatory parts is in step number (Fig. 8b).

Step length $T_c/300$ is approximately 3.03 ns for 1.1 MHz, which corresponds to one-way range 0.45 m. The autocorrelation function shows that sometimes two different time delays have the same correlation value. Thus, when the movement range between two objects is smaller than 0.45 m, the PN ranging system may not distinguish the range movement.

For validating the effects of correlation properties to the time delay discrimination, we use the simulation model to evaluate the time delay τ in step lengths $T_c/100$ and $T_c/300$. The sample rate is 19.2 MHz, integration time is 0.853 33 ms, the number of range values is 1000 and the numbers of accumulated time delay steps are 1–12. Simulation results are shown in Fig. 9. The *x*-axis is the step number, and the *y*-axis is the time delay of theory and simulation. The theory is the input parameter τ_0 in the simulation model, and the simulation is the output τ of

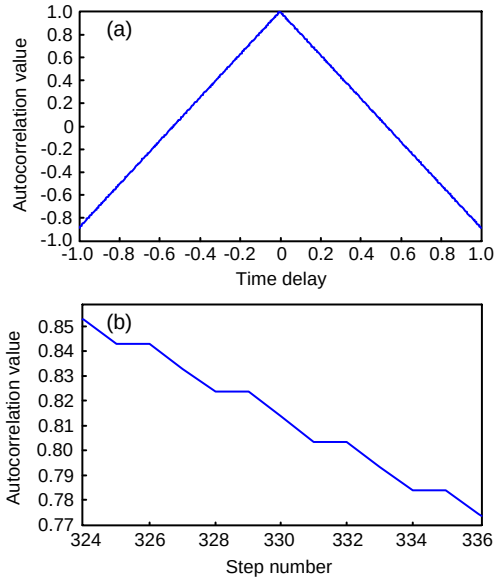

Fig. 8 Autocorrelation function for a chip rate of 1.1 MHz with a step length of $T_c/300$
(b) is an amplificatory part of (a)

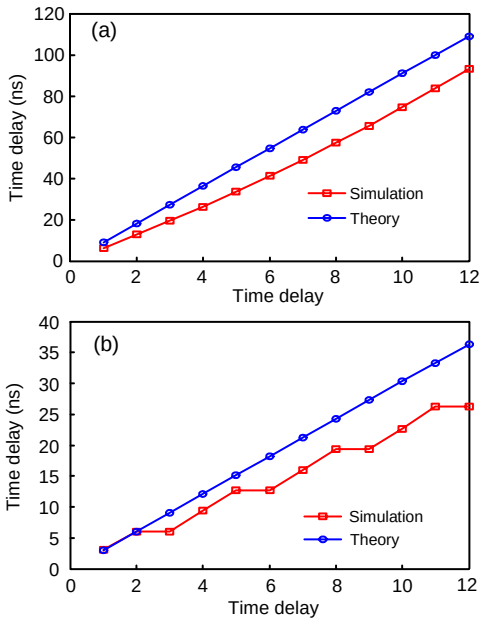

Fig. 9 Time delay simulation for a chip rate of 1.1 MHz with step lengths of $T_c/100$ (a) and $T_c/300$ (b)

the simulation model. By comparing these two values, we can know whether the output time delay changes with the input time delay. And the ability to distinguish different chip rates can also be decided.

The simulation results show that time delay τ changes with step length $T_c/100$, but contrarily time delay τ sometimes does not change with step length

T_c/300. This means that the PN ranging system with these same parameters has the ability to distinguish the step length T_c/100 but cannot distinguish the step length T_c/300. If the PN ranging system is required to distinguish the step length T_c/300, a convenient method is to change the chip rate. As discussed in Section 2, the theoretical time delay discrimination can be obtained according to Eq. (1), and it is T_c/192 for sample rate 19.2 MHz and chip rate 1.1 MHz. When chip rate 1.11 MHz is selected, theoretical time delay discrimination is T_c/640, which can distinguish the step length T_c/300. The simulation results for 1.11 MHz with step length T_c/300 are shown in Fig. 10.

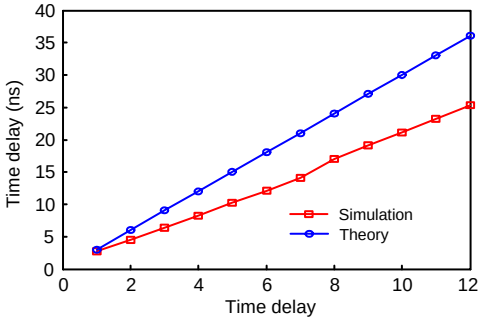

Fig. 10 Time delay simulation for chip rate of 1.11 MHz with a step length of T_c/300

The simulation results show that a 1.11 MHz chip rate can distinguish the step length T_c/300. For a given chip rate, if every fractional chip period time delay uniquely corresponds to a certain correlation value, then the PN ranging system with this sample-to-chip rate ratio can distinguish the accumulated step length.

6 Conclusions

The final ranging accuracy of a PN ranging system is decided mainly by range jitter and time delay discrimination. Based on the above simulation and test results, we can conclude that a non-integer sample-to-chip rate can achieve a better range jitter and time delay discrimination. For different chip rates, the simulation model can make qualitative analysis on range jitter and time delay discrimination. In some design missions, the simulation results can help to select a better sample-to-chip rate ratio to achieve a higher ranging accuracy.

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Appendix

This appendix gives a detailed derivation of Eq. (7). Take W_{I} for granted. It gives

$$
\begin{aligned}
W_{\mathrm{I}} &= \frac{\sqrt{2}}{T}\left(\sum_{i=0}^{K-1}\int_{iT_{\mathrm{RC}}}^{(i+\frac{1}{2})T_{\mathrm{RC}}}\sin\left(2\pi f_{\mathrm{RC}}(t-\tau)\right)\mathrm{d}t-\sum_{i=0}^{K-1}\int_{(i+\frac{1}{2})T_{\mathrm{RC}}}^{(i+1)T_{\mathrm{RC}}}\sin\left(2\pi f_{\mathrm{RC}}(t-\tau)\right)\mathrm{d}t\right)\\
&= \frac{\sqrt{2}}{T}\sum_{i=0}^{K-1}\left(-\frac{\cos\left(2\pi f_{\mathrm{RC}}(t-\tau)\right)}{2\pi f_{\mathrm{RC}}}\right)\Bigg|_{iT_{\mathrm{RC}}}^{(i+1/2)T_{\mathrm{RC}}}-\frac{\sqrt{2}}{T}\sum_{i=0}^{K-1}\left(-\frac{\cos\left(2\pi f_{\mathrm{RC}}(t-\tau)\right)}{2\pi f_{\mathrm{RC}}}\right)\Bigg|_{(i+1/2)T_{\mathrm{RC}}}^{(i+1)T_{\mathrm{RC}}}\\
&= \frac{\sqrt{2}}{T}\sum_{i=0}^{K-1}\left(-\frac{\cos\left(2\pi f_{\mathrm{RC}}\left((i+1/2)T_{\mathrm{RC}}-\tau\right)\right)-\cos\left(2\pi f_{\mathrm{RC}}(iT_{\mathrm{RC}}-\tau)\right)}{2\pi f_{\mathrm{RC}}}\right)\\
&\quad-\frac{\sqrt{2}}{T}\sum_{i=0}^{K-1}\left(-\frac{\cos\left(2\pi f_{\mathrm{RC}}\left((i+1)T_{\mathrm{RC}}-\tau\right)\right)-\cos\left(2\pi f_{\mathrm{RC}}\left((i+1/2)T_{\mathrm{RC}}-\tau\right)\right)}{2\pi f_{\mathrm{RC}}}\right)\\
&= \frac{\sqrt{2}}{T}\sum_{i=0}^{K-1}\left(-\frac{\cos(\pi-2\pi f_{\mathrm{RC}}\tau)-\cos(2\pi f_{\mathrm{RC}}\tau)}{2\pi f_{\mathrm{RC}}}\right)+\frac{\sqrt{2}}{T}\sum_{i=0}^{K-1}\left(\frac{\cos(2\pi f_{\mathrm{RC}}\tau)-\cos(\pi-2\pi f_{\mathrm{RC}}\tau)}{2\pi f_{\mathrm{RC}}}\right)\\
&= \frac{2\sqrt{2}}{T}\sum_{i=0}^{K-1}\frac{2\cos(2\pi f_{\mathrm{RC}}\tau)}{2\pi f_{\mathrm{RC}}}=\frac{2\sqrt{2}}{KT_{\mathrm{RC}}}\cdot K\cdot\frac{2\cos(2\pi f_{\mathrm{RC}}\tau)}{2\pi f_{\mathrm{RC}}}\\
&= \frac{2\sqrt{2}}{\pi}\cos(2\pi f_{\mathrm{RC}}\tau).
\end{aligned}
$$

And W_{Q} can be given as $W_{\mathrm{Q}}=\dfrac{2\sqrt{2}}{\pi}\sin(2\pi f_{\mathrm{RC}}\tau)$. Then Eq. (7) is obtained.