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Design of ternary D flip-flop with pre-set and pre-reset functions based on resonant tunneling diode literal circuit

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Abstract: The problems existing in the binary logic system and the advantages of multiple-valued logic (MVL) are introduced. A literal circuit with three-track-output structure is created based on resonant tunneling diodes (RTDs) and it has the most basic memory function. A ternary RTD D flip-flop with pre-set and pre-reset functions is also designed, the key module of which is the RTD literal circuit. Two types of output structure of the ternary RTD D flip-flop are optional: one is three-track and the other is single-track; these two structures can be transformed conveniently by merely adding tri-valued RTD NAND, NOR, and inverter units after the three-track output. The design is verified by simulation. Ternary flip-flop consists of an RTD literal circuit and it not only is easy to understand and implement but also provides a solution for the algebraic interface between the multiple-valued logic and the binary logic. The method can also be used for design of other types of multiple-valued RTD flip-flop circuits.

Key words: Resonant tunneling diode (RTD), Ternary logic, Literal circuit, D flip-flop
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1 Introduction

Binary logic is developed and exploited based on Boolean algebra. Binary integrated circuit technology has rapidly advanced in the last few decades (Hurst, 1984; Kameyama, 1990). It is very easy to produce and recognize binary signals in the Boolean algebra system with binary integrated circuits, and the basic binary units are very simple. The devices used in binary digital circuits operate in switching mode. All these advantages make the binary circuits easy to design. Until now, the binary logic circuit has been widely and deeply developed with the continuously developing capability of microelectronics. However, the advance of processing speeds and the improvement of the performance/cost ratio based on conventional binary logic circuits will not continue indefinitely into future very-large-scale integration (VLSI) (Hurst, 1984; Kameyama, 1990; Hanyu *et al*., 1993). The most urgent are interconnection problems both on-chip and among-chips. While the device scaling satisfies the requirement for higher integration density, the number of interconnections greatly increases as more and more functions are integrated onto one chip, and also the silicon area used for interconnections is greater than that used for active logic elements. The increasing number of interconnections also brings new packaging problems.

Using multiple-valued logic (MVL) is one of the most promising solutions for overcoming the above problems. MVL can reduce the number and complexity of interconnections and greatly increase density as well as processing speed. As multiple-valued signals can carry more information, MVL has more obvious advantages in the processes of transmission and storage. For example, the amount of information expressed by a two-bit decimal signal is 24 times greater than that expressed by a two-bit binary signal. Moreover, the delay time and crosstalk noise are also reduced by using MVL. When dealing with the same

amount of information, the number of signals used in multiple-valued circuits is far less than that in binary circuits. Therefore, although the logic design techniques for MVL are more complex than familiar binary logic (Hurst, 1988), the subject of MVL is very necessary for research and has been receiving more and more attention (Quan *et al*., 2000; Chen and Shen, 2001; Yao, 2010).

The work on emitter couple logic (ECL), integrated injection logic (I^2L), n-channel mental oxide semiconductor (nMOS) technology, charge-coupled device (CCD) technology, complementary metal oxide semiconductor (CMOS), etc. has achieved great results in MVL (Etiemble and Israel, 1988). In extremely scaled down devices, the quantum effect becomes a fundamental limit for normal operations. However, this effect offers exciting and interesting uses for quantum devices, especially the resonant tunneling diode (RTD) (Kameyama, 1990). RTD has a unique negative differential resistance (NDR) characteristic, which allows for diverse multiple-valued application areas (Mazumder *et al*., 1998; Berezowski and Vrudhula, 2005; 2007; Nunez *et al*., 2008). Thus, in this paper, the tri-valued logic system with RTD is studied. First, the literal operation and its properties are described. The literal operation is a very important operation which is composed of a complete set with a tri-valued AND operation and OR operation in the tri-valued algebra system. Second, the characteristic of RTD is introduced. RTD is one of the most popular quantum devices in recent research, and its unique negative differential resistance characteristic leads to broad applications. Third, a literal circuit based on RTD is created. The circuit has a three-track-output structure with binary values in each track, and also a basic memory function. Fourth, a ternary RTD D flip-flop is designed with pre-set and pre-reset functions. The key part is the RTD literal circuit, and the internal structures of the ternary RTD D flip-flop are all binary units; that is, the RTD circuits can use binary logic to realize ternary logic. Finally, simulations are made to verify the correctness of the design.

2 Literal operation and its properties

The definition of the literal operation in the ternary algebra system is as follows (Wu, 1994; Drechsler, 1996; Zhang and Wu, 2008; Zeng and Wang, 2009):

$$ {}^{i}x^{i} = \begin{cases} 2, & x = i, \\ 0, & x \neq i, \end{cases} \quad i \in \{0, 1, 2\}. \tag{1} $$

In the ternary algebra system, the literal operation with AND and OR operations constitutes a complete set. Its main properties are as the following.

Mutually exclusive property:

$$ {}^{i}x^{i} \cdot {}^{j}x^{j} = 0, \quad i \neq j. \tag{2} $$

Complementary property:

$$ {}^{0}x^{0} + {}^{1}x^{1} + {}^{2}x^{2} = 2. \tag{3} $$

Reducibility property:

$$ \begin{cases} x = {}^{2}x^{2} + 1 \cdot {}^{1}x^{1}, \\ x = \overline{{}^{0}x^{0}}(1 + \overline{{}^{1}x^{1}}). \end{cases} \tag{4} $$

Eqs. (2) and (3) indicate that, in ternary logic, there are constrained relationships of exclusivity and complementary among the three literal operations, and one literal operation can always be acquired from the other two (Wu, 1994):

$$ {}^{i}x^{i} = \overline{{}^{j}x^{j} + {}^{k}x^{k}} = \overline{{}^{j}x^{j}} \cdot \overline{{}^{k}x^{k}}, \quad i \neq j \neq k. \tag{5} $$

In the next sections, we will design an RTD literal circuit according to the above properties of the literal operation, and the ternary RTD D flip-flop can also be created.

3 RTD and RTD literal circuit

With the development of integrated circuit manufacturing techniques, the feature size of devices has been decreased to nanometer scale. Quantum devices reveal new applications of the nano-semiconductor materials because of the resonant tunneling effects. RTD is one of the most popular quantum devices in recent research with the characteristics of ultra-high speed, ultra-high frequency, ultra-high integration density, high efficiency, and low power loss. Its NDR feature reveals a very important application prospect in VLSI field in the

future (Ding and Mazumder, 2003; Choi *et al*., 2004; Li *et al*., 2005; Maezawa, 2005; Avedillo *et al*., 2006). RTD can also be combined with GaAs or InP based field effect transistor (FET), heterojunction bipolar transistor (HBT), modulation-doped field effect transistor (MODFET), etc. to acquire three-terminal resonant tunneling (RT) devices, which can combine diverse high-speed integrated circuits with outstanding performance (Li, 2009). RTD+HEMT will be used in this study. The symbols and characteristic curves of RTD and RTD+HEMT are shown in Fig. 1. I_p is the peak current of RTD and I_v is the valley current; the corresponding voltages of I_p and I_v are V_p and V_v, respectively. RTD+HEMT also has a negative resistance characteristic similar to RTD, and its peak current is controlled by the input signal V_G. Compared with a single RTD, the three-terminal device RTD+HEMT makes the circuit design more flexible, and has better fan-out and drive capability, greater gain, higher noise margins, etc. In this study, the simulation of RTD is implemented by using the MOS-NDR RTD emulator (Bhattacharya *et al*., 2000; González *et al*., 2001), the V_p of RTD is about 0.372 V, V_v is about 0.561 V, and the peak/valley ratio of the current is about 10:1. The V_t of HEMT is 0.3 V.

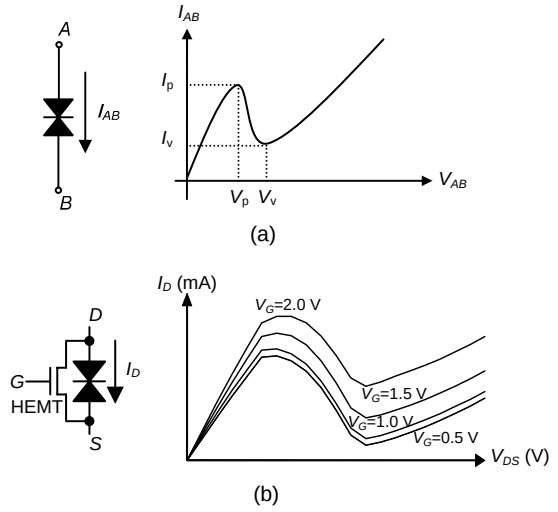

Fig. 1 Symbols and *I-V* characteristics of the resonant tunneling diode (RTD) (a) and RTD+HEMT (b)

The basic structure of the literal circuit with three-track-output based on RTD and RTD+HEMT (Fig. 2) is composed of three similar units built up in a loop. The unit is a binary RTD NOR circuit which consists of an RTD and two parallel RTD+HEMT in series. V_{CK} is a pulse signal, and the binary RTD NOR circuit is a rising-edge-triggered unit of V_{CK}; when V_{CK} is fixed in high voltage, the output remains unchanged. The output is low in the falling-edge of V_{CK} or when V_{CK} is low (Lin *et al*., 2004). Each output track of the RTD literal circuit is

$$\begin{cases} \overline{{}^0Q^0 + {}^1Q^1} = {}^2Q^2, \\ \overline{{}^0Q^0 + {}^2Q^2} = {}^1Q^1, \\ \overline{{}^1Q^1 + {}^2Q^2} = {}^0Q^0. \end{cases} \tag{6}$$

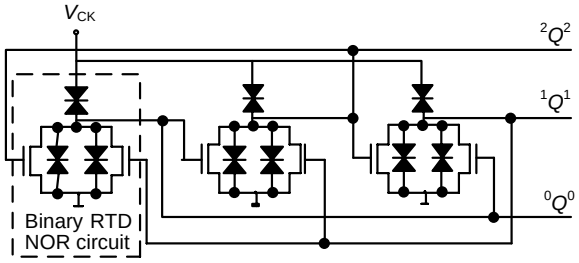

Fig. 2 Basic resonant tunneling diode (RTD) literal circuit with three-track-output

According to the definition of the literal operation, each output track of the literal circuit is a (0, 2) binary signal. From the structure shown in Fig. 2 and Eq. (6), it can be found that each track of output is related to the other two output tracks at the rising edge of V_{CK}, which indicates that the RTD literal circuit has basic memory capability and triggering characteristics. However, this structure has only output without input; to add external signals, it is possible to insert NAND circuits in the RTD NOR loop (Wu, 1994), as shown in Fig. 3a. The NAND circuits and the monostable-bistable transition logic elements (MOBILE) acting as inverters are both composed of RTDs (Chen *et al*., 1995; Lin *et al*., 2004; Quintana *et al*., 2006) and are all binary logic circuits. Therefore, the three-track-output RTD literal circuit has three input signals L_{2D}, L_{1D}, and L_{0D} (Fig. 3b). The relationships between the three-track-output and the three inputs are

$$^2Q^2 = \overline{({}^1Q^1 + {}^0Q^0) \cdot L_{2D}}, \tag{7}$$

$$^1Q^1 = \overline{({}^2Q^2 + {}^0Q^0) \cdot L_{1D}}, \tag{8}$$

$$^0Q^0 = \overline{({}^1Q^1 + {}^2Q^2) \cdot L_{0D}}. \tag{9}$$

Compared with Eq. (6), each output track is related not only with the other two output tracks, but also with current input L_{iD}. The NAND units can be

controlled by setting different values of L_{2D}, L_{1D}, and L_{0D}. The value of L_{iD} is a (0, 2) binary signal.

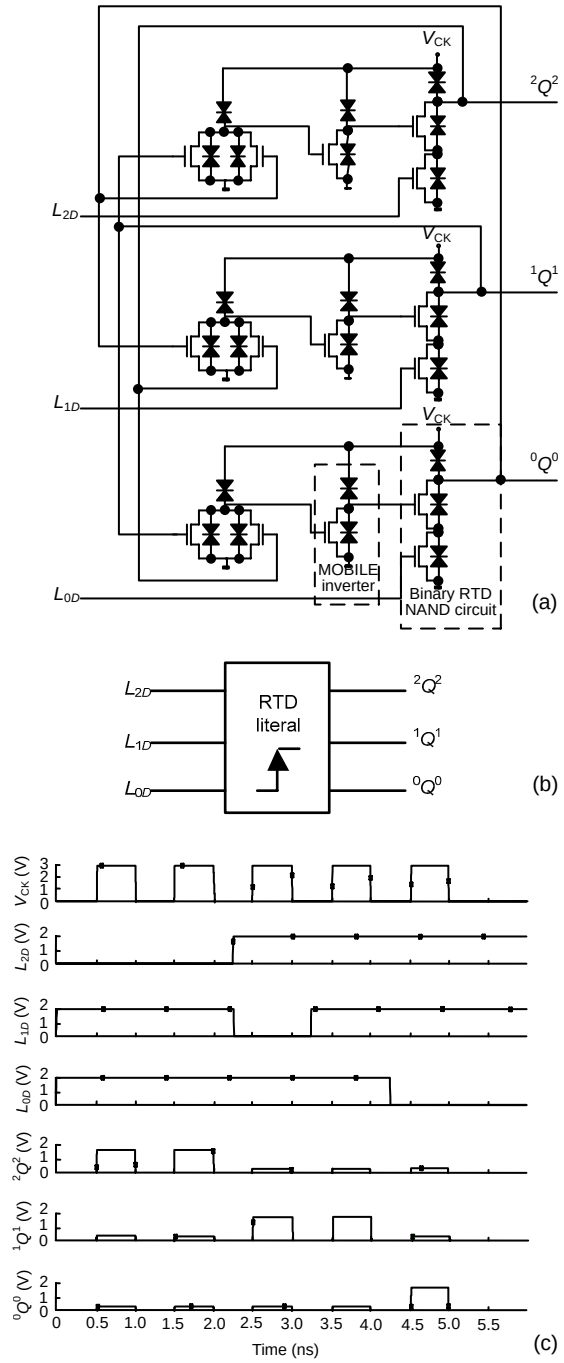

Fig. 3 Resonant tunneling diode (RTD) literal circuit with three-track-output and three inputs (a) and its simplified model (b) and simulation curves (c)

The different effects on the output by a different setting of input L_{iD} are described in Table 1. When two or three input L_{iD} are logic '0', Eqs. (2)–(5) will be invalid. Therefore, at most one input signal can be logic '0' or at least two input signals should be logic '2'.

Table 1 Logic functions of resonant tunneling diode (RTD) literal circuit

L_{2D}	L_{1D}	L_{0D}	$^2Q^2$	$^1Q'^1$	$^0Q^0$	Q'
0	0	0	×	×	×	×
0	0	2	×	×	×	×
0	2	0	×	×	×	×
0	2	2	2	0	0	2
2	0	0	×	×	×	×
2	0	2	0	2	0	1
2	2	0	0	0	2	0
2	2	2	$^2Q^2$	$^1Q^1$	$^0Q^0$	Q

×: forbidden state

When $L_{2D}L_{1D}L_{0D}$=222, there is no effect on the three NAND units, and the output remains unchanged. When $L_{2D}L_{1D}L_{0D}$=220, according to Eq. (9), the next state of $^0Q^0$ is logic '2' (that is to say, $^0Q'^0$=2); combined with Eq. (2), it can be concluded that $^2Q'^2$=0 and $^1Q'^1$=0. Thus, based on the definition of the literal operation and Eq. (4), the output Q'=0. Similarly, when $L_{2D}L_{1D}L_{0D}$=202, we have $^1Q'^1$=2, $^0Q'^0$=0, $^2Q'^2$=0, and Q'=1; when $L_{2D}L_{1D}L_{0D}$=022, we have $^2Q'^2$=2, $^1Q'^1$=0, $^0Q'^0$=0, and Q'=2. Above all, although each output track signal $^iQ^i$ of the RTD literal is a (0, 2) binary signal, combined with Eq. (4), the ultimate value of Q is a tri-valued signal. The simulation curves of the RTD literal circuit are shown in Fig. 3c. V_{CK} is a 3 V pulse signal, τ of the MOS-NDR RTD net is about 21.8 ps, the rising time (TR) of V_{CK} is thus about 3τ–5τ, the high voltage of L_{iD} is 2 V, high voltage of $^iQ'^i$ is about 1.94 V, low voltage is about 0.35 V, and the frequency is about 1 GHz.

The Karnaugh maps of the logic relationships are shown in Fig. 4, and the corresponding equations of the next state are as follows:

$$\begin{cases} Q' = \overline{L_{2D}} + 1 \cdot \overline{L_{1D}} + L_{1D} \cdot L_{0D} \cdot Q, \\ {}^2Q'^2 = \overline{L_{2D}} + L_{1D} \cdot L_{0D} \cdot {}^2Q^2, \\ {}^1Q'^1 = \overline{L_{1D}} + L_{2D} \cdot L_{0D} \cdot {}^1Q^1, \\ {}^0Q'^0 = \overline{L_{0D}} + L_{2D} \cdot L_{1D} \cdot {}^0Q^0. \end{cases} \tag{10}$$

According to Eq. (10), it can be concluded that the output of the RTD literal circuit is related not only to the current input, but also to the past output, so that

the structure shown in Fig. 3a actually has the memory function. As long as the input signals represent a different signal combination, different functions will be achieved.

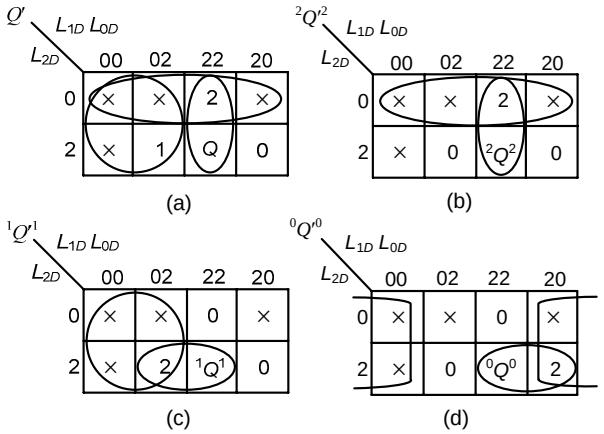

Fig. 4 Karnaugh maps of three-track-output resonant tunneling diode (RTD) literal circuit
(a) Q'; (b) ${}^2Q'^2$; (c) ${}^1Q'^1$; (d) ${}^0Q'^0$

4 Design of ternary D flip-flop based on RTD literal circuit

4.1 Ternary RTD D flip-flop with three-track-output

In Eq. (10), let the three input signals L_{2D}, L_{1D}, and L_{0D} be three literal operations $\overline{{}^2D^2}$, $\overline{{}^1D^1}$, and $\overline{{}^0D^0}$ of D, respectively. Then, Q' can be written as

$$\begin{aligned} Q' &= {}^2D^2 + 1\cdot {}^1D^1 + \overline{{}^1D^1}\cdot\overline{{}^0D^0}\cdot Q \\ &= {}^2D^2 + 1\cdot {}^1D^1 + {}^2D^2\cdot Q \\ &= {}^2D^2(2+Q) + 1\cdot {}^1D^1 \\ &= {}^2D^2 + 1\cdot {}^1D^1. \end{aligned} \tag{11}$$

According to Eq. (4), Eq. (11) can be simplified as $Q'=D$.

Each track of the output can also be written as

$$\begin{cases} {}^2Q'^2 = {}^2D^2 + \overline{{}^1D^1}\cdot\overline{{}^0D^0}\cdot {}^2Q^2 = {}^2D^2, \\ {}^1Q'^1 = {}^1D^1 + \overline{{}^2D^2}\cdot\overline{{}^0D^0}\cdot {}^1Q^1 = {}^1D^1, \\ {}^0Q'^0 = {}^0D^0 + \overline{{}^2D^2}\cdot\overline{{}^1D^1}\cdot {}^0Q^0 = {}^0D^0. \end{cases} \tag{12}$$

Considering the effect of V_{CK}, Eqs. (11) and (12) can further be rewritten as

$$\begin{cases} Q' = ({}^2D^2 + 1\cdot {}^1D^1)V_{CK\uparrow} + Q\cdot V_{CKH}, \\ {}^2Q'^2 = ({}^2D^2 + \overline{{}^1D^1}\cdot\overline{{}^0D^0}\cdot {}^2Q^2)V_{CK\uparrow} + {}^2Q^2\cdot V_{CKH}, \\ {}^1Q'^1 = ({}^1D^1 + \overline{{}^2D^2}\cdot\overline{{}^0D^0}\cdot {}^1Q^1)V_{CK\uparrow} + {}^1Q^1\cdot V_{CKH}, \\ {}^0Q'^0 = ({}^0D^0 + \overline{{}^2D^2}\cdot\overline{{}^1D^1}\cdot {}^0Q^0)V_{CK\uparrow} + {}^0Q^0\cdot V_{CKH}, \end{cases} \tag{13}$$

where $V_{CK\uparrow}$ represents the rising edge of V_{CK}, and V_{CKH} represents the high voltage of V_{CK}. Eq. (13) indicates that, the RTD literal circuit shown in Fig. 3a in fact has the logic function of D flip-flop if the inputs are $\overline{{}^iD^i}$, and its single output Q and three-track-output ${}^iQ^i$ both correspond to the D flip-flop function. One of ${}^2D^2$, ${}^1D^1$, and ${}^0D^0$ can always be expressed by the other two according to Eq. (5), and compared with ${}^1D^1$, ${}^2D^2$ and ${}^0D^0$ are easier to calculate; hence, we express ${}^1D^1$ with ${}^2D^2$ and ${}^0D^0$:

$$L_{1D} = \overline{{}^1D^1} = \overline{\overline{{}^2D^2}\cdot\overline{{}^0D^0}} = \overline{L_{2D}\cdot L_{0D}}. \tag{14}$$

MVL systems have not yet been developed in spite of their potential advantages. It is difficult to establish a niche for multiple-valued systems in the binary world because of the need for cooperation with multiple-valued systems at devices, circuits, algorithm architecture, etc. The general scheme of a multiple-valued system is as shown in Fig. 5 (Etiemble and Israel, 1988). The main difficulty involved in combining the existing binary devices and circuits to create multiple-valued systems is the complexity of the encoder and decoder

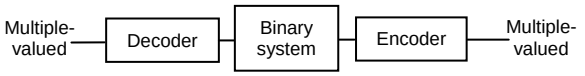

Fig. 5 General scheme of multiple-valued systems

To realize ternary D flip-flop with a single input signal, two MOBILE units (Uemura and Baba, 2000) are used as decoders. Fig. 6 shows the ternary RTD D flip-flop circuit based on the literal circuit with single input and three-track-output, which is a synchronously triggered D flip-flop. The input D is a (0, 1, 2) tri-valued signal, and ${}^2Q^2$, ${}^1Q^1$, and ${}^0Q^0$ are all (0, 2) binary signals.

The output structure is optional. If a single track output is required, the ternary RTD NAND, NOR, inverter (Yamamoto *et al*., 1999; Lin *et al*., 2007; Nunez *et al*., 2007a; 2007b) units combined with Eq. (4) can be used.

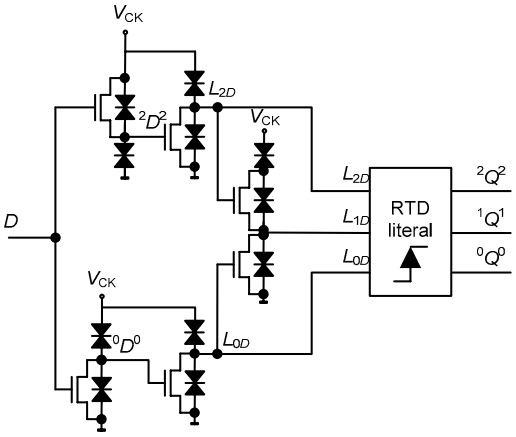

Fig. 6 Ternary resonant tunneling diode (RTD) D flip-flop with single input and three-track-output

The ternary RTD NAND, NOR, and inverter (Fig. 7) act as the encoder. The ternary RTD D flip-flop has the structure of a single track output with tri-value or three-track-output, where each track is a binary signal. These two structures can be converted easily. All the internal units of the circuit are binary units with the value (0, 2). Using binary units to realize a ternary logic circuit, it can be easier to understand both design steps and theoretical basis, and the circuits are very simple. The ternary RTD D flip-flop shown in Fig. 6 easily solves the algebraic interface problems between the tri-valued circuits and the binary circuits.

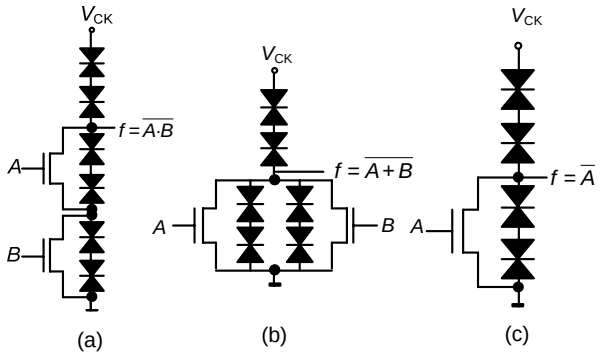

Fig. 7 Ternary resonant tunneling diode (RTD) logic units (a) Ternary RTD NAND unit; (b) Ternary RTD NOR unit; (c) Ternary RTD inverter

4.2 Ternary RTD D flip-flop with pre-set and pre-reset functions

The initial state of the ternary RTD D flip-flop shown in Fig. 6 is an unknown value. To enable the D flip-flop to have an identified initial state, the input L_{iD} should be controlled by setting different values. SET and RESET control signals are added to the input; they are both (0, 2) binary signals (Table 2). When SET and RESET are both logic '0', there is no effect on L_{iD}; other combinations of SET and RESET can make L_{iD} a different state to create setting '0' or '2' functions when it is three-track-output structure or setting '0' or '1' or '2' functions when it is single-track output structure.

Table 2 Logic functions of SET and RESET

SET	RESET	L_{2D}	L_{1D}	L_{0D}
0	0	$\overline{^2D^2}$	$\overline{^1D^1}$	$\overline{^0D^0}$
0	2	2	2	0
2	0	0	2	2
2	2	2	0	2

The Karnaugh maps of pre-set and pre-reset functions are shown in Fig. 8. According to the Karnaugh maps, the equations are as follows:

$$\begin{aligned} L_{2D} &= \overline{^2D^2}\cdot\overline{\mathrm{SET}}+\mathrm{RESET} \\ &= \overline{\overline{\overline{^2D^2}\cdot\overline{\mathrm{SET}}+\mathrm{RESET}}} \\ &= \overline{\overline{\overline{^2D^2}\cdot\overline{\mathrm{SET}}}\cdot\overline{\mathrm{RESET}}}, \end{aligned} \tag{15}$$

$$\begin{aligned} L_{1D} &= \overline{^1D^1}\cdot\overline{\mathrm{SET}}+\overline{^1D^1}\cdot\overline{\mathrm{RESET}} \\ &= \overline{\overline{^1D^1}\cdot(\overline{\mathrm{SET}}+\overline{\mathrm{RESET}})} \\ &= \overline{^1D^1+(\overline{\mathrm{SET}}+\overline{\mathrm{RESET}})}, \end{aligned} \tag{16}$$

$$\begin{aligned} L_{0D} &= \overline{^0D^0}\cdot\overline{\mathrm{RESET}}+\mathrm{SET} \\ &= \overline{\overline{^0D^0}\cdot\overline{\mathrm{RESET}}+\mathrm{SET}} \\ &= \overline{\overline{^0D^0}\cdot\overline{\mathrm{RESET}}}\cdot\overline{\mathrm{SET}}. \end{aligned} \tag{17}$$

The structure of three-track-output ternary RTD D flip-flop with pre-set and pre-reset functions is shown in Fig. 9a. Fig. 9b illustrates the characteristic curves of L_{2D} controlled by SET and RESET signals, which are effective at high level. The pre-set and pre-reset functions are synchronous. Compared with the setting of SET and RESET in traditional circuits,

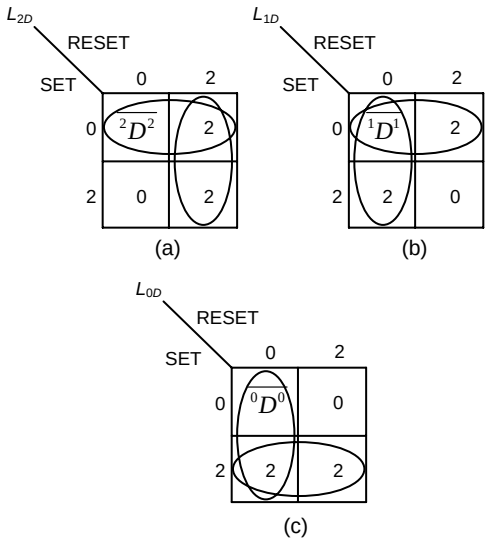

Fig. 8 Karnaugh maps of pre-set and pre-reset functions
(a) Setting '2'; (b) Setting '1'; (c) Setting '0'

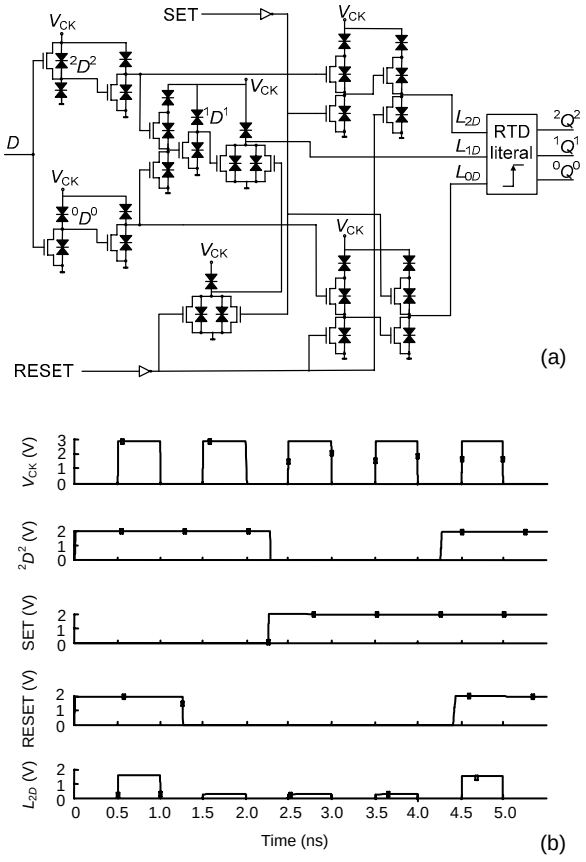

Fig. 9 Ternary resonant tunneling diode (RTD) D flip-flop with pre-set and pre-reset functions
(a) Structure of three-track-output ternary RTD D flip-flop with pre-set and pre-reset functions; (b) Characteristic curves of L_{2D} controlled by SET and RESET signals

when SET and RESET are both valid, the RTD D flip-flop also has correct logic. Therefore, all the states of SET and RESET are fully utilized and the structure is simplified to the extreme.

5 Conclusions

A ternary literal circuit with three-track-output based on RTD is presented, each track of which is a set of (0, 2) binary signals. The internal units of the RTD literal are also binary logic circuits. Combined with the definition and properties of the literal operation, the D flip-flop with pre-set and pre-reset functions based on RTD literal circuit is designed to create tri-valued logic, which can solve the compatibility problem between binary logic circuits and multiple-valued logic circuits. Although there are other structures of a ternary RTD D flip-flop (Uemura and Baba, 2001a; 2001b), the proposed RTD literal circuit with three-track-output can not only be designed with optional single-track-output, but also be used in the design of other types of RTD flip-flop.

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