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A 20 μW 95 dB dynamic range 4th-order Delta-Sigma modulator with novel power efficient operational transconductance amplifier and resonator*

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Abstract: A low power high performance Delta-Sigma modulator for portable measurement applications is presented. To reduce power consumption while maintaining high performance, a fully feedforward architecture with a comprehensive system-level design is implemented. As a key building block, a novel power efficient current mirror operational transconductance amplifier (OTA) with a fast-settling less-error switched-capacitor common-mode feedback (SC CMFB) circuit is introduced, and the effects of both gain nonlinearity and 1/*f* noise of OTA are discussed. A new method to determine the voltage gain of an OTA is also proposed. The bottom terminal parasitic effect of poly-insulator-poly (PIP) capacitors is considered. About an extra 20% of capacitance is added to the total capacitance load. A power and area efficient resonator is adopted to realize a coefficient of 1/90 for 50% power and 75% area reduction compared with conventional designs. The chip is implemented in a low cost 0.35 μm complementary metal oxide semiconductor (CMOS) process. The total power consumption is 20 μW with a 1.5 V supply, and the measured dynamic range (DR) is 95 dB over a 1 kHz bandwidth. Experimental results show that a high figure-of-merit (FOM) is achieved for the designed modulator in comparison with those from the literature.

Key words: Low power, High performance, Power efficient OTA and resonator, Delta-Sigma modulator
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1 Introduction

Low power portable electronic systems, such as portable measurement systems, implantable medical devices, and digital cameras, are in great demand for today's consumer electronic products (Rabii and Wooley, 1997; Yao *et al*., 2004). Hence, power efficiency is a key consideration in the design of circuits for such applications (Roh *et al.*, 2008). Reducing supply voltage is an easy and efficient way to reduce power consumption. However, its contribution to low power analog circuit designs is restrained by the threshold voltage since too low a threshold voltage will give rise to the static leakage power issue (Chae and Han, 2009) in modern digital technologies. Thus, it is necessary to develop other approaches for achieving power efficient circuit designs.

Owing to the wide application of Delta-Sigma modulators in portable products, many low power high performance designs have been reported in recent years. Utilization of an advanced complementary metal oxide semiconductor (CMOS) process with a low threshold voltage is a common method, but it is quite costly (Yao *et al.*, 2004; Roh *et al.*, 2008). Some systems were implemented by using the switched-opamp technique, which reduces the power consumption and the switch number in signal paths simultaneously (Peluso *et al.*, 1997; Sauerbrey *et al.*, 2002; Goes *et al.*, 2006). However, in these systems, the first sampling switch is still insufficiently driven and the power efficiency of switched-opamps is not

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high enough. As for the operational transconductance amplifier (OTA), a body-driven technique was used to reduce the supply voltage and power consumption (Pun *et al.*, 2006). However, body-driven transistors have a low bandwidth due to their small transconductance and have some limitations including those caused by bad noise performance (Rajput and Jamuar, 2002). To remove the OTAs for better power savings, inverter- and comparator-based switched-capacitor circuits were proposed in some recent publications (Fiorenza *et al.*, 2006; Chae and Han, 2007; 2009). An inverter-based circuit can be used to replace the OTA since it can operate at a very low supply voltage to save power. A comparator-based system has the potential for significant power reduction compared with an OTA-based design because it needs to drive only the switched-capacitor loads. However, it is difficult for these two OTA-less techniques to achieve a resolution up to 14-bit or more because of the residual offset and stringent conditions for their operating region.

To reduce manufacturing cost, our design combines a comprehensive system-level design with a meticulous design of a novel power efficient OTA and resonator. Also, a modulator featuring low power and high performance in a low cost standard 2-poly 4-metal (2P4M) 0.35 μm CMOS process is proposed. In other words, our efforts were focused on the performance and power optimization of the modulator without the use of any costly advanced technology.

2 System-level design

2.1 Modulator topology

Compared with multi-stage noise shaping (MASH) topology, a single-loop modulator is suitable for low voltage, low power applications since it has better immunity to an analog circuit's non-idealities such as OTA DC gain and switch on-resistance (Yao *et al.*, 2004). Also, instead of the classical feedback architecture, a fully feedforward architecture which has been widely used in recent years was adopted in this design (Silva *et al.*, 2001; Yang *et al.*, 2003; Yao *et al.*, 2004; Gharbiya and Johns, 2006). This architecture has extra signal paths from the outputs of integrators to the quantizer. Therefore, most signal energy can be prevented from leaking into the modulator loop. Hence, the design requirements of OTAs can be relaxed, and the total power consumption of the proposed modulator will be reduced.

Although single-loop multi-bit topology can achieve lower power consumption with a lower oversampling ratio (OSR), it is hard to realize a feedback digital-to-analog converter (DAC) with linearity much better than 12-bit without trimming (Schreier and Temes, 2004). Usually, dynamic element matching (DEM) circuits with extra power and area cost are required to remove the nonlinearity and in-band tones caused by the capacitor-element mismatch of feedback DAC (Schreier and Temes, 2004). Also, a super low power area efficient multi-bit quantizer is difficult to implement since the resistor-string of voltage reference and the comparator with a preamp in this quantizer dissipate a lot of extra static power and area. Therefore, a single-loop single-bit modulator topology with inherent linearity was introduced for low power medical measurement applications in this design.

The achievable peak signal-to-quantization-noise ratio (SQNR) for single-bit modulators of orders N=1 to 8 is shown in Fig. 1 (Schreier and Temes, 2004). There are three main topologies with an SQNR of more than 100 dB. The first has the order N=7 with OSR=32. This order N is too high to maintain stability. The other two topologies have the order N=4 with OSR=64 and the order N=3 with OSR=128, respectively. Comparing the total power consumption, especially that of decimation filters, 4th-order modulator topology with OSR=64 was proposed due to its low sampling frequency and power saving of about 50%.

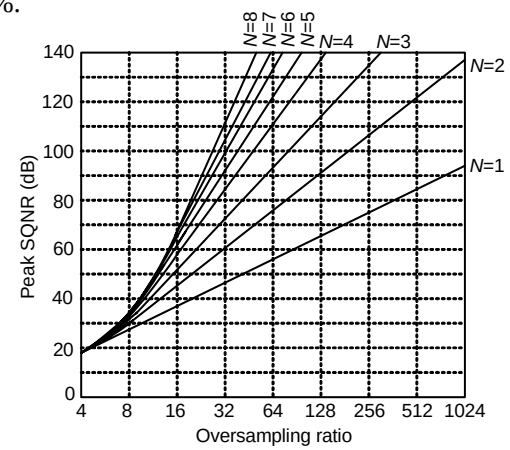

Fig. 1 Empirical signal-to-quantization-noise ratio (SQNR) limit for one-bit modulators of orders N=1 to 8

Two single-loop, single-bit 4th-order Delta-Sigma modulator topologies with OSR=64 are shown in Fig. 2. The coefficients of these two feedforward modulators are summarized in Table 1. The coefficient g_1 of the modulator in Fig. 2a is too small to be realized under current CMOS technologies. Besides, due to the small coefficient g_1, the values of the sampling and resonator capacitors in the first integrator would need to be increased greatly to keep the total thermal noise low enough. Thus, both the capacitance load and the power consumption of the first OTA would be increased significantly. The topology in Fig. 2b was proposed to overcome these difficulties. There is a local resonator feedback loop with a gain coefficient of g between the last two integrators, which is used to put two zeros at the edge of the signal band and to improve the performance. The noise transform function (NTF) of the proposed modulator can be calculated as

$$\mathrm{NTF}(z)=\frac{(z-1)^2[(z-1)^2+c_4gz]}{A\cdot B+[a_3(z-1)+a_4c_4]c_1c_2c_3z}, \quad (1)$$

where

$$A=(z-1)^2+a_1c_1(z-1)+a_2c_1c_2,\ B=(z-1)^2+c_4gz.$$

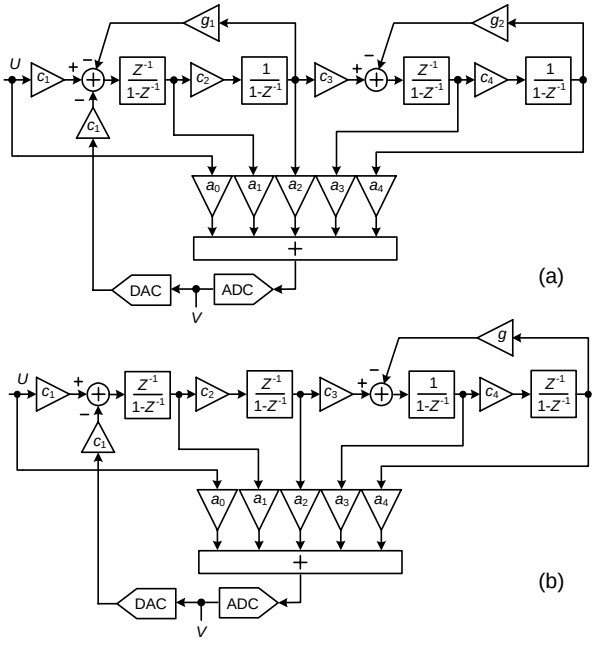

Fig. 2 Two single-loop 4th-order modulator topologies
(a) Two resonators; (b) One resonator

Table 1 Coefficients of the modulator shown in Fig. 2a and the proposed modulator shown in Fig. 2b

Integrator coefficients	Feedforward coefficients	Resonator coefficients	
		Fig. 2a	Fig. 2b
	a_0=1.0		
c_1=1/3	a_1=2.0	g_1=1/10 000	g=1/90
c_2=2/7	a_2=3.0	g_2=1/90	
c_3=1/4	a_3=1.5		
c_4=1/7	a_4=2.0		

Fig. 3 shows a behavioral quantization noise simulation result of the proposed modulator with a clear notch in the spectrum caused by the local resonator.

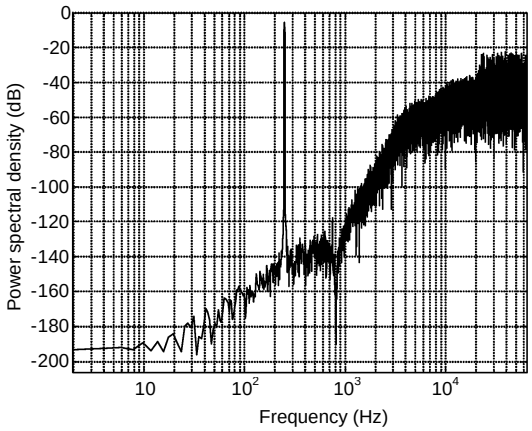

Fig. 3 Ideal output spectrum with a 250 Hz input signal

2.2 Integrator output swings

Fig. 4 shows the output swings of integrators in the proposed modulator normalized to the reference voltage while feeding a −3.7 dB input signal. Note that the largest output swing in the first integrator is about 50% of the reference voltage. Hence, the design requirements of OTAs are relaxed due to the small output swings.

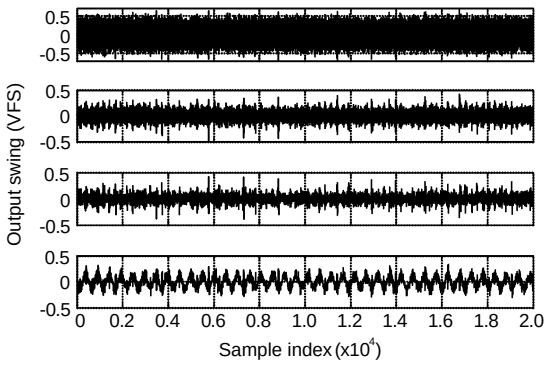

Fig. 4 Integrator output swings with a −3.7 dB input signal (for integrators 1, 2, 3, and 4 from top to bottom)

2.3 OTA requirements

As a key building block in a Delta-Sigma modulator, an OTA is adopted to compose a switched capacitor integrator. The performance of the modulator is greatly affected by the integrator in terms of power consumption and non-idealities, including finite DC gain, finite gain bandwidth (GBW), and finite slew rate (SR).

To save the energy and time of system-level design, the voltage gains of all the OTAs are sometimes regarded as the same when considering the effect of finite gain on performance (Yao *et al.*, 2004). However, this approximation is not adequate as a design guideline. In this work, a simple but efficient method is presented to determine the voltage gains of two different modulators. Another modulator similar to the proposed modulator is shown in Fig. 5. When taking into account a finite DC gain factor, the NTF of the new modulator is written as Eq. (2), and that of the proposed modulator is rewritten as Eq. (3).

$$\mathrm{NTF}(z)=\frac{E[(z-p_3)(z-p_4)+c_4g_2p_3p_4]}{C[(z-p_3)(z-p_4)+c_4g_2p_3p_4]+D}, \quad (2)$$

$$\mathrm{NTF}(z)=\frac{E[(z-p_3)(z-p_4)+c_4g_2p_3p_4z]}{C[(z-p_3)(z-p_4)+c_4g_2p_3p_4z]+Dz}, \quad (3)$$

where

$$C=(z-p_2)[(z-p_1)+a_1c_1p_1]+a_2c_1c_2p_1p_2,$$

$$D=c_1c_2c_3p_1p_2p_3[a_3(z-p_4)+a_4c_4p_4],$$

$$E=(z-p_1)(z-p_2),\quad p_i=1-1/A_{\mathrm{DC}}(i),\quad 1\le i\le 4.$$

$A_{\mathrm{DC}}(i)$ is the DC gain value of the ith OTA.

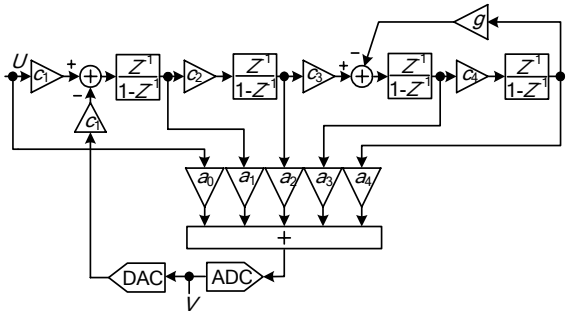

Fig. 5 Another single-loop 4th-order modulator topology

These two equations were processed in MATLAB, and the modulator noise degradation versus different DC gains was obtained easily. Fig. 6a shows the noise degradation of the new modulator from Fig. 5, and Fig. 6b gives that of the proposed modulator from Fig. 2b. Here, each figure has three curves with different opamp gains. In one curve, the DC gains of all the OTAs are variable. In another curve, the DC gains of the first two OTAs are variable while those of the other OTAs are set to 60 dB. In the last curve, the DC gains of the last two OTAs are variable while those of the other OTAs are set to 60 dB. Fig. 6a shows that the DC gains of the first two OTAs should be as large as possible (≥60 dB) while those of the other OTAs should be 60 dB in order to obtain the best noise performance from the new modulator. Also, to achieve the best noise performance from the proposed modulator, the DC gains of all the OTAs should be as large as possible (≥60 dB). Fig. 7 plots the NTFs of the proposed modulator with different DC gains. The same conclusion on the selection of voltage gain can be inferred.

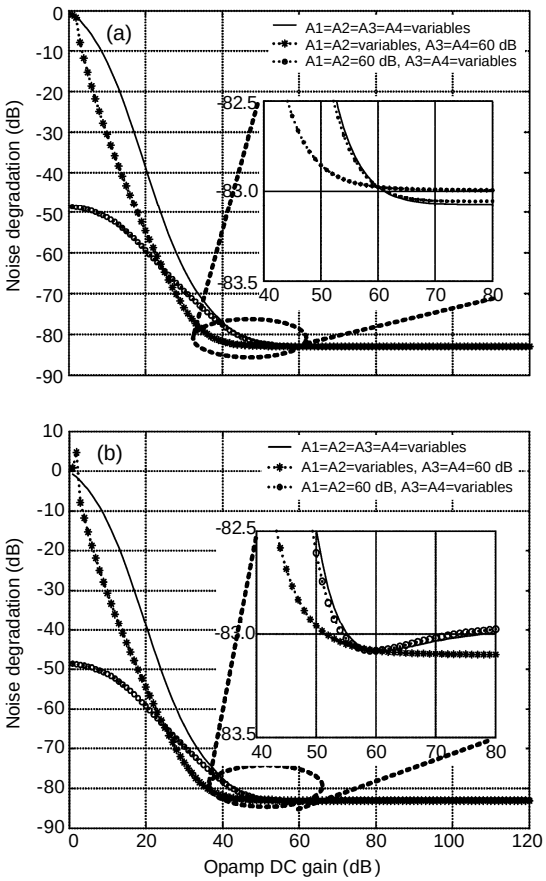

Fig. 6 Noise degradation versus different DC gains
(a) New modulator from Fig. 5; (b) Proposed modulator from Fig. 2b

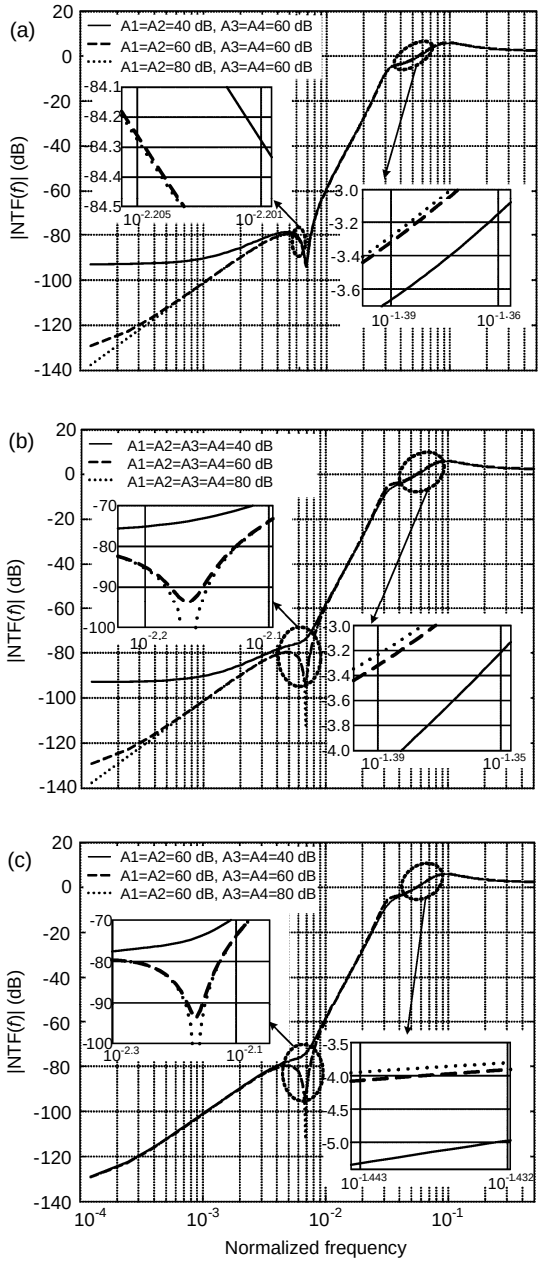

Fig. 7 Noise transform functions (NTFs) of the proposed modulator with different voltage gains
(a) Type 1; (b) Type 2; (c) Type 3

Usually, the voltage gain of an OTA is not constant over the required output-swing range. To ensure a high performance, the gain should be kept large enough (≥60 dB) over the whole range (Park *et al.*, 2009). Hence, the effect of gain nonlinearity on the performance is also discussed. Eq. (4) is used to denote the voltage gain with a nonlinearity coefficient *B*:

$$A_{\mathrm{DC}}(V_{\text{out-swing}}) = \frac{A_{\mathrm{DC}}(0)}{1 + BV_{\text{out-swing}}}, \tag{4}$$

where $A_{\mathrm{DC}}(0)$ is a constant gain and $V_{\text{out-swing}}$ is the output swing of an integrator.

When the coefficient *B* is set to 0, the voltage gain is constant. When the coefficient *B* is increased, the effect of gain nonlinearity is deteriorated. Fig. 8 shows a plot of modified voltage gains versus output-swings and gain nonlinearity coefficients *B*. An integrator behavioral model in SIMULINK was then developed with this equation. Peak SQNR with the effect of gain nonlinearity was readily obtained. Fig. 9 shows that, to ensure a peak SQNR above 100 dB, the gain should be above 58 dB with a gain nonlinearity coefficient *B* of less than 2.

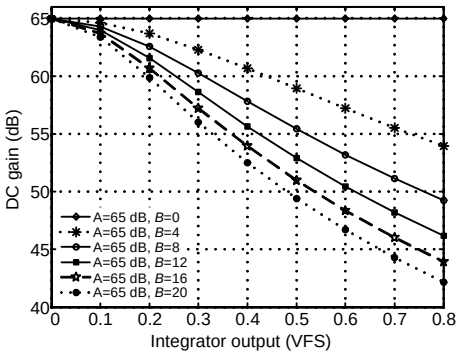

Fig. 8 Modified voltage gain versus output swings and gain nonlinearity coefficients *B*

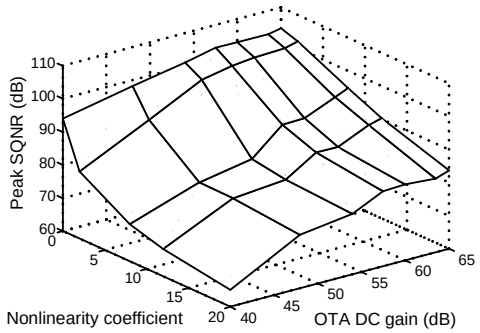

Fig. 9 Peak signal-to-quantization-noise ratio (SQNR) degradation with voltage gain nonlinearity in the proposed modulator

Fig. 10 shows the peak SQNR with the finite slew rate and GBW of the proposed modulator. To keep the peak SQNR above 100 dB, OTAs should satisfy the specifications summarized in Table 2.

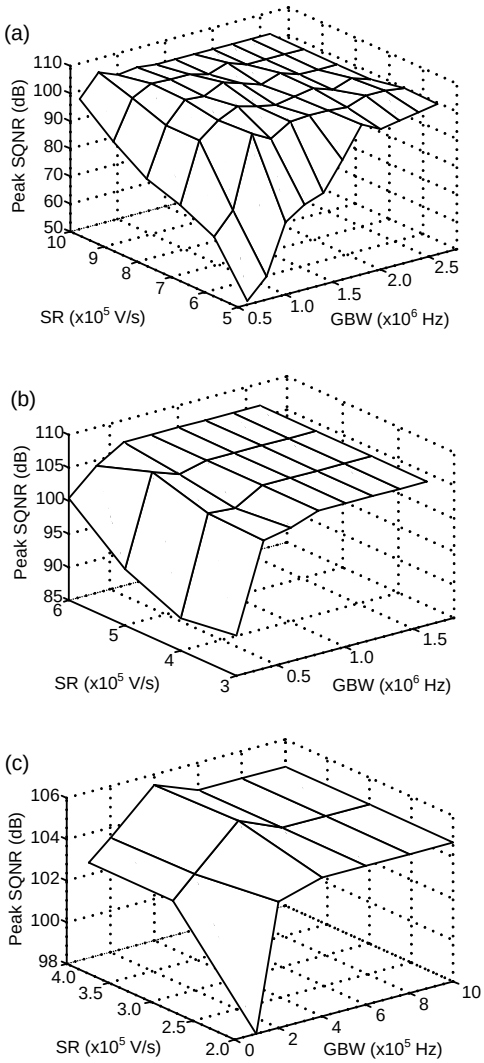

Fig. 10 Peak signal-to-quantization-noise ratio (SQNR) degradation with finite slew rate (SR) and gain bandwidth (GBW)

(a) OTA 1; (b) OTA 2; (c) OTAs 3 & 4

Table 2 Specifications of the designed operational transconductance amplifiers (OTAs)

OTA	Gain (dB)	GBW (MHz)	Slew rate (V/μs)
1	≥60	≥1.8	≥0.8
2	≥60	≥1.4	≥0.5
3, 4	≥60	≥0.7	≥0.3

GBW: gain bandwidth

2.4 Effect of 1/*f* noise in integrators

The required bandwidth of the proposed modulator is 20–1000 Hz. Since 1/*f* noise is a well-known low frequency noise, a 1/*f* noise cancellation technique should be adopted to ensure good noise degradation over the required bandwidth. Chopper stabilization (CHS) and correlated double sampling (CDS) are two typical low frequency noise cancellation techniques, which are usually adopted to reduce the effects of opamp imperfections including the noise (mainly 1/*f* and thermal noise) and the input-referred DC offset voltage. However, the CDS technique requires more capacitor area and induces more thermal noise (Enz and Temes, 1996). Thus, the CHS technique was used to cancel 1/*f* noise because of its simple circuit implementation.

Fig. 11 shows an improved integrator behavioral model with the CHS technique in SIMULINK. The implementation of the CHS technique model is similar to the circuit operation principle. The 1/*f* noise source is generated by MATLAB processing. Fig. 12a shows the simulation results of the proposed modulator while considering 1/*f* noise in each integrator, and Fig. 12b shows the simulation results with the CHS technique. These figures show that the 1/*f* noise of the first two integrators, especially of the first integrator, has a dominant effect on performance. Therefore, the CHS technique was adopted in the first two integrators to reduce the effect of 1/*f* noise.

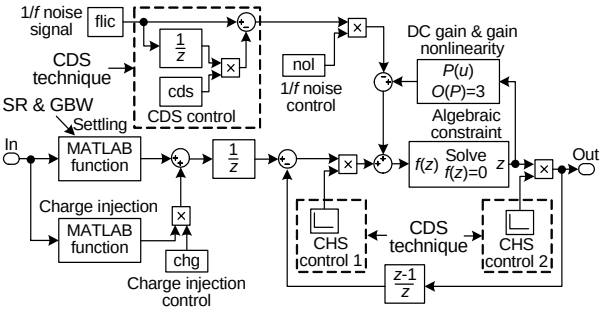

Fig. 11 An improved behavioral model of integrators in SIMULINK

2.5 Sampling capacitors and behavioral model

The sampling capacitor in the first integrator is chosen to satisfy the *KT*/*C* noise requirement, which is shown as (Rabii and Wooley, 1999)

$$C_{\mathrm{S}}=\frac{8KT\cdot \mathrm{DR}}{V_{\mathrm{in,max}}^{2}\cdot \mathrm{OSR}}, \tag{5}$$

where *K* is the Boltzmann constant, *T* is the absolute

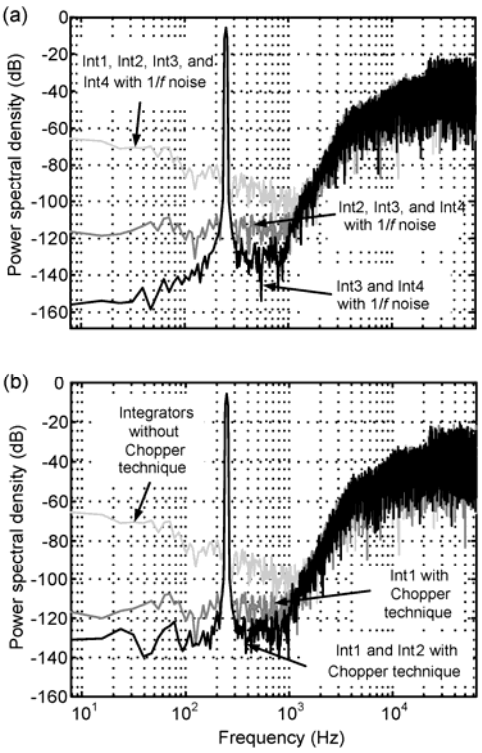

Fig. 12 Modulator simulation results
(a) With 1/*f* noise; (b) After adopting the Chopper stabilization (CHS) technique in each integrator

temperature, DR is the dynamic range, OSR is the oversampling ratio, and $V_{\text{in,max}}$ is the maximum amplitude of a sinusoidal input. Usually, $V_{\text{in,max}}$ is regarded as the amplitude of a full-scale sinusoidal input (Roh *et al.*, 2008). However, in practice, $V_{\text{in,max}}$ is impossible to achieve in the full-scale range due to the stability requirement. Thus, the maximum input amplitude of the proposed modulator was used to determine the value of the sampling capacitor. The OSR is 64 and the DR is set to 100 dB for a design margin. The maximum signal input amplitude $V_{\text{in,max}}$ is 60% of the reference voltage. For a 1.5 V reference voltage, the required sampling capacitance in the first integrator is 6.4 pF. The final sampling capacitance is 7 pF for an extra noise margin. The values of other capacitances are summarized in Table 3.

Table 3 Capacitors of the proposed modulator

Sampling capacitors	Integrating capacitors
C_{s1}=7.0 pF	C_{i1}=21.0 pF
C_{s2}=1.0 pF	C_{i2}=3.5 pF
C_{s3}=0.5 pF	C_{i3}=2.0 pF
C_{s4}=0.2 pF	C_{i4}=1.4 pF

To evaluate the effects of non-ideal factors completely, an integrator behavioral model in SIMULINK was used (Fig. 11). Here, slew rate, gain bandwidth, finite DC gain and gain nonlinearity, leakage current, *KT*/*C* noise, 1/*f* noise, CHS technique, and CDS technique were all included. The details of these models in SIMULINK can be found in Ou and Wu (2008). Using this comprehensive system level design and simulation, a low power high performance modulator structure was proposed.

3 Building block circuits design

3.1 Low voltage low power OTA

The OTA usually consumes most of the total power of a modulator. In particular, the OTA in the first integrator may consume more than half of the total power and has a decisive influence on its performance. Therefore, it is important to design a power efficient and high performance OTA.

An OTA topology with a rail-to-rail output swing is usually used in low voltage and low power designs (Yao *et al.*, 2004). Also, a high gain and wide bandwidth OTA is needed to ensure high performance. A popular approach to enhancing voltage gain is to use a folded-cascade amplifier structure. But the cascading transistor occupies extra output swing headroom and is usually noisier than other transistors (Rabii and Wooley, 1997). A single-stage OTA is more power efficient than a two-stage type because the latter has to consume much more power to drive the compensation capacitor (Yao *et al.*, 2004). Therefore, a single-stage OTA topology with a rail-to-rail output swing is preferred. For such an OTA topology, a current mirror structure is often adopted. However, in deep-submicron technologies the voltage gain of such an OTA is about 40 dB. To enhance the gain with no additional power consumption, a gain enhancement technique was proposed by Yao *et al.* (2004), which is able to provide a voltage gain over 60 dB. However, the circuit they proposed is difficult to implement in a standard 0.35 μm CMOS process for a 1.5 V supply. To solve this problem, we propose a novel OTA structure with a gain enhancement technique.

It is well known that, compared with a Class-A output stage, a Class-AB stage can provide higher power efficiency, higher slew rate, and wider rail-to-rail output swing (Yao *et al.*, 2004; Xu *et al.*,

2007). Hence, a Class-AB current mirror OTA with a current starving technique (Fig. 13) was applied to reduce the power and enhance the voltage gain. Its voltage gain and GBW are given by

$$A_{\text{Gain}} \approx \frac{1}{(V_{\text{GS1}}+V_{\text{THP1}})(\lambda_{\text{N9}}+\lambda_{\text{P12}})}\frac{1}{(1-k)}, \quad (6)$$

$$\text{GBW} \approx \frac{2B\cdot I}{(V_{\text{GS1}}+V_{\text{THP1}})C_{\text{L}}}, \quad (7)$$

where V_{GS} is the transistor voltage difference between gate and source terminals, V_{THP} is the PMOS transistor threshold voltage, λ_{N} and λ_{P} are channel length modulation coefficients of NMOS and PMOS transistors respectively, B is the current ratio of the current mirror, kI is the drain current in transistors M_3 and M_4, and C_{L} is the amplifier load capacitor.

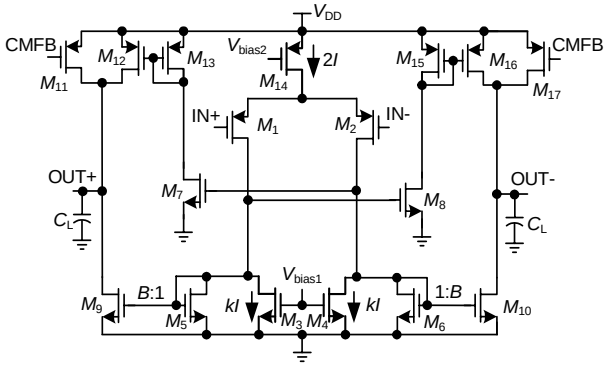

Fig. 13 Schematic of the proposed Class-AB current mirror operational transconductance amplifier (OTA) with the current starving technique

The current starving technique is realized by the transistors M_3 and M_4, which take away most of the DC current provided by the input transistors M_1 and M_2. This makes the DC current in the output transistors M_9 and M_{10} become smaller and the output resistances become higher. Thus, the voltage gain is increased. The Class-AB output stage is realized through the push-pull operation, which is implemented by using current mirrors M_6–M_{13}.

The OTA used in a modulator is usually a fully differential opamp which provides better rejection against both common-mode (CM) noise and power supply variations (Choksi and Carley, 2003). However, the output CM voltage trends to drift to the supply rails without proper control due to power supply variations, offset, etc. Hence, an additional CMFB circuit is necessary. An improved SC CMFB circuit (Fig. 14) was proposed by Choksi and Carley (2003). In this circuit, extra sets of capacitors C_1 and switches are used compared with the traditional structure. Thus, during every clock phase, the total capacitance load is constant (C_{T}=C_1+C_2). Φ_1 and Φ_2 are two non-overlapping clocks, V_{cmref} is the desired output CM voltage, V_{bias} is the expected bias voltage, and V_{cmfb} is the CM feedback voltage. This circuit also has lower error and less settling time than traditional circuits (Choksi and Carley, 2003). Its main drawback is that a few more switches and capacitors are needed.

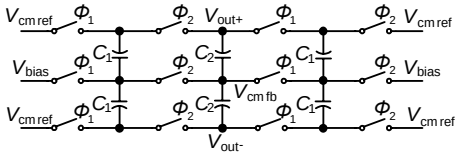

Fig. 14 An improved switched-capacitor common-mode feedback (SC CMFB) circuit

Table 4 summarizes the simulation results of the designed OTAs. The results show that the proposed OTA in the first integrator achieves a normal DC voltage gain of 65 dB with a 1.5 V supply. For an 11.4 pF load capacitor, the GBW is 2.3 MHz and the static current power consumption is only 6.6 μA. Based on the simulation, the variability of the DC voltage gain is less than 1 dB while that of the GBW is less than 0.3 MHz under different process corners. Fig. 15 shows the gain nonlinearity of the first OTA. It can be seen that the designed OTA satisfies the gain requirements introduced previously.

Table 4 Simulated performance of the designed operational transconductance amplifiers (OTAs)

Parameter	Value		
	OTA 1	OTA 2	OTAs 3 & 4
Supply voltage (V)	1.5	1.5	1.5
DC gain (dB)	65	67	66
Phase margin (degree)	63	61	71
Slew rate (V/μs)	1.1	0.9	0.8
GBW (MHz)	2.3	1.7	0.9
Load capacitance (pF)	11.4	2.9	1.9
Static current power (μA)	6.6	2.2	1.4

GBW: gain bandwidth

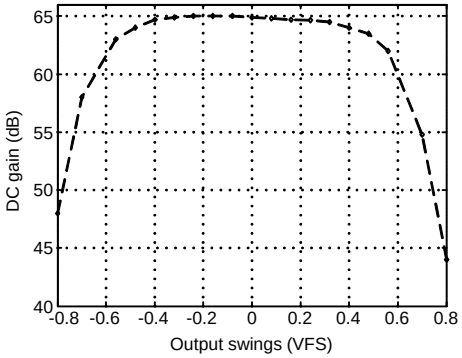

Fig. 15 First operational transconductance amplifier (OTA) voltage gain versus different output swings

In practice, when a modulator is fabricated, there are always some parasitic capacitors at the bottom terminal of the poly-insulator-poly (PIP) capacitors. In this design, this bottom terminal parasitic effect was considered. About an extra 20% of capacitance is added to the total capacitance load. The effective capacitance load $C_{\mathrm{L,eff}}$ is thus given by

$$C_{\mathrm{L,eff}} = C_{\mathrm{S}}(i) \,||\, C_{\mathrm{I}}(i) + 0.2C_{\mathrm{I}}(i) + (1+0.2)C_{\mathrm{Sum}}, \quad (8)$$

where $C_{\mathrm{Sum}}=C_{\mathrm{S}}(i+1)+C_{\mathrm{cmfb1}}+C_{\mathrm{cmfb2}}+C_{\mathrm{ff}}(i)$, $C_{\mathrm{S}}(i)$, $C_{\mathrm{I}}(i)$, and $C_{\mathrm{ff}}(i)$ are the sampling capacitor, integrating capacitor, and feedforward capacitor, respectively, of the ith integrator. $C_{\mathrm{S}}(i+1)$ is the sampling capacitor of the next integrator. C_{cmfb1} and C_{cmfb2} are the capacitors used in the CMFB circuit. The designed integrator is a half-delay type, so the sampling capacitance of the next stage should be added to the total capacitance load.

3.2 Area and power efficient resonator circuit

A local resonator with a coefficient of 1/90 was adopted in the last two integrators, so there is another input path in the third integrator. A conventional resonator structure with a gain coefficient of $C_{\mathrm{R}}/C_{\mathrm{i3}}$ is shown in Fig. 16a. Thus, if this resonator is used in this design, compared with the capacitance summarized in Table 3, the values of the sampling capacitor and integrating capacitor in the third integrator would need to be greatly increased to realize this very small coefficient. For example, when the resonator capacitor C_{R} is set to 0.1 pF, the value of the integrating capacitor C_{i3} should be 9 pF. The sampling capacitor C_{s3} is also increased to 2.25 pF. According to Eq. (8), the effective capacitance load of the third OTA is changed to 4.6 pF. This large load will increase both area and power cost.

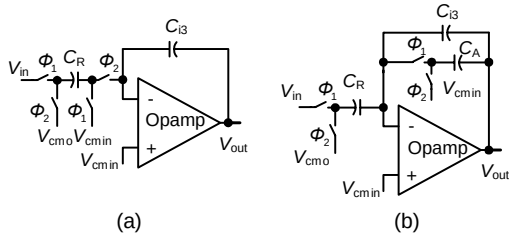

Fig. 16 Schematic diagrams and transfer functions of two resonators

(a) Traditional type, $V_{\mathrm{out}} = Z^{-1/2}C_{\mathrm{R}}V_{\mathrm{in}}/[(1-Z^{-1})C_{\mathrm{i3}}]$; (b) Proposed type, $V_{\mathrm{out}} = Z^{-1/2}C_{\mathrm{R}}C_{\mathrm{A}}V_{\mathrm{in}}/[(1-Z^{-1})C_{\mathrm{i3}}(C_{\mathrm{i3}}+C_{\mathrm{A}})]$

In our system, we introduced a parasitic insensitive power and area efficient integrator as a local resonator. The proposed integrator was used by Nagaraj (1989) to implement a notch filter. Fig. 16b shows its schematic employing three capacitors. To realize a small coefficient, C_{i3} is typically a large capacitor while C_{R} and C_{A} are small capacitors. The circuit operation is as follows: during phase 1, a charge $V_{\mathrm{in}}C_{\mathrm{R}}$ is transferred from C_{R} to C_{i3}, and the intermediate output voltage $V_{\mathrm{o}}(n-1/2)$ is sampled by C_{A}. During phase 2, C_{R} withdraws the charge $V_{\mathrm{in}}C_{\mathrm{R}}$ from C_{i3}, and C_{A} redistributes its charge with C_{i3}. Its z-domain transfer function can be written as

$$V_{\mathrm{out}} = \frac{z^{-1/2}}{1-z^{-1}} \frac{C_{\mathrm{R}}C_{\mathrm{A}}V_{\mathrm{in}}}{C_{\mathrm{i3}}(C_{\mathrm{i3}}+C_{\mathrm{A}})}. \quad (9)$$

According to Eq. (9), this circuit structure can be used as a local resonator in Delta-Sigma modulators. Therefore, when realizing a coefficient of 1/90 with this resonator, the values of both C_{s3} and C_{i3} do not need to be changed, and the values of C_{R} and C_{A} are simply set to 0.2 pF and 0.25 pF, respectively. Now, the effective capacitance load of the third OTA is decreased to 1.9 pF. Compared with the conventional resonator, our proposed resonator saves about 75% capacitor area and 50% power consumption in calculation and simulation.

3.3 Other main circuit blocks

The design requirements of a single-bit quantizer can be relaxed for a single-loop modulator since the

non-idealities of the quantizer can also experience noise-shaping (Roh *et al.*, 2008). Thus, a simple dynamic comparator with an SR latch was used in this work. The details of this quantizer can be found in Roh *et al.* (2008).

In our design, the clock generator was made on-chip. To ensure an adequately low switch-on resistance in a low voltage environment, especially for the switches in the first integrator, a clock boosting circuit with a voltage doubler was adopted to boost the clock signal above V_{DD}. The circuit implementation of the clock generator was introduced by Rabii and Wooley (1997).

3.4 Complete modulator circuit

The complete modulator is shown in Fig. 17. It is a fully feedforward modulator and has four integrators with a one-bit quantizer. The CHS technique was used in the first two integrators to reduce the effect of 1/*f* noise, and a proposed power and area efficient resonator with a coefficient of 1/90 is between the third integrator and the fourth integrator, which can improve the SQNR performance of the designed modulator. The input CM voltage V_{cmin} is set to 0.3 V, and the output CM voltage V_{cmo} is set to $V_{DD}/2$.

4 Measurement results

The proposed modulator was implemented in a standard 2P4M 0.35 μm CMOS process. A photograph of the fabricated chip is shown in Fig. 18. Its core size is 1.37 mm×0.65 mm. Four integrators with their respective capacitors, OTAs, and switches are on the left side; the clock generator and bootstrapped circuits are on the right side. The middle part includes the feedforward circuit and the quantizer. Hence, analog circuits and digital circuits are separated to avoid the interactions of these circuits. Also, small unit capacitors are laid out in symmetry to realize the accurate coefficients and match the positive and negative signal paths.

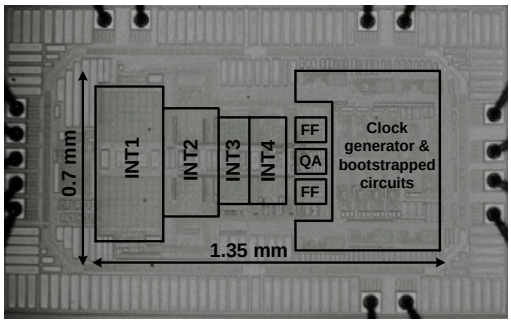

Fig. 18 Chip photograph

The test board including the single-ended-to-differential circuit (SEDC), high precision voltage references, low drop out (LDO) power supply voltages, and clock signal isolation circuit is shown in Fig. 19. Separate power supplies for analog and digital circuits, local bypass capacitors, and simple filters were adopted to reduce noise in the measurement. The input signal of the test board is provided by a high precision audio precision (AP), and the output data of the designed modulator is captured by a logical analyzer and processed by MATLAB procedures.

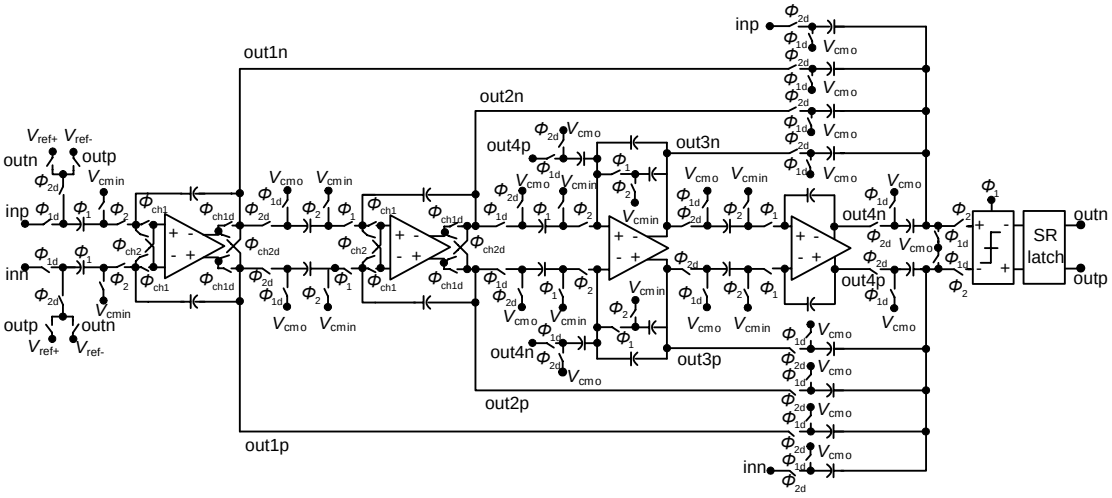

Fig. 17 Circuit implementation of the proposed 4th-order modulator

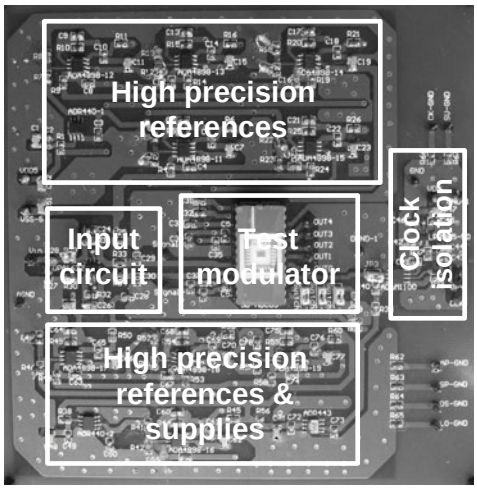

Fig. 19 Test board

The output signal of the SEDC (Fig. 20) is used as the input signal of the designed modulator. A noise of 50 Hz power frequency and its harmonic distortions appear in the frequency spectrum. When estimating the performance, this noise and its harmonic distortions are not considered. The measured output spectrum of a 250 Hz sinusoidal signal with 40 960 samples is shown in Fig. 21. Fig. 22 shows the measured SNR and signal-to-noise and distortion ratio (SNDR) curves versus different input signal amplitudes normalized by the reference voltage. As the input signal amplitude becomes large, its harmonic distortions appear in the spectrum. But their amplitudes are small enough to be ignored since the GBW and slew rate of the designed OTAs are sufficiently large. The peak SNR reaches 90.2 dB while the peak SNDR without power frequency noise is 89.8 dB. Even when the power frequency noise is considered, the measured peak SNDR is still 88.4 dB. The DR is measured as 95 dB over a 1 kHz bandwidth.

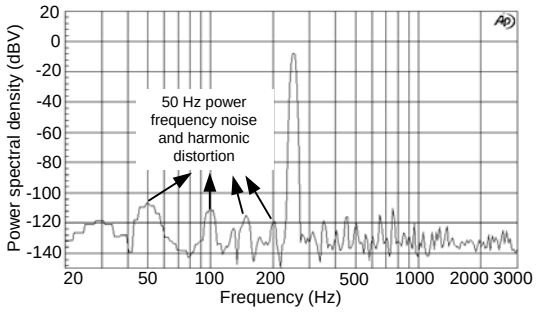

Fig. 20 Spectrum of the input signal for the designed modulator

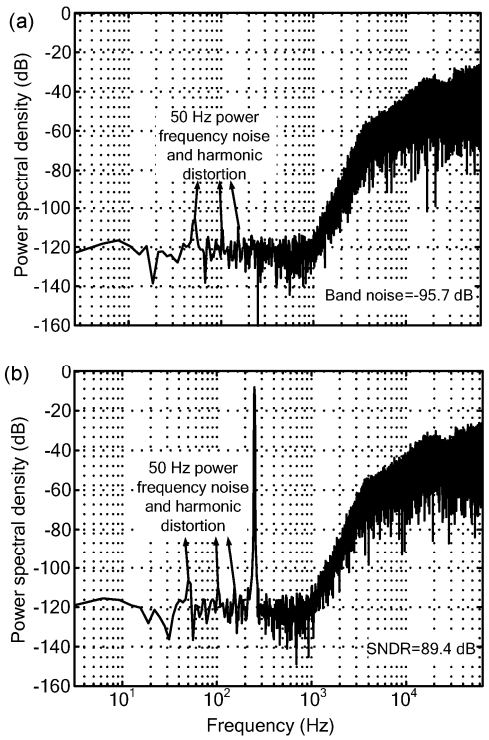

Fig. 21 Measured output spectrum of the designed modulator with 40 960 samples
(a) Noise floor; (b) With a −6.3 dB input signal

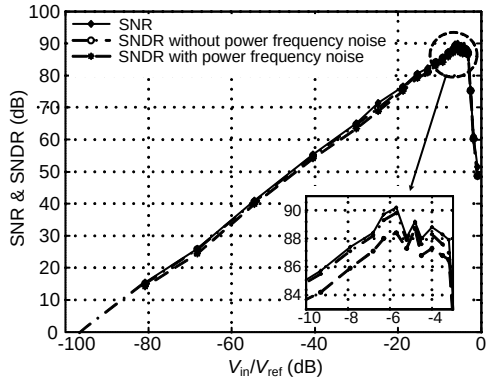

Fig. 22 Measured signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) versus input amplitude

Clocked at 128 kHz, the total power consumption including the digital circuits is only 20 μW with a 1.5 V supply. The details of measurement results are summarized in Table 5.

Table 6 lists the performance of our modulator compared with that of recently published low power high performance Delta-Sigma modulators. The FOM is defined as

$$\mathrm{FOM} = \mathrm{DR}/\mathrm{dB} + 10\lg\frac{\mathrm{BW}/\mathrm{Hz}}{P/\mathrm{W}}, \qquad (10)$$

where BW is the signal bandwidth and P is the total power consumption. Table 6 clearly shows that the FOM of our designed modulator is the highest among the systems compared.

Table 5 Performance summary of the designed modulator

Parameter	Measurement results
Supply voltage	1.5 V
Power	
Analog	18 μW
Digital	2 μW
Peak SNR	90.2 dB
Peak SNDR	89.8 dB
Dynamic range	95.0 dB
Sampling frequency	256 kHz
Signal bandwidth	1 kHz
OSR	64
FOM	172

SNR: signal-to-noise ratio; SNDR: signal-to-noise and distortion ratio; OSR: oversampling ratio; FOM: figure-of-merit

Table 6 Performance comparison with recently published systems

Parameter	Value				
	ISSCC*	JSSC1	JSSC2	JSSC3	This work
Process (nm)	180	90	130	350	350
V_{DD} (V)	0.7	1.0	0.9	1.2	1.5
f_s (MHz)	10.24	4	2	2	0.128
Bandwidth (kHz)	8	20	20	8	1
Power (μW)	80	140	60	5.6	20
Dynamic range (dB)	75	88	83	76	95
Peak SNR (dB)	70	85	82.2	72	90.2
Peak SNDR (dB)	67	81	73.1	63	89.8
FOM	155.0	169.5	168.2	167.5	172.0

* From Sauerbrey *et al.* (2002). JSSC1, JSSC2, and JSSC3 are from Yao *et al.* (2004), Roh *et al.* (2008), and Chae and Han (2009), respectively. SNR: signal-to-noise ratio; SNDR: signal-to-noise and distortion ratio; FOM: figure-of-merit

5 Conclusions

A 20 μW 95 dB DR single-bit 4th-order Delta-Sigma modulator was implemented in a low cost 0.35 μm CMOS process. A fully feedforward architecture was adopted to reduce the output swings of integrators, and a comprehensive system-level design to improve the performance of the modulator was discussed in detail. A highly efficient method was developed to determine the voltage gain and to consider the effects of both gain nonlinearity and 1/*f* noise. At the circuit-level design, a novel low voltage power-efficient Class-AB current mirror OTA with a fast-settling less-error CMFB circuit was proposed. To realize a coefficient of 1/90, a power and area efficient resonator was introduced with 50% power and 75% area reduction in comparison with conventional designs. Experimental results showed that the FOM of the proposed modulator was high and suitable for low power medical measurement applications.

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