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Current oscillations and low-frequency noises in GaAs MESFET channels with sidegating bias*

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Abstract: Low-frequency noises (LFN) and noise-like oscillations (NLO) in GaAs metal semiconductor field effect transistor (MESFET) channel current were investigated under sidegating bias conditions. It was found that the fluctuations of the channel current were directly dependent upon the sidegating bias. As the sidegating bias decreased, the amplitudes of the oscillations would increase correspondingly. Furthermore, the LFN and NLO would attenuate sharply when the sidegating bias increased to more than a certain voltage. Two mechanisms are presented to demonstrate that the effective substrate resistivity or the channel-substrate junction modulated by sidegating bias and deep level traps would take responsibilities for the LFN and NLO.

Key words: Low-frequency noises (LFN), Effective substrate resistivity, Channel-substrate junction, Sidegating bias
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1 Introduction

Low-frequency noises (LFN) in current (Dobrzański and Wolosiak, 2000; Wong, 2003; Izpura, 2007; 2008; Lin *et al*., 2007; Chiu *et al*., 2008; Zutavern *et al*., 2009), such as thermal noise, 1/*f* noise, generation-recombination noise, diffusion noise, and shot noise, as well as noise-like current oscillations (NLO) (Ding *et al*., 2005), have been reported in various GaAs field effect transistor (FET) structures. Recently, more attention has been paid to LFN and NLO due to their effect on the performance of low-noise monolithic microwave integrated circuits (MMICs). The main characteristics of LFN and NLO are: (1) LFN and NLO strongly depend upon the substrate material quality; (2) LFN and NLO are dependent upon the fabrication procedure and bias condition; (3) Oscillation amplitudes of LFN and NLO are typically of the order of 0.1–5.0 μA, approximately lower than the leakage current by three orders of magnitude; (4) LFN and NLO are sensitive to illumination.

The exact mechanism of LFN and NLO in GaAs MESFET current is not completely clear, but a great deal of effort has been devoted to understanding its behavior. Birbas *et al*. (1991) investigated the influence of the backgating effect on LFN in GaAs MESFETs and presented an explanation in terms of a negative capacitive coupling of noise produced on the substrate side of the channel/substrate junction. Dobrzański and Wolosiak (2000) claimed that charge fluctuations in the Shockley-Read-Hall (SRH) centers inside the depleted layer below the gate electrode are likely to be the origin of LFN in GaAs MESFETs, while Ding *et al*. (2005) argued that low frequency oscillations observed in MESFET was directly related to the peculiarities of the channel-substrate (C-S) junction and impact ionization of deep level traps, such as EL_2, under high field.

In this paper, LFN and NLO in GaAs MESFET channel current are investigated under sidegating conditions, and two mechanisms are proposed. One argues that the effective substrate resistivity should take full responsibility for LFN and NLO, and the

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other attempts to prove that the C-S junction modulated by sidegating bias and deep level traps (DLTs) are directly associated with the fluctuations of channel current.

2 Test pattern and device structure

The test pattern for investigating LFN and NLO in experiments is as shown in Fig. 1a. The structure and schematic of the device used for electrical measurements are as shown in Fig. 1b. The test device comprised a 10 μm×10 μm sidegate (SG) and MESFETs. The gate (G) width of MESFET was 10 μm, and the length was 2 μm. FETs and SG were fabricated on undoped liquid encapsulated Czochralski (LEC) SI GaAs substrate. Selective silicon ions implantation was used with a dose of 6×10^{12} cm^{-2} at 60 keV for n layer, and 1.5×10^{13} cm^{-2} at 30 keV for n$^+$ regions. Annealing was carried out at 940 °C for 10 s. The devices were laterally isolated by Boron ions implantation at 80 keV with a dose of 8×10^{12} cm^{-2}. The distance between SG and the MESFET was 20 μm. The gate was made by alloying Ti/Pt/Au, and the alloy for ohmic contact is Au/Ge/Ni/Au. The fringe portions of all these contacts and probe pads were in direct contact with the substrate. Larger

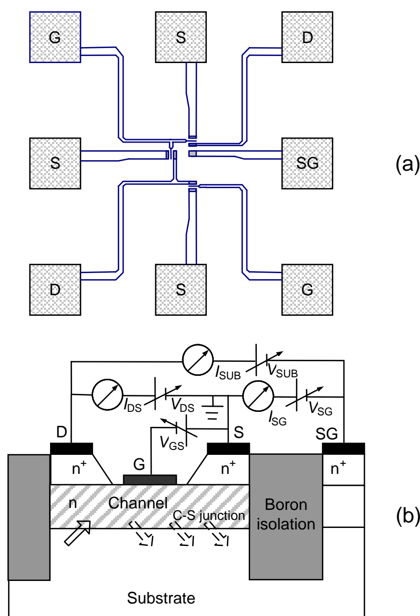

Fig. 1 Test pattern used in sidegating measurements (a) and structure and schematic of the device used for electrical measurements (b)
SG: sidegate; G: gate; S: source; D: drain

metallic pads of size 100 μm×100 μm were deposited and slightly alloyed for wire bonding.

To investigate LFN and NLO in channel current of MESFET, measurements were made at room temperature. Keeping the substrate floating and the source (S) of MESFET grounded, the gate bias (V_{GS}) and drain bias (V_{DS}) varied from 0 to −3 V and from 0 to 4 V, respectively. The sidegating bias (V_{SG}) varied negatively from 0 to −20 V with a step of 30 mV. The substrate bias (V_{SUB}) varied from 0 to −10 V. The channel current (I_{DS}) versus V_{DS} with different sidegating biases and the substrate leakage current (I_{SUB}) versus V_{SUB} were recorded with a semiconductor parameter analyzer HP4145B (Agilent Technologies, USA) whose ‘integration time’ was set to ‘short’, and ‘delay time’ was set to 1 s. The channel current spectrum with different V_{SG} was obtained using a dynamic signal analyzer HP3516A (Agilent Technologies, USA).

3 Experimental results

To investigate the LFN and NLO in channel current, the channel current was recorded as sidegating bias decreased (Fig. 2). Fig. 2a shows that I_{DS}-V_{SG} exhibited a typical sidegating effect, in which the channel current and pinch-off voltage of MESFET were reduced abruptly when the negative bias increased beyond a critical value V_{TSG} (Zhao *et al.*, 2000). In this case, V_{TSG} was approximately −3.8 V. It can be expected that the channel will be pinched off for any sidegating bias voltage more negative than −3.8 V. Remarkable LFN and NLO can be observed in I_{DS}-V_{DS} with V_{SG} varying negatively (Figs. 2b–2f). As V_{DS} was raised to the point where the channel current was becoming saturated, the channel current became noisy. In agreement with the earlier work (Birbas *et al.*, 1991; Chiu *et al.*, 2008), it can be found that the oscillations were enlarged as V_{SG} decreased. While at the same time, note that the amplitude of LFN and NLO approached the peak when V_{SG} reached V_{TSG}, and that it attenuated sharply when V_{SG} decreased to more than a certain voltage. This is in direct contrast to the previous reports. Also, Figs. 2b and 2f show that the saturation current with V_{SG}=−5 V was less than that with V_{SG}=0 V. In short, LFN and NLO in MESFET channel current have a direct dependency upon the sidegating bias conditions.

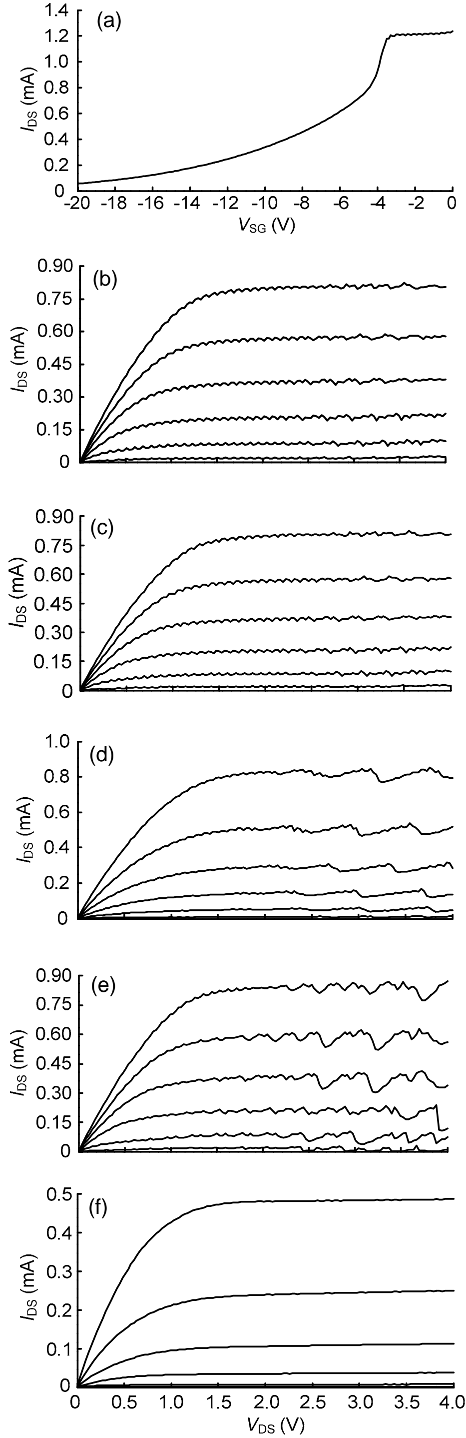

Fig. 2 Hysteresis behavior of channel current with sidegating bias decreasing with V_{DS}=1.5 V (a) and LFN and NLO with V_{SG}=0 V (b), V_{SG}=−0.8 V (c), V_{SG}=−3 V (d), V_{SG}=−3.8 V (e), and V_{SG}=−5V (f)

For the six curves in (b)–(f), from top to bottom, V_{GS}=0, −0.3, −0.6, −0.9, −1.2, and −1.5 V. I_{DS}: drain-source current; V_{SG}: sidegating bias; V_{DS}: drain bias

To thoroughly study the strong dependency between LFN and NLO in channel current and sidegating bias, the channel current spectrum of MESFET with different sidegating biases is measured. The spectral intensity of the channel current fluctuations is represented as (Birbas *et al*., 1991)

$$S(f)=\alpha_{\mathrm{H}}qI_{\mathrm{DS}}v_{\mathrm{s}}/(fL), \tag{1}$$

where α_H is the Hooge parameter, f is the frequency, I_{DS} is the channel current, v_s is the effective saturation velocity, and L is the channel length, which equaled 2 μm in the experiments.

With V_{GS}=0 V and V_{DS}=2.5 V, the channel current spectrum with different sidegating biases was obtained (Fig. 3). Note that the spectra intensity approximately followed an inverse proportionality to frequency. The magnitude of LFN and NLO increased as V_{SG} became more negative, and the oscillations became maximum when V_{SG} reached the sidegating threshold (V_{SG}=−3.8 V). Also, note that the magnitude of the LFN and NLO dropped by a factor of nearly 10000 (e.g., it practically disappears) when V_{SG} was raised up to V_{SG}=−5 V. This dependence of noise magnitude on the sidegating voltage seemed to have disappeared when V_{SG} decreased to more than a certain sidegating threshold (V_{SG}=−5 V).

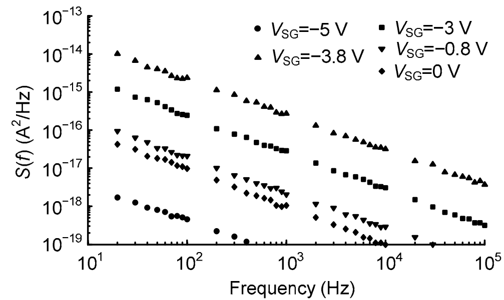

Fig. 3 Channel current spectrum with different sidegating biases

4 Discussion

In this section, two mechanisms are presented to explain the LFN and NLO in channel current with sidegating bias. One argues that the effective substrate resistivity is fully responsible for the LFN and NLO in channel current. The other indicates that the C-S junction modulated by the sidegating bias voltage and DLTs plays an important role in the fluctuations

of channel current. Maybe both of these mechanisms work together, or one of them is the dominant factor. Further research is necessary to discover this.

4.1 Dependence of LFN and NLO on effective substrate resistivity

Considering the GaAs planar MESFET structure that consists of a low-resistivity channel and a substrate, the equivalent circuit of the GaAs MESFET under sidegating bias conditions is as shown in Fig. 4. R_S is the surface leakage resistivity, R_{CS} is the resistivity of the C-S junction, and R_{SUB} is the effective resistivity of the substrate. The sidegating bias will partly drop across the substrate and partly drop across the C-S junction (the voltage is denoted as V_{CS}), because R_{SUB} is series connected with R_{CS}.

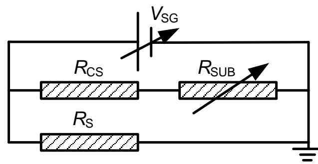

Fig. 4 Equivalent circuit of the test structure used for investigation

Actually, in the sidegating backward biased regime, R_{SUB} is variable with V_{SG}. The behavior of effective substrate resistivity with negative sidegating bias is illustrated in Fig. 5. In experiments, since the ohmic contacts D and SG of Fig. 1b have been undertaken on the substrate, it is easy to realize that at low V_{SUB} values we can measure the resistance of the substrate from the ratio between V_{SUB} and I_{SUB}. At low voltage, R_{SUB} exhibits an omhic characteristic. In general, the typical resistance of substrate is 10^7–10^9 Ω·cm. As a result, R_{SUB} decreases approximately following a linear proportionality to V_{SG} (Region I in Fig. 5).

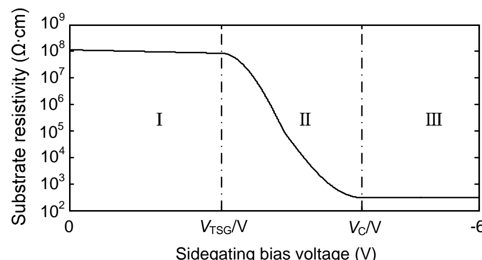

Fig. 5 Behavior of effective substrate resistivity with negative sidegating bias

If we start to increase the voltage V_{SG} negatively (e.g., terminal SG more negative than terminal S) while keeping the same V_{SUB}, the voltage drop between terminals D and SG increases, resulting in the terminal D being more positive than terminal SG. Therefore, the voltage drop along the effective resistivity in the bottom of the substrate also increases. If the voltage along the substrate is just lower than that along the highly-conducting n-channel due to this high conductivity, there will be an equipotential region. Thus, there will be a voltage drop ALONG the C-S junction (e.g., along the n-channel with a gate on top), leading to a different voltage drop ACROSS this C-S junction. This situation leads to the n-channel-substrate junction having a non-uniform bias, in such a way that this p-n junction becomes forward biased on the left and reverse biased on the right. It means that electrons are being injected from the n-channel to the substrate on the left (illustrated as a solid arrow in Fig. 1b) while electrons are extracted from the p-substrate to the n-channel on the right (illustrated as dashed arrows in Fig. 1b). According to Izpura (2008), the forward biased region is shorter than the reverse biased region. In this way, the highly conducting n-type slab that is the channel on top is being put (e.g., connected) in parallel with the effective substrate resistance, and Region II in Fig. 5 appears. Note that the trend is to have both the substrate layer and the n-channel layer conducting in parallel between the D and SG terminals as would happen if we had a layered substrate.

For high V_{SG} values, the highly conducting n-channel becomes 'well connected' in parallel to the effective substrate resistance; since its resistance is several orders of magnitude below the substrate resistance, Region III in Fig. 5 appears. This undoubtedly means that most of the current I_{SUB} now goes along the n-channel, and a very low and stable effective substrate resistance is observed.

These analyses on the effective substrate resistivity are in agreement with the previous reports on negative differential conductivity (NDC) in SI GaAs, which claimed that NDC is due to the intervalley transfer appearing in GaAs under high electric fields (Horio *et al.*, 1988; Reklaitis *et al.*, 1999). NDC of the substrate was used to explain the hysteresis behavior of current with sidegating bias.

Further, we can use the analyses on the behavior

of effective substrate resistivity with negative sidegating bias to explain the experimental results shown in Figs. 2 and 3. From Fig. 2a we can say that, for V_{SG}=−3.8 V the n-channel has a very thin region, thus being very prone to being modulated by any sidegating effect similar to that studied by Izpura (2008). This will explain why NLO is the larger one at this sidegating bias shown in Fig. 2e and especially, why the LNF in Fig. 3 is maximum for this sidegating bias.

The problem, however, is that a further increase of V_{SG} up to V_{SG}=−5 V led to Fig. 2f, which seems to be a totally different or 'new' MESFET, without LNO, and with a saturation current of about 0.48 mA which is approximately half that in Fig. 2b. This would suggest a narrower channel for this new MESFET than for that in Fig. 2b, but if we measure the slope of the I_{DS} at the origin, both are similar, e.g., 4/5 (mA/V), thus suggesting that the channel would be similar in both cases since their dynamic resistance for V_{GS}=0 V and V_{DS}=0 V would be close to 1.125 kΩ.

Due to the above, we can say that the channels controlled by V_{GS} in Figs. 2b and 2f are the same, but in the case of Fig. 2f, this control would be more 'tight' or less 'soft' than in the case of Fig. 2b. To answer this we would study Fig. 3, where the LFN that was maximum for V_{SG}=−3.8 V, dropped by a factor of nearly 10000 when V_{SG} was raised up to −5 V. Following Izpura (2008), it means that the 'bottom floating gate' (which is the substrate) has been 'silenced' by this high V_{SG}=−5 V. Considering Fig. 2b, we can say that this V_{SG} is enough to 'make a good electrical connection' between the V_{SG} terminal and the substrate region NEXT to the C-S junction. In this way, this C-S junction that will be quite 'floating' (thus noisy) for low V_{SG} because the substrate is an SI one, becomes effectively short owing to the low impedance of the V_{SG} generator, which is necessary to avoid the sidegating effect of the thermal noise of this C-S junction, which generates the 1/*f* resistance noise in the n-channel.

4.2 Dependence of channel current fluctuations on DLTs and the C-S junction

Although the exact mechanism of LFN in GaAs MESFET channel current is not fully understood, it is generally accepted that DLTs and the C-S junction play significant roles in GaAs MESFETs characteristics with sidegating bias (Horio *et al.*, 1988; Li *et al.*, 1990; Khuchua *et al.*, 2002; Ding *et al.*, 2005; Gorev *et al.*, 2007). To set up the theoretical model of the behaviors of DLTs and the C-S junction, hypotheses are made that: (1) The channel of MESFET has a uniform doping density and the substrate contains shallow impurity and compensating DLTs; (2) The only generation-recombination process is thermal capture from the conduction band to DLTs and thermal emission from DLTs to the conduction band. If carrier generation and recombination via the deep donor are treated by the SRH statistics (Reklaitis *et al.*, 1999), Poisson's equation can be written as follows:

$$\nabla^2\phi = -\frac{q}{\varepsilon}(p - n + N_{\rm D} - N_{\rm A} + N^{+}_{\rm DLTs}), \qquad (2)$$

where q is the electron charge, ε is the permittivity of the semiconductor, N_D is the shallow donor density, N_A is the shallow acceptor density, and N_{DLTs} is the concentration of vacant DLTs. N^{+}_{DLTs} represents the density of ionized DLTs, and

$$N^{+}_{\rm DLTs} = \frac{e_n}{e_n + c_n n} N_{\rm DLTs}, \qquad (3)$$

$$e_n = \sigma_n v_n N_{\rm C} g^{-1} \exp[(E_{\rm DLPs} - E_{\rm C})/(kT)], \qquad (4)$$

where c_n is the electron capture coefficient of DLTs, e_n is the electron emission rate of DLTs, σ_n is the electron capture cross section of DLTs, v_n is the electron thermal velocity, N_C is the density of the state in the conduction band, and g is the degeneracy factor of DLTs.

The space-charge distribution of the C-S junction resembles a p-n junction with the depletion region located in the doped channel and formed by the charge of ionized donors. If the free carrier charge in the depletion and accumulation regions of the C-S junction and the variation in the trapped charge across the accumulation region are neglected, we can obtain

$$N_{\rm D} w_{\rm ch} = N_{\rm DLTs} w_{\rm sub} = \varepsilon E_{\rm CS}/q, \qquad (5)$$

$$E_{\rm CS}(w_{\rm ch} + w_{\rm sub}) = 2(V_{\rm bcs} + V^{*}_{\rm CS}), \qquad (6)$$

where w_{ch} is the thickness of the depletion region of the C-S junction, w_{sub} is the thickness of its accumulation region, V^{*}_{CS} is the effective voltage across the C-S junction, and V_{bcs} is the built-in voltage of the

C-S junction, which is determined by the difference between the electron densities in the channel and the substrate.

With sidegating bias V_{SG}, effective voltage across the C-S junction consists of two terms. One is the direct contribution of the voltage across the C-S junction (V_{CS}), and the other comes from the indirect contribution of the voltage across the substrate, equal to $V_{SG}-V_{CS}$ (Zhao *et al.*, 2000). Thus, the effective voltage across the C-S junction is

$$V_{CS}^{*}=V_{CS}+\frac{\varepsilon[(V_{SG}-V_{CS})/d]^{2}}{2qN_{DLTs}}, \quad (7)$$

where d represents the effective distance between sidegate and MESFET.

Under an external electric field, expansion of the depletion region of the C-S junction on the substrate side is accompanied by electron capture in DLTs, while contraction of the depletion region is accompanied by electron emission from DLTs to the conduction band. Solving Eq. (6) with Eqs. (5) and (7), the relationship of the thickness of the C-S junction depletion region (w_{ch}) with V_{CS} and V_{SG} can be deduced:

$$\begin{aligned} w_{ch}&=\sqrt{\frac{2\varepsilon N_{DLTs}(V_{CS}^{*}+V_{bcs})}{qN_{D}(N_{D}+N_{DLTs})}} \\ &=\sqrt{\frac{2q\varepsilon N_{DLTs}(V_{CS}+V_{bcs})+[\varepsilon(V_{SG}-V_{CS})/d]^{2}}{q^{2}N_{D}(N_{D}+N_{DLTs})}}. \end{aligned} \quad (8)$$

Consequently, the fluctuations of the channel current caused by V_{CS} and V_{SG} can be approximately expressed as

$$\frac{\Delta I_{DS}}{I_{DS0}}=\frac{I_{DS0}-I_{DS}}{I_{DS0}}=\frac{w_{ch}-w_{ch0}}{h_{0}}, \quad (9)$$

where I_{DS0}, w_{ch0}, and h_0 are I_{DS}, w_{ch}, and the width of the channel under zero sidegating bias, respectively. h_0 can be expressed in terms of the MESFET threshold voltage V_T (Khuchua *et al.*, 2002):

$$h_{0}=\sqrt{\frac{2\varepsilon(V_{b}-V_{T})}{qN_{D}}}-\sqrt{\frac{2\varepsilon V_{b}}{qN_{D}}}, \quad (10)$$

where V_b is the Schottky built-in voltage, and it can be taken as 0.7 V for GaAs.

Combining Eqs. (8)–(10), we can obtain the expression for the fluctuations of channel current caused by V_{CS} and V_{SG} as follows:

$$\frac{\Delta I_{DS}}{I_{DS0}}=k\sqrt{V_{CS}+V_{bcs}+\frac{\varepsilon[(V_{SG}-V_{CS})/d]^{2}}{2qN_{DLTs}}}-k\sqrt{V_{bcs}}, \quad (11)$$

where

$$k=\frac{1}{\sqrt{1+N_{D}/N_{DLTs}}}\frac{1}{\sqrt{V_{b}-V_{T0}}-\sqrt{V_{b}}}. \quad (12)$$

Overall, based on the analyses of the behavior of effective substrate resistivity with negative sidegating bias and the peculiarities of the C-S junction varying with external electric field, we can explain the strong dependency between LFN and NLO in channel current and sidegating bias. Under sidegating bias conditions, the variation of R_{SUB} caused by V_{SG} gives rise to V_{CS} changing correspondingly. The modulation on V_{CS} by the variation in R_{SUB} exerts an influence on the depletion width of the C-S junction, resulting in oscillations of the depletion width. These oscillations have a direct relationship with LFN and NLO in the channel current. Incorporating Eqs. (1) and (11), the relationship between the channel current spectrum and the fluctuations of the channel current can be expressed as

$$\frac{\Delta S(f)}{S_{0}(f)}\propto\frac{\Delta I_{DS}}{I_{DS0}}. \quad (13)$$

In Region I of Fig. 5, V_{CS} is far less than V_{SG}, so Eq. (13) can be simplified as

$$\frac{\Delta S(f)}{S_{0}(f)}\propto k\left(\sqrt{V_{bcs}+\frac{\varepsilon V_{SG}^{2}}{2qd^{2}N_{DLTs}}}-\sqrt{V_{bcs}}\right). \quad (14)$$

In this case, the fluctuations of LFN and NLO are caused mainly by the variation of V_{SG}. As V_{SG} decreases, the oscillations are aggravated, resulting in the amplitude of LFN and NLO in channel current magnifying (Figs. 2b–2d).

In Region II of Fig. 5, with the superlinear decrease of R_{sub}, V_{sub} decreases significantly, causing V_{CS} to increase dramatically with the contraction of the C-S junction depletion region on the channel side (Khuchua *et al.*, 2002). According to Eq. (11), the

fluctuations in I_{DS} will be amplified. Meanwhile, there is some hysteresis in the response of the depletion region expansion of the C-S junction on the variation of external electric field caused by V_{SG} (Ding *et al.*, 2005). These two factors give rise to larger fluctuations of the depletion region thickness in the C-S junction, which strongly modulates the effective width of the FET channel. In consequence, according to Eq. (14), oscillations have a great magnitude (Figs. 2e and 3).

In Region III of Fig. 5, R_{sub} resumes omhic characteristics and gets stable and low resistance. The total resistance is the series resistance of R_{CS} and R_{sub}, so V_{SG} drops mainly across the C-S junction. In this case, V_{CS} can be compared with V_{SG}. Consequently, the modulation on V_{CS} caused by R_{sub} can be negligible. The simplification of Eq. (13) is

$$\frac{\Delta S(f)}{S_0(f)} \propto k\left(\sqrt{V_{SG}+V_{bcs}}-\sqrt{V_{bcs}}\right). \qquad (15)$$

As a result, LFN and NLO in current attenuate sharply, and even disappear (Figs. 2f and 3). Additionally, because the expansion of C-S junction depletion on the channel side greatly reduces the channel width when V_{SG} becomes more negative, the saturation channel current in Fig. 2f declines.

5 Conclusions

Experimental investigations show that LFN and NLO in MESFET channel current exhibit remarkable dependence upon the sidegating bias. Theoretical analysis indicates that the LFN and NLO are directly related with the effective substrate resistivity and the C-S junction, which are modulated by the sidegating bias voltage and DLTs. These conclusions should be of value to elucidate the fundamental nature of the noises modulation in GaAs ICs.

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