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Design of a novel low power 8-transistor 1-bit full adder cell*

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Abstract: An addition is a fundamental arithmetic operation which is used extensively in many very large-scale integration (VLSI) systems such as application-specific digital signal processing (DSP) and microprocessors. An adder determines the overall performance of the circuits in most of those systems. In this paper we propose a novel 1-bit full adder cell which uses only eight transistors. In this design, three multiplexers and one inverter are applied to minimize the transistor count and reduce power consumption. The power dissipation, propagation delay, and power-delay produced using the new design are analyzed and compared with those of other designs using HSPICE simulations. The results show that the proposed adder has both lower power consumption and a lower power-delay product (PDP) value. The low power and low transistor count make the novel 8T full adder cell a candidate for power-efficient applications.

Key words: Full adder design, Low power, CMOS circuit, Very large-scale integration (VLSI)
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1 Introduction

Great attention has been focused on low-power microelectronics due to the rapid development of laptops, portable systems, and cellular networks. Low power consumption has become a major consideration in circuit design (Navi *et al.*, 2009; Wang *et al.*, 2009).

Adders are the core elements of complex arithmetic circuits as they are widely used in arithmetic logic units (ALU), in the floating-point units, and for address generation in the case of cache or memory access (Lee *et al.*, 2007; Xia *et al.*, 2009). Transistor count is an important concern in full adder design because it affects power consumption and area (Lin *et al.*, 2007). The full adder design (28T) in static complementary metal-oxide-semiconductor (CMOS) (Fig. 1), with complementary pull-up P-channel metal-oxide-semiconductor (PMOS) and pull-down N-channel metal-oxide-semiconductor (NMOS) networks, is the most conventional, but it requires as many as 28 transistors (Zimmermann and Fichtner, 1997). The transmission function full-adder (TFA) cell (Zhuang and Wu, 1992) is based on transmission function theory and needs 16 transistors. In the design of Abu-Shama and Bayoumi (1996), the number of transistors is further reduced to only 14 using a lower power XOR design and transmission gates. All of these circuits can operate with full output voltage swing.

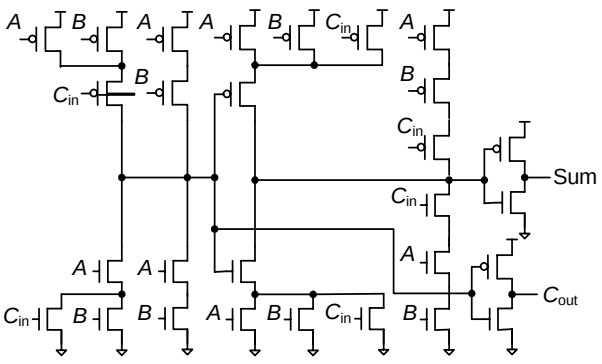

Fig. 1 28-transistor CMOS full adder

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To pursue an even lower transistor count and lower power consumption, pass transistor logic (PTL) can be used. A new full adder called the static energy-recovery full-adder (SERF) uses only 10 transistors and reportedly has the lowest power consumption (Shalem *et al*., 1999). Because of the threshold loss problem in PTL, the output voltage swing of the circuit has a tendency to degrade. In other words, the output high (or low) voltage deviates from the V_{dd} (or ground) by a multiple of the threshold voltage V_T (Lin *et al*., 2007). However, circuits based on PTL are certainly useful in building up larger circuits such as multiple-bit input adders and multipliers (Bui *et al.*, 2002).

In this paper, a new low-power full adder cell using eight transistors is presented, namely an 8T full adder. To demonstrate the efficiency of the new design, we compare some general characteristics of the new design, such as power consumption, against another five full adder cells.

2 Previous works

In this section, several different designs of low power and high speed adders are introduced. SERF (Fig. 2a) is claimed to be an extremely low power adder because it does not contain a direct path to the ground and can re-apply the load charge to the control gate (energy recovery) (Shalem *et al.*, 1999). Bui *et al.* (2002) proposed 41 different full adder designs based on a systematic combination approach using several XOR/XNOR and multiplexer modules. The designs (denoted 9A and 13A in Figs. 2b and 2c) have the best performance in those circuits. Another design (Fig. 2d), denoted CLRCL (complementary and level restoring carry logic), features a lower operating voltage, higher computing speed, and lower energy operation. The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss problem (Lin *et al*., 2007).

Chowdhury *et al.* (2008) proposed an eight-transistor full adder based on a new three-transistor XOR (Fig. 3). In spite of claims of superior delay in this circuit, the design suffers from a logic fault in the output C_{out}. For example, when the inputs A and B are both at low logic, the pass transistors M7 and M8 are all disabled and C_{out} is at high impedance.

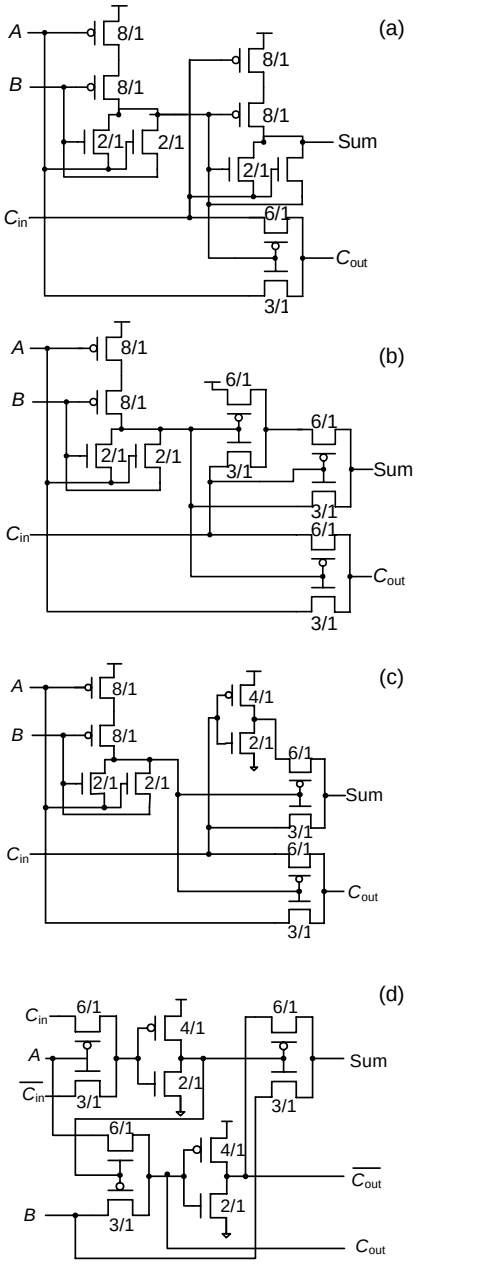

Fig. 2 10T full adder designs
(a) SERF full adder design; (b) 9A full adder design; (c) 13A full adder design; (d) CLRCL full adder design

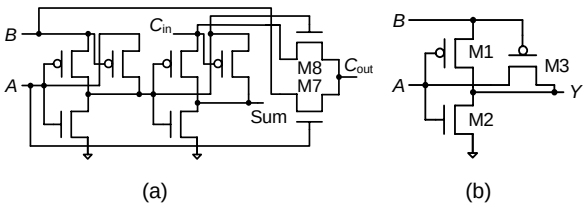

Fig. 3 Design of Chowdhury *et al.* (2008)
(a) 8T full adder; (b) 3T XOR gate

3 The proposed full adder design

The full adder function can be described as follows: the addition of two 1-bit inputs A and B with forestage carry C_{in} calculates the two 1-bit outputs Sum and C_{out}, where

$$\text{Sum}=A\oplus B\oplus C_{in}, \quad (1)$$

$$C_{out}=A\cdot B+C_{in}\cdot(A\oplus B). \quad (2)$$

In our design, we rewrite the Boolean function as

$$\text{Sum}=(A\oplus C_{in})\cdot\overline{C_{out}}+\overline{A\oplus C_{in}}\cdot B, \quad (3)$$

$$C_{out}=(A\oplus C_{in})\cdot B+\overline{A\oplus C_{in}}\cdot A. \quad (4)$$

From Eqs. (3) and (4), the 8T design is proposed (Fig. 4).

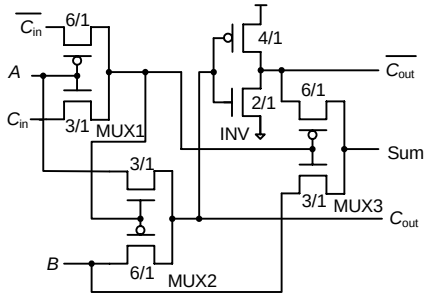

Fig. 4 The proposed 8-transistor full adder (8T)

The entire design process can be divided into several steps as follows:

1. $\overline{A\oplus C_{in}}$ (or $A\oplus C_{in}$) is needed as a control signal in multiplexers MUX2 and MUX3 to generate C_{out} and Sum. In this study, $\overline{A\oplus C_{in}}$ is implemented by MUX1 (Fig. 4).

2. The multiplexer circuit MUX2 is adopted in our proposed design to generate C_{out} followed by an inverter INV. The inverter has three advantages for the circuit: firstly, it speeds up the carry propagation as a buffer along the carry chain. Secondly, it provides complementary signals needed for the generation of Sum. Thirdly, the inverter can improve the output voltage swing as a level restoring circuit (Lin *et al*., 2007).

3. The Sum is generated by the multiplexer MUX3 passing either B or $\overline{C_{out}}$ according to the value of $\overline{A\oplus C_{in}}$.

The proposed full adder circuit, which uses three multiplexers and an inverter, requires eight transistors. Choosing appropriate width to length rates of transistors, W/L, improves the threshold drop of the circuit (Chowdhury *et al.*, 2008). The multiplexer uses transistor sizes of $(W/L)_p$=6/1 and $(W/L)_n$=3/1 for PMOS and NMOS, respectively, while the inverter uses the typical sizes of $(W/L)_p$=4/1 and $(W/L)_n$=2/1 (Fig. 4).

4 Simulation results

To test the performance of the proposed full adders, detailed comparisons were performed. The 10T full adder designs mentioned in Fig. 2 and 28T were included for comparison with the proposed design.

All the schematics are based on TSMC 180 nm technology with a 1.8 V supply voltage, and were simulated using HSPICE. In our simulation, the power consumption of these designs was examined at different input frequencies. Table 1 shows the power measurement for frequencies from 100 to 500 MHz when the output load was 100 fF. From the results of simulation, the 8T full adder had the best performance in all conditions. Compared with the other designs, it consumed 7.2%–37.3% less power.

Table 1 Comparison of power consumption at different frequencies from 100 to 500 MHz with a load of 100 fF

Full adder cell	Power consumption (μW)				
	100	150	200	300	500
28T	52.41	74.81	104.40	140.20	202.80
SERF	43.44	61.07	84.30	123.60	176.10
9A	40.37	56.26	77.40	114.10	152.30
13A	40.42	56.46	76.99	109.40	143.60
CLRCL	42.19	58.31	78.18	106.10	137.20
8T (this work)	36.47	50.92	67.63	98.52	127.10

Propagation delay is the time between the fastest input signal and the output signal. The worst case delay, i.e., the longest delay in all input combinations, was measured under five loading conditions varying from 50 to 250 fF with a 200 MHz frequency. From the results (Table 2), we can conclude that the delay of 8T was somewhat poorer than that of 28T but better than that of the other designs.

Table 2 Comparison of delay at different output loads from 50 to 250 fF with a frequency of 200 MHz

Full adder cell	Delay (ns)				
	50	100	150	200	250
28T	0.223	0.366	0.531	0.681	0.820
SERF	0.482	0.765	1.057	1.243	1.431
9A	0.310	0.519	0.755	0.969	1.189
13A	0.408	0.639	0.790	0.990	1.229
CLRCL	0.385	0.642	0.877	1.134	1.364
8T (this work)	0.265	0.496	0.728	0.957	1.117

Furthermore, the power-delay product (PDP) for various loads was computed (Fig. 5) under the same conditions as the delay simulation. The 8T showed better performance than the other adders due to its low power consumption.

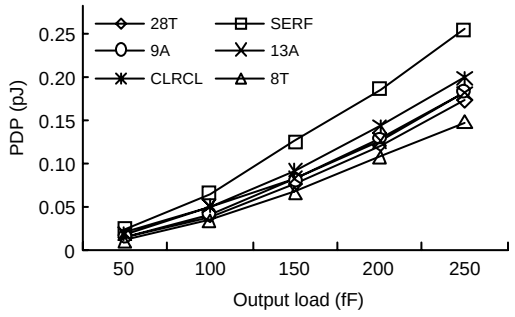

Fig. 5 Power-delay product (PDP) at different output loads for various full adder designs (frequency: 200 MHz)

From this comparison of different designs, the proposed 8T full adder appears to be a good candidate for building large circuits, such as multipliers, with low power consumption. Moreover, the area of these systems can be reduced because of the small area of this adder.

5 Conclusions

The performance of digital VLSI applications depends largely on the characteristics of the full adder circuits employed in such systems. The novel full adder design proposed is composed of only eight transistors forming three multiplexers and one inverter to produce complementary carry signals (C_{out} and $\overline{C_{out}}$) and summation signal (Sum). Comparing the proposed design with other existing adders in respect of power consumption, delay, and power-delay product, the new design embodies a good many advantages. In future work, the proposed design will be embedded into ripple-carry adders and the multiplier to demonstrate the performance in realistic applications.

References

Abu-Shama, E., Bayoumi, M., 1996. A New Cell for Low Power Adders. IEEE Int. Symp. on Circuits and Systems, p.49-52. [doi:10.1109/iscas.1996.541898]

Bui, H.T., Wang, Y., Jiang, Y.T., 2002. Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates. *IEEE Trans. Circ. Syst. II*, **49**(1):25-30. [doi:10.1109/82.996055]

Chowdhury, S.R., Banerjee, A., Roy, A., Saha, H., 2008. A high speed 8 transistor full adder design using novel 3 transistor XOR gates. *Int. J. Electron. Circ. Syst.*, **2**(4): 217-223.

Lee, P.M., Hsu, C.H., Hung, Y.H., 2007. Novel 10-T Full Adders Realized by GDI Structure. Int. Symp. on Integrated Circuits, p.115-118. [doi:10.1109/ISICIR.2007.4441810]

Lin, J.F., Hwang, Y.T., Sheu, M.H., Ho, C.C., 2007. A novel high-speed and energy efficient 10-transistor full adder design. *IEEE Trans. Circ. Syst. I*, **54**(5):1050-1059. [doi:10.1109/TCSI.2007.895509]

Navi, K., Moaiyeri, M.H., Mirzaee, R.F., Hashemipour, O., Nezhad, B.M., 2009. Two new low-power full adders based on majority-not gates. *Microelectron. J.*, **40**(1): 126-130. [doi:10.1016/j.mejo.2008.08.020]

Shalem, R., John, E., John, L.K., 1999. A Novel Low Power Energy Recovery Full Adder Cell. Proc. 9th Great Lakes Symp. on VLSI, p.380-383. [doi:10.1109/GLSV.1999.757461]

Wang, D., Yang, M.F., Cheng, W., Guan, X.G., Zhu, Z.M., Yang, Y.T., 2009. Novel Low Power Full Adder Cells in 180nm CMOS Technology. 4th IEEE Conf. on Industrial Electronics and Applications, p.430-433. [doi:10.1109/ICIEA.2009.5138242]

Xia, B.J., Liu, P., Yao, Q.D., 2009. New method for high performance multiply-accumulator design. *J. Zhejiang Univ.-Sci. A*, **10**(7):1067-1074. [doi:10.1631/jzus.A0820566]

Zhuang, N., Wu, H.M., 1992. A new design of the CMOS full adder. *IEEE J. Sol.-State Circ.*, **27**(5):840-844. [doi:10.1109/4.133177]

Zimmermann, R., Fichtner, W., 1997. Low-power logic styles: CMOS versus pass-transistor logic. *IEEE J. Sol.-State Circ.*, **32**(7):1079-1090. [doi:10.1109/4.597298]