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A low drift curvature-compensated bandgap reference with trimming resistive circuit*

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Abstract: A low temperature drift curvature-compensated complementary metal oxide semiconductor (CMOS) bandgap reference is proposed. A dual-differential-pair amplifier was employed to add compensation with a high-order term of $T\ln T$ (T is the thermodynamic temperature) to the traditional 1st-order compensated bandgap. To reduce the offset of the amplifier and noise of the bandgap reference, input differential metal oxide semiconductor field-effect transistors (MOSFETs) of large size were used in the amplifier and to keep a low quiescent current, these MOSFETs all work in weak inversion. The voltage reference's temperature curvature has been further corrected by trimming a switched resistor network. The circuit delivers an output voltage of 3 V with a low dropout regulator (LDO). The chip was fabricated in Taiwan Semiconductor Manufacturing Company (TSMC)'s 0.35-μm CMOS process, and the temperature coefficient (TC) was measured to be only 2.1×10^{-6}/°C over the temperature range of −40–125 °C after trimming. The power supply rejection (PSR) was −100 dB @ DC and the noise was 42 μV (rms) from 0.1 to 10 Hz.

Key words: Voltage reference, Bandgap, Temperature compensation, Low drift, Resistive trimming
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1 Introduction

Voltage reference is widely used in many electronic devices, such as power converters, data converters, and radio frequency (RF) circuits (Ka *et al*., 2003; Atrash and Aude, 2004; Spady and Ivanov, 2005; Ruzza *et al*., 2008). In particular, 12-bit and higher resolution digital to analog circuits (DACs) and analog to digital circuits (ADCs) require higher precision voltage reference. To achieve true accuracy, these devices require a voltage reference with less than 1 LSB error over their operating temperature range (1 LSB is 240×10^{-6} for a 12-bit system or 15×10^{-6} for a 16-bit system). The temperature coefficient (TC) of traditional 1st-order compensated bandgap or zener voltage reference may have up to 0.02 of the absolute value error without trimming and 0.002 with trimming over the temperature range of −40–125 °C (Spady and Ivanov, 2005).

To reduce the temperature drift of voltage references, a resistor ratio between a high sheet resistivity poly-silicon resistor and a diffused resistor can be used to provide high-order compensation. However, the temperature characteristic of resistors varies a lot due to process variation. It is rarely possible to hold the value of TC to tolerances of better than $\pm250\times10^{-6}$/°C for a poly resistor (Alan, 2006). Thus, complex trimming is necessary to obtain a high precision reference for this design, which needs six temperature measurements during one trimming operation (Ka *et al*., 2003). Atrash and Aude (2004) and Ruzza *et al*. (2008) used switching techniques to reduce offsets in the amplifier and current source devices. However, voltage references stated above are only 1st-order compensated and their drift is still larger than 10×10^{-6}/°C. Malcovati *et al*. (2001) used a V_{EB} (emitter to base voltage of bipolar) linearization technique to compensate high-order terms of bandgap

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reference with current mode structure. References of this technique require that their 1st- and high-order coefficients should be trimmed separately. Also, voltage references based on the threshold voltage of metal oxide semiconductor field-effect transistors (MOSFETs) have been proposed (Filanovsky *et al*., 2009; Ueno *et al*., 2009). However, among various device parameters in semiconductor technologies, the characteristics of bipolar transistors have proven to be the most reproducible and well-defined quantities that can provide positive and negative TCs (Behzad, 2005). Therefore, bipolar operation still forms the core of voltage references.

Moreover, to minimize temperature drift, voltage reference also needs to be trimmed. Brito *et al*. (2007) and Ekekwe and Etienne-Cummings (2008) have trimmed proportion-to-absolute-temperature (PTAT) current to reduce the temperature drift of references, whereas the trimming circuits would result in more power consumption. Spilka *et al*. (2007) and Ge *et al*. (2010) trimmed resistors by using MOSFET-switches. However, the MOSFET-switch has a turn-on resistance R_{on}, which may affect the linearity of trimming. An approach of reducing the switches' effect is to enlarge the size of MOSFETs to reduce R_{on}, but a larger size MOSFET would occupy more chip area.

This paper proposes a new structure of bandgap reference. Compensation with a high-order term of $T\ln T$ (T is the thermodynamic temperature) is added to the traditional 1st-order compensated bandgap reference to reduce temperature drift. Trimming with a switched resistor network has also been used, and negative channel metal oxide semiconductor field-effect transistor (NMOSFET) pairs are adopted to eliminate the effect of MOSFET-switches' R_{on} on trimming's linearity.

2 The proposed curvature-compensated bandgap reference

Fig. 1 shows the circuits of the proposed bandgap reference, which contains four parts: bias, bandgap core, low dropout regulator (LDO), and curvature compensation circuit. The bandgap core produces PTAT currents I_1 and I_2 which flow through bipolars Q_1 and Q_2, respectively, while the curvature compensation circuit produces a complementary-to-absolute-temperature (CTAT) current I_3 which flows through bipolar Q_3. Therefore, the differential value of emitter-base voltage between Q_1 and Q_3 is a high-order term associated with temperature, which has been added to the traditional 1st-order temperature compensated bandgap by a dual-differential-pair amplifier (dual_op in Fig. 1) in the bandgap core. An LDO is also integrated for driving ability and produces a stable supply for the curvature compensation circuit.

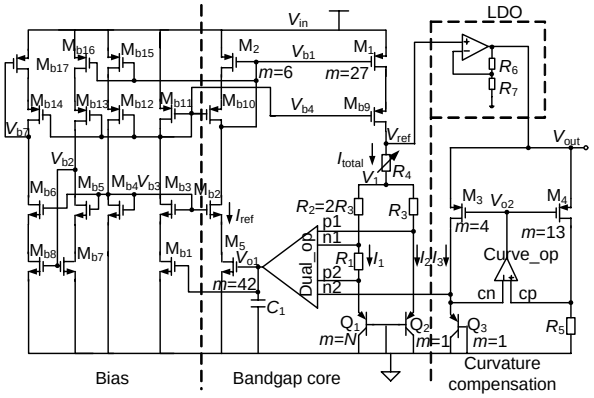

Fig. 1 The proposed bandgap reference

V_{in}: input voltage of the circuit; V_{out}: output voltage of the LDO; V_{o1}: output voltage of dual_op; V_{o2}: output voltage of curve_op; V_{bi}: bias voltage; V_{ref}: bandgap reference voltage; V_1: node voltage between R_3 and R_4; R_i: resistor; I_{ref}: bias current; Q_i: bipolar; I_1–I_3: emitter currents of Q_1–Q_3, respectively; I_{total}: summary current of I_1 and I_2; M_i: MOSFET in bandgap core and curvature compensation; M_{bi}: MOSFET in bias; C_1: output capacitor of dual_op; m: number of the corresponding devices; curve_op: amplifier for curvature compensation; cn and cp: negative and positive inputs of curve_op, respectively

The structure of the dual_op is shown in Fig. 2. To reduce the offset of the amplifier and 1/f noise of the voltage reference, size of the input differential transistors should be very large (Vishal, 2007), and to keep a low quiescent current, input differential MOSFETs should all work in the weak inversion region. When the drain to source voltage V_{DS}>200 mV, the drain current of the positive channel metal oxide semiconductor field-effect transistor (PMOSFET) in weak inversion can be given as (Behzad, 2005)

$$I_{DS}=\frac{W}{L}I_0\exp\left(\frac{V_{SG}}{\xi V_T}\right)=\frac{W}{L}I_0 e^{n\cdot V_{SG}}, \qquad (1)$$

where ξ is determined by the process and usually

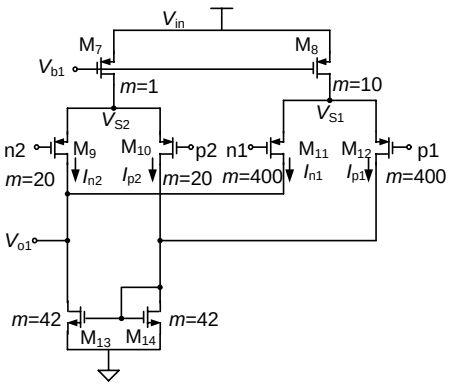

Fig. 2 Structure of dual_op

$1<\xi<3$, V_T is the thermal voltage, $n=1/(\xi V_T)$, I_0 is the drain current of the unity PMOSFET when the source to gate voltage $V_{SG}=0$, and W/L is the width to length ratio. Thus, the drain currents of MOSFETs M_9–M_{12} can be expressed as

$$I_{n1}=400I_0\left(\frac{W}{L}\right)e^{n\cdot V_{SG,n1}}, \tag{2}$$

$$I_{p1}=400I_0\left(\frac{W}{L}\right)e^{n\cdot V_{SG,p1}}, \tag{3}$$

$$I_{n2}=20I_0\left(\frac{W}{L}\right)e^{n\cdot V_{SG,n2}}, \tag{4}$$

$$I_{p2}=20I_0\left(\frac{W}{L}\right)e^{n\cdot V_{SG,p2}}, \tag{5}$$

where n1, n2, p1, and p2 are the four input nodes of the dual-op, and $V_{SG,i}$ is the source to gate voltage of the corresponding MOSFET. Because the ratio of the two differential pairs' tail current is 10, we can obtain

$$I_{n1}+I_{p1}=10(I_{n2}+I_{p2}). \tag{6}$$

M_{13} and M_{14} constitute a current mirror. When the op-amp is balanced, we can obtain

$$I_{n1}+I_{n2}=I_{p1}+I_{p2}. \tag{7}$$

Substitution of Eqs. (2)–(5) into Eqs. (6) and (7) gives

$$400e^{n\cdot V_{SG,n1}}+400e^{n\cdot V_{SG,p1}}=10(20e^{n\cdot V_{SG,n2}}+20e^{n\cdot V_{SG,p2}}), \tag{8}$$

$$400e^{n\cdot V_{SG,n1}}+20e^{n\cdot V_{SG,n2}}=400e^{n\cdot V_{SG,p1}}+20e^{n\cdot V_{SG,p2}}. \tag{9}$$

Because $V_{SG,i}=V_{S,i}-V_{G,i}$, where $V_{S,i}$ and $V_{G,i}$ are the source voltage and gate voltage of the corresponding MOSFET, respectively, Eqs. (8) and (9) can be rearranged as

$$\frac{2e^{-n\cdot V_{G,n1}}+2e^{-n\cdot V_{G,p1}}}{e^{-n\cdot V_{G,n2}}+e^{-n\cdot V_{G,p2}}}=\frac{e^{n\cdot V_{S2}}}{e^{n\cdot V_{S1}}}, \tag{10}$$

$$20\cdot\frac{e^{-n\cdot V_{G,n1}}-e^{-n\cdot V_{G,p1}}}{e^{-n\cdot V_{G,p2}}-e^{-n\cdot V_{G,n2}}}=\frac{e^{n\cdot V_{S2}}}{e^{n\cdot V_{S1}}}, \tag{11}$$

where V_{S1} and V_{S2} are the source voltages shown in Fig. 2. The use of Eqs. (10) and (11) gives

$$\begin{aligned}&11e^{-n\cdot V_{G,n1}}e^{-n\cdot V_{G,n2}}+9e^{-n\cdot V_{G,n1}}e^{-n\cdot V_{G,p2}}\\&=9e^{-n\cdot V_{G,p1}}e^{-n\cdot V_{G,n2}}+11e^{-n\cdot V_{G,p1}}e^{-n\cdot V_{G,p2}}.\end{aligned} \tag{12}$$

From Fig. 1, we can obtain

$$V_{G,n1}=V_{EB1}+I_1R_1, \tag{13}$$

$$V_{G,p1}=V_{EB2}, \tag{14}$$

$$V_{G,n2}=V_{EB3}, \tag{15}$$

$$V_{G,p2}=V_{EB1}, \tag{16}$$

where V_{EBi} is the emitter-base voltage of Q_i, and substitution of Eqs. (13)–(16) into Eq. (12) results in

$$\begin{aligned}&e^{-n\cdot(V_{EB1}+I_1\cdot R_1)}(11e^{-n\cdot V_{EB3}}+9e^{-n\cdot V_{EB1}})\\&=e^{-n\cdot V_{EB2}}(9e^{-n\cdot V_{EB3}}+11e^{-n\cdot V_{EB1}}).\end{aligned} \tag{17}$$

Solving Eq. (17) for I_1 gives

$$\begin{aligned}I_1&=\frac{1}{R_1}\left[(V_{EB2}-V_{EB1})+\frac{1}{n}\ln\frac{11e^{-n\cdot V_{EB3}}+9e^{-n\cdot V_{EB1}}}{9e^{-n\cdot V_{EB3}}+11e^{-n\cdot V_{EB1}}}\right]\\&=\frac{1}{R_1}\left[(V_{EB2}-V_{EB1})+\frac{y}{n}\right],\end{aligned} \tag{18}$$

where

$$\begin{aligned}y&=\ln\frac{11e^{-n\cdot V_{EB3}}+9e^{-n\cdot V_{EB1}}}{9e^{-n\cdot V_{EB3}}+11e^{-n\cdot V_{EB1}}}\\&=\ln\left[\frac{11}{9}-\frac{40}{99}\times\frac{1}{1+\frac{9}{11}e^{n\cdot(V_{EB1}-V_{EB3})}}\right].\end{aligned} \tag{19}$$

Through inspection of the circuit in Fig. 1, we can obtain the node voltage

$$\begin{aligned} V_1 &= V_{\mathrm{EB1}} + I_1(R_1 + R_2) \\ &= V_{\mathrm{EB1}} + \left(1 + \frac{R_2}{R_1}\right)\left[(V_{\mathrm{EB2}} - V_{\mathrm{EB1}}) + \frac{y}{n}\right]. \end{aligned} \tag{20}$$

Since R_2=2R_3 (Fig. 1), Eq. (20) can be rewritten as

$$V_1 = V_{\mathrm{EB1}} + \left(1 + \frac{2R_3}{R_1}\right)\left[(V_{\mathrm{EB2}} - V_{\mathrm{EB1}}) + \frac{y}{n}\right]. \tag{21}$$

Using Eq. (21), we can obtain

$$I_2 = \frac{V_1 - V_{\mathrm{EB2}}}{R_3} = \frac{2}{R_1}(V_{\mathrm{EB2}} - V_{\mathrm{EB1}}) + \left(\frac{1}{R_3} + \frac{2}{R_1}\right)\frac{y}{n}. \tag{22}$$

Then, the summary current of I_1 and I_2 can be given as

$$I_{\mathrm{total}} = I_1 + I_2 = \frac{3}{R_1}(V_{\mathrm{EB2}} - V_{\mathrm{EB1}}) + \left(\frac{3}{R_1} + \frac{1}{R_3}\right)\frac{y}{n}. \tag{23}$$

Using Eqs. (21) and (23), the reference voltage V_{ref} can be written as

$$\begin{aligned} V_{\mathrm{ref}} &= V_1 + I_{\mathrm{total}}R_4 \\ &= V_{\mathrm{EB1}} + \left(1 + \frac{2R_3 + 3R_4}{R_1}\right)(V_{\mathrm{EB2}} - V_{\mathrm{EB1}}) \\ &\quad + \left(1 + \frac{2R_3 + 3R_4}{R_1} + \frac{R_4}{R_3}\right)\frac{y}{n}. \end{aligned} \tag{24}$$

Besides, we know that the emitter-base voltage of the bipolar transistor versus temperature is (Gray *et al*., 2003)

$$\begin{aligned} V_{\mathrm{EB}}(T) &= V_{\mathrm{G0}} + \frac{T}{T_r}\left[V_{\mathrm{EB}}(T_r) - V_{\mathrm{G0}}\right] \\ &\quad - (\gamma - \alpha)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right), \end{aligned} \tag{25}$$

where V_{G0} is the bandgap voltage of silicon extrapolated to 0 K, T_{r} is a reference temperature, generally 323 K, $V_{\mathrm{EB}}(T_{\mathrm{r}})$ is the emitter-base voltage when T=T_{r}, γ is a constant parameter related to the process, α is determined by the TC of the collector current I_{C} of the bipolar transistor (Gray *et al*., 2003), k is Boltzmann's constant, and q is electron charge. Eq. (25) shows that the emitter-base voltage V_{EB} contains one 1st-order term and one high-order term of $T\ln T$ both related to temperature.

The multiplier ratio of Q_1, Q_2, and Q_3 is N:1:1, the current I_1 is set to be N times of I_3 at the temperature of T_{r}, and thus V_{EB3} equals V_{EB1} at the temperature of T_{r}. Simulation results show that the difference between V_{EB1} and V_{EB3} is no more than 10 mV over a temperature range of −40–125 °C. Consequently, we can consider V_{EB1}≈V_{EB3} in that temperature range. Then, y≈ln1=0, and currents I_1 and I_2 can be treated as PTAT currents. Thus,

$$V_{\mathrm{EB2}} - V_{\mathrm{EB1}} = \frac{kT}{q}\ln(2N). \tag{26}$$

Setting x=n(V_{EB1}−V_{EB3}), from Eq. (25) we can obtain

$$\begin{aligned} x &= n(V_{\mathrm{EB1}} - V_{\mathrm{EB3}}) \\ &= n(\alpha_1 - \alpha_3)T\ln T = n\zeta T\ln T, \end{aligned} \tag{27}$$

where ζ is determined by the TC of both Q_1 and Q_3's collector currents. Since V_{EB3} equals V_{EB1} at the temperature of T_{r}, the linear terms of V_{EB1} and V_{EB3} are equal, and then the linear term in Eq. (27) is eliminated. Here, I_{C1} (I_{C1}≈I_1) is a PTAT current, while I_{C3} produced by the curvature compensation circuit, I_{C3}≈I_3=V_{EB3}/R_5, is a CTAT current, so ζ is a positive value. The difference between V_{EB1} and V_{EB3} is very small, so x→0. Eq. (19) can be Taylor expanded at x=0, and the first two terms are preserved:

$$y \approx y|_{x=0} + y'|_{x=0}\, x = \frac{x}{10}. \tag{28}$$

Substitution of Eqs. (27) and (28) in Eq. (24) gives

$$\begin{aligned} V_{\mathrm{ref}} &= V_{\mathrm{EB1}} + \left(1 + \frac{2R_3 + 3R_4}{R_1}\right)(V_{\mathrm{EB2}} - V_{\mathrm{EB1}}) + \left(1 + \frac{R_4}{R_3}\right. \\ &\quad \left. + \frac{2R_3 + 3R_4}{R_1}\right)\frac{\zeta T\ln T}{10} = V_{\mathrm{EB1}} + aT + bT\ln T, \end{aligned} \tag{29}$$

where

$$a=\left(1+\frac{2R_3+3R_4}{R_1}\right)\frac{k}{q}\ln(2N), \tag{30}$$

$$b=\frac{1}{10}\left(1+\frac{2R_3+3R_4}{R_1}+\frac{R_4}{R_3}\right)\zeta. \tag{31}$$

Since aT and $bT\ln T$ can be used to eliminate the 1st-order term and high-order terms of V_{EB1}, respectively, V_{ref} is a well temperature-compensated bandgap reference. Here, R_1–R_5 are all poly-type resistors for high precision and are designed by a ratio of 10:34:17:3:56. Fig. 3 gives the structure of amplifier curve_op. Capacitor C_2 in Fig. 3 is placed between the gate of M_{22} and node V_{o2}, which can enhance the power supply rejection (PSR) in high frequency and produce a low dominant pole to improve the phase margin of the loop.

We add an LDO, as shown in Fig. 4, as a driver of V_{ref} which can also provide a stable supply of 3 V for curvature compensation circuit. The LDO has a class AB minimal delay output stage, which causes it to provide a load current of −20–20 mA. Fig. 5 is the bias circuit for the LDO, which makes LDO's quiescent current steady under different temperatures and process corners. The LDO is stable for any load capacitor and its structure is similar to Ivanov and Spady (2005)'s. The output voltage V_{out} of the LDO can be described as

$$V_{out}=\frac{R_6+R_7}{R_7}V_{ref}. \tag{32}$$

Fig. 6 gives the simulated curvature of V_{out} versus temperature, which shows that the reference has a low temperature drift of only 3.2×10^{-6}/°C over the temperature range of −40–125 °C.

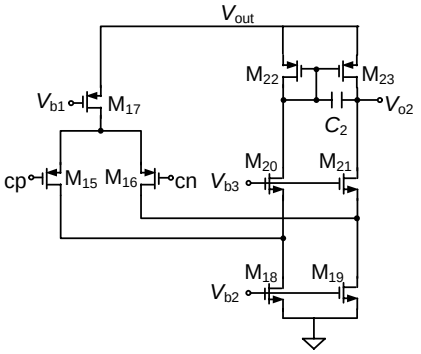

Fig. 3 Structure of the amplifier curve_op

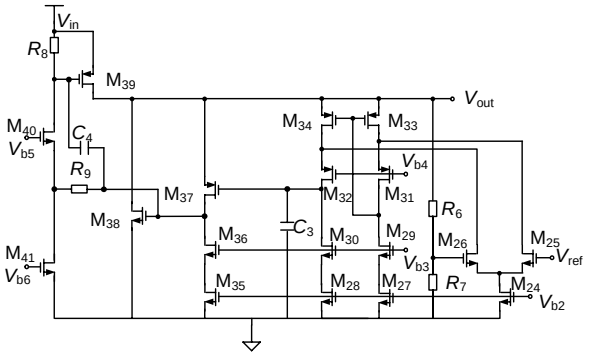

Fig. 4 Structure of the low dropout regulator (LDO)

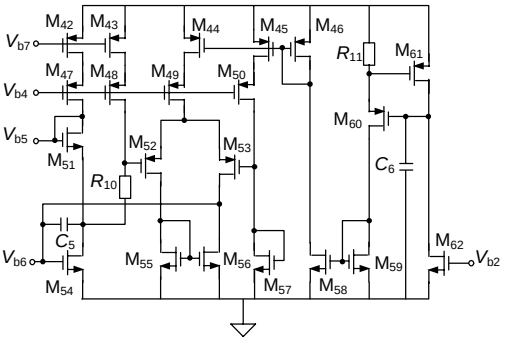

Fig. 5 Bias circuit for the low dropout regulator (LDO)

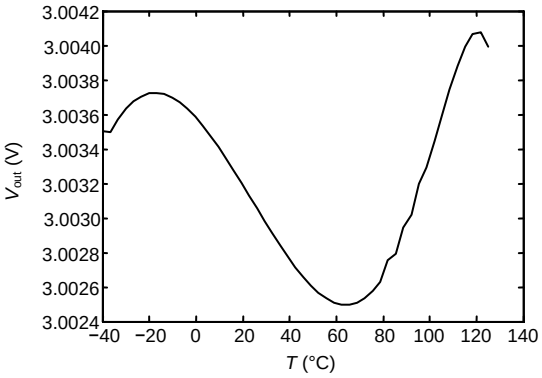

Fig. 6 Relationship between V_{out} and temperature

Fig. 7 presents the startup circuit of this design. Comp1 is a comparator with an offset of approximately 300 mV. At the beginning of startup, $V_{G,p2}$ and V_{ref} both equal zero and the logic makes M_{71}–M_{75} turn on to charge nodes V_{ref}, V_{S1}, and V_{b3}. After the bandgap core has started up, V_{ref} would get a voltage level which is 300 mV larger than $V_{G,p2}$. Then the logic is reversed, which makes M_{70}–M_{71} turn off, and startup is completed.

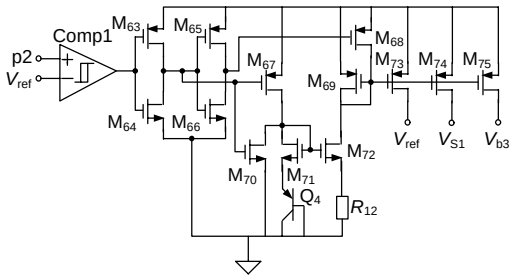

Fig. 7 Startup circuit

3 Trimming

Trimming is necessary in voltage reference design, because the mismatch of devices, amplifier's offset, and process variations would deteriorate its TC property. Eq. (29) shows that trimming R_1 and/or R_4 can be used to modify the 1st-order and high-order coefficients of the voltage reference simultaneously. However, variation of R_1 would change the PTAT current, so trimming R_4 is a better choice to correct the reference's curvature.

Fig. 8 shows the structure of a trimming circuit for R_4, which is a switched resistor network. Monte Carlo simulation was performed to obtain the TC correction range of the trimming circuit and 8-bit trimming can meet the accuracy of TC in our design. Here, every switch is constituted by an inverter and a pair of NMOSFETs. M_{ia} and M_{ib} in each NMOSFET pair are of the same size and placed together in the layout; therefore, they have the same turn-on resistance of $R_{on(i)}$. Then R_4 can be expressed as

$$R_4 = \sum_{i=0}^{7} (\sim \text{bit}i) \cdot 2^i \cdot R + \sum_{i=0}^{7} R_{on(i)}, \qquad (33)$$

where ~bit$i$ is the inverted value of the digital signal bit$i$, and R is a unit resistance. Since $\sum_{i=0}^{7} R_{on(i)}$ is a constant offset of R_4, the variation of R_4 is linear to the digital signals bit7–bit0. The current I_{total} flowing through R_4 is almost a PTAT current, and thus the TC of V_{ref} varies linearly to R_4. Therefore, the TC of V_{ref} varies linearly to the digital signals bit7–bit0. Simulation results show that trimming R_4 with an 8-bit digital signal can provide the TC correction in a range of $\pm 240\times10^{-6}$/°C for the voltage reference, and the accuracy is 1.88×10^{-6}/°C. Here, $\sum_{i=0}^{7} R_{on(i)}$ is associated with temperature, and simulation results show that its effect may cause a total error of 7×10^{-6}/°C to the reference's TC, when the dimension of each NMOSFET is 100 μm/500 nm. However, the error of 7×10^{-6}/°C is a constant TC error, which can also be corrected by the trimming circuit. Therefore, this switched resistor network is suitable for bandgap reference correction.

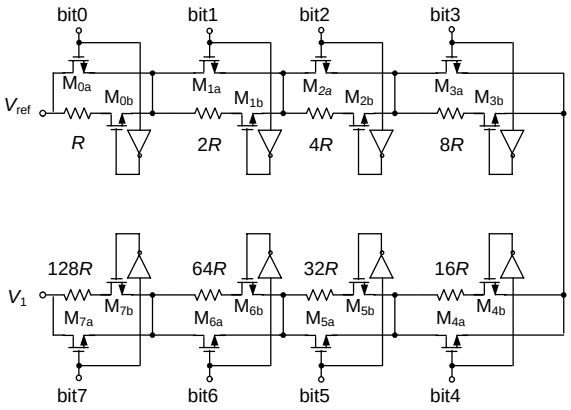

Fig. 8 Trimming circuit

M_{ia}: NMOSFET controlled by bit$i$ signal; M_{ib}: NMOSFET controlled by ~bit$i$ signal

During the trimming procedure, we measure the output of the chip over the temperature of −40–125 °C when bit7–bit0 are set 00000000 and 11111111, and calculate the TC separately, and then the trimming bits, which bit7–bit0 should be set, can be given by

$$\text{bit7}-\text{bit0}=256\times\frac{\left|\text{TC}_{00000000}\right|}{\left|\text{TC}_{00000000}\right|+\left|\text{TC}_{11111111}\right|}. \qquad (34)$$

4 Measurement results

The proposed voltage reference has been fabricated in Taiwan Semiconductor Manufacturing Company (TSMC)'s 0.35-μm complementary metal oxide semiconductor (CMOS) process. The chip microphotograph is shown in Fig. 9. Measurement results show that it generates a reference voltage of approximately 3 V with a variation of 1.4 mV at room

temperature, when the supply voltage varies from 3.05 to 5 V (Fig. 10). When V_{in}=4 V, a ripple of 200 mV is added to V_{in} to test the PSR of the voltage reference. The PSR versus frequency is shown in Fig. 11, which reveals that PSR is −100 dB @ DC and −50 dB @ 1 kHz. Fig. 12 presents the load regulation of the LDO, which is about 7.5×10^{-6}/mA over the range of −20–20 mA. The integrated noise of this reference is 42 μV (rms) over the frequency of 0.1 to 10 Hz and the quiescent current is 120 μA.

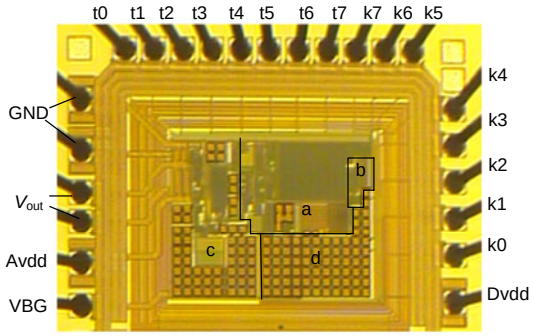

Fig. 9 Chip microphotograph

a: BGR; b: trimming circuits; c: LDO; d: capacitor. t0–t7: pads of TC trimming bits; k0–k7: pads of LDO's trimming bits; Avdd: pad of analog supply; Dvdd: pad of digital supply; V_{out}: pads of LDO's output; VBG: pad of BGR; GND: pads of ground

We calculate the trimming bits by testing $TC_{00000000}$ and $TC_{11111111}$ of one chip from the multi-project wafer (MPW) over the temperature of −40–125 °C, set the trimming bits to all the chips from different areas of the same MPW wafer, and then measure the temperature drift of all the chips. Twenty-eight chips are tested and the smallest drift of these chips is only 2.1×10^{-6}/°C. Measurement results are shown in Fig. 13a. All the chips' drift is smaller than 25×10^{-6}/°C and chips of $(5–10)\times10^{-6}$/°C are in the majority. To achieve a more precise voltage reference, each chip can be trimmed separately with a distinct series of trimming bits, and then the TC of all the chips can be smaller than 7×10^{-6}/°C (Fig. 13b). The mean value and standard deviation of the TC in Fig. 13a are 12.9×10^{-6}/°C and 6.3×10^{-6}/°C respectively, while in Fig. 13b they are 3.8×10^{-6}/°C and 1.1×10^{-6}/°C respectively. Fig. 14 presents five temperature curves after trimming whose middle value is around 3.003 V, and these curves are in agreement with results as shown in Fig. 6.

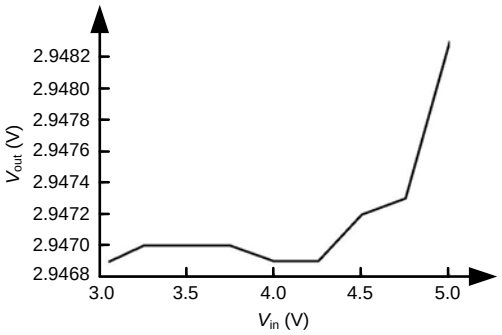

Fig. 10 Relationship between V_{out} and V_{in}

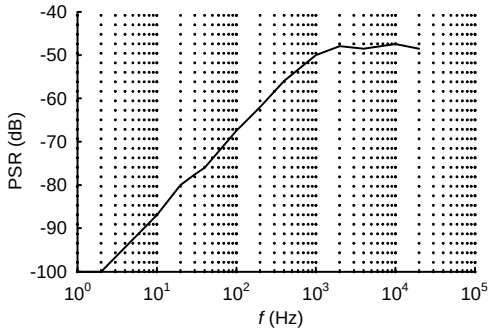

Fig. 11 Relationship between power supply rejection (PSR) and frequency

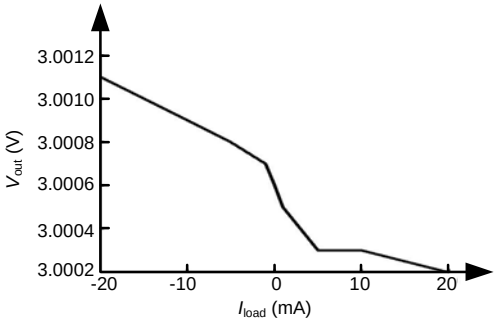

Fig. 12 Relationship between V_{out} and I_{load}

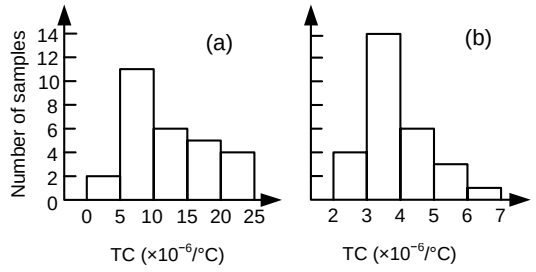

Fig. 13 Measured temperature coefficient (TC) distribution of reference with the same trimming bits (a) and trimmed separately (b)

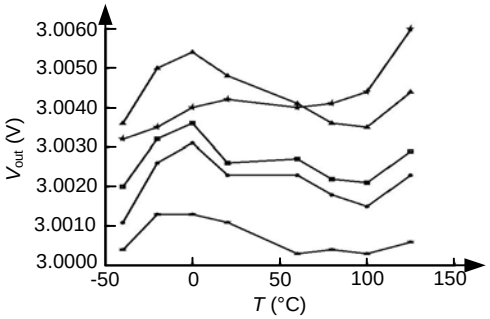

Fig. 14 Relationship between V_{out} and temperature after trimming

Table 1 summarizes a comparison of the performance of recent research and this work. Malcovati *et al*. (2001) presented a voltage reference generated by MOSFETs' threshold voltage, which is of the largest drift. Ge *et al*. (2010) and Sanborn *et al*. (2007) introduced a high-order compensation to the traditional bandgap reference. However, the bipolar and metal oxide semiconductor (BiCMOS) technology used by Sanborn *et al*. (2007) is expensive and not always available. Also, it is demonstrated that the temperature drift of this work is the lowest because a superior high-order compensation structure was used. An LDO is integrated in the circuit for driving ability while it causes the chip to have larger power consumption, larger active area, and larger noise. Noise was not considered too much when we designed our circuits. This work presents poor noise because of LDO's contribution and relatively bad noise characteristics of TSMC's 0.35-μm CMOS model. The noise could not be decreased by simply enlarging MOSFETs' size. To reduce the noise of the voltage reference, we prepared a new version designed with BiCMOS process. Simulation results show a much better noise performance of only 0.5 μV (rms) over the frequency of 0.1 to 10 Hz. Besides, chopping the op-amp is another available method to reduce the reference noise (Ge *et al*., 2010).

5 Conclusions

A low temperature drift voltage reference with resistive trimming circuits, fabricated in TSMC's 0.35-μm CMOS process, has been presented. The chip was designed to minimize the temperature drift. A dual-differential-pair amplifier was used to add compensation with a high-order term of $T\ln T$ to the traditional 1st-order compensated bandgap. The expression of the voltage reference versus temperature has been calculated in detail. To reduce the offset of the amplifier and noise of the bandgap reference, input differential transistors of large size in the amplifier are employed and they all work in weak

Table 1 A comparison of recent research and this work

Literature	Technology	Supply voltage (V)	Output reference (mV)	Temperature range (°C)	Temperature drift ($\times10^{-6}$/°C)	Number of samples
Sanborn *et al*. (2007)*	0.5-μm BiCMOS	1–5	190.9±1.083	−40–125	4–24	32
Ueno *et al*. (2009)*	0.35-μm CMOS	1.4–3	745	−20–80	7–45	17
Ge *et al*. (2010)**	0.16-μm CMOS	1.8±0.18	1087.5	−40–125	5–12	61
This work**	0.35-μm CMOS	3.05–5	3000	−40–125	2.1–7	28

Literature	Supply current (μA)	Noise (0.1 to 10 Hz)	PSR/PSRR	Load ability (mA)	Active area (mm^2)	$V_{ref}\pm3\sigma$ (%)
Sanborn *et al*. (2007)*	20	4 μV (peak-to-peak)	PSR, −86 dB @ DC		N.A.	±0.57
Ueno *et al*. (2009)*	0.22	N.A.	PSRR, −45 dB @ 100 Hz		0.055	±2.61
Ge *et al*. (2010)**	55	6.3 μV (rms)	PSR, −70 dB @ 5 Hz		0.12	±0.15
This work**	120 (52 for BGR)	42 μV (rms) (about 20 μV (rms) for BGR)	PSR, −100 dB @ DC, −50 dB @ 1 kHz	±20	0.4	±0.82

* No trimming; ** Resistive trimming. BGR: bandgap reference; PSRR: power supply rejection ratio; σ: standard deviation. N.A.: not available

inversion to reduce the power consumption. The lowest TC of the voltage reference was measured to be 2.1×10^{-6}/°C over the temperature of −40–125 °C, the PSR @ DC is −100 dB, and the integrated noise is 42 μV (rms) over the frequency of 0.1 to 10 Hz, which makes the circuit very attractive for high precision ADC/DAC design.

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