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Design of dual-edge triggered flip-flops based on quantum-dot cellular automata*

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Abstract: Quantum-dot cellular automata (QCA) technology has been widely considered as an alternative to complementary metal–oxide–semiconductor (CMOS) due to QCA's inherent merits. Many interesting QCA-based logic circuits with smaller feature size, higher operating frequency, and lower power consumption than CMOS have been presented. However, QCA is limited in its sequential circuit design with high performance flip-flops. Based on a brief introduction of QCA and dual-edge triggered (DET) flip-flop, we propose two original QCA-based D and JK DET flip-flops, offering the same data throughput of corresponding single-edge triggered (SET) flip-flops at half the clock pulse frequency. The logic functionality of the two proposed flip-flops is verified with the QCADesigner tool. All the proposed QCA-based DET flip-flops show higher performance than their SET counterparts in terms of data throughput. Furthermore, compared with a previous DET D flip-flop, the number of cells, covered area, and time delay of the proposed DET D flip-flop are reduced by 20.5%, 23.5%, and 25%, respectively. By using a lower clock pulse frequency, the proposed DET flip-flops are promising for constructing QCA sequential circuits and systems with high performance.

Key words: Quantum-dot cellular automata (QCA), Dual-edge triggered (DET), Flip-flop, Sequential circuit
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1 Introduction

With constantly increasing frequencies and downscaling feature sizes in very large scale integration (VLSI) systems, complementary metal–oxide–semiconductor (CMOS) technology is approaching its physical limits and facing serious challenges in power consumption, interconnection, and so on. Much attention has been paid to overcome these obstacles. One of the proposed techniques for effectively increasing performance and lowering power consumption is the dual-edge triggered (DET) flip-flops latching data on both edges of a clock pulse (Hossain *et al.*, 1994; Blair, 1997; Wu and Wei, 1998; Nedovic and Oklobdzija, 2005; Zhao *et al.*, 2007). Extensive research on nanometer alternatives to CMOS has also been carried out. One of the alternatives is known as quantum-dot cellular automata (QCA), which was first proposed by Lent *et al.* (1993) and fabricated by Orlov *et al.* (1997). In the past decades, QCA has attracted considerable attention due to its inherent merits (Amlani *et al.*, 1999; 2000; Bonci *et al.*, 2002; Zeng *et al.*, 2005; Ottavi *et al.*, 2011), and it is anticipated that QCA cells of a few nanometers can be fabricated and operate at terahertz frequencies in the near future (Lent and Isaksen, 2003). A QCA cell is composed of four quantum dots and two extra electrons in a square. Two stable configurations of the electrons can be applied to encode binary information. Logic computation may be performed using the Coulombic repulsion between neighboring cells, rather than using current or voltage

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as is used in CMOS. This unique computational paradigm results in some inherent merits such as ultra low power consumption and wireless interconnection between QCA cells, thus making QCA a promising candidate for future VLSI.

Since the introduction of QCA, a number of interesting QCA-based logic circuits with smaller feature size, higher operating frequency, and lower power consumption than CMOS have been proposed. Utilizing primitives (majority voter and inverter) and QCA wires, various QCA combinational circuits have been presented, such as adders (Wang *et al.*, 2003; Cho and Swartzlander, 2009), multipliers (Cho and Swartzlander, 2009), multiplexers (Gin *et al.*, 1999; Mardiris and Karafyllidis, 2010), comparators (Qiu and Xia, 2007), field-programmable gate arrays (FPGAs) (Amiri *et al.*, 2008), and arithmetic logic units (ALUs) (Gin *et al.*, 1999). However, sequential circuit design in QCA is still in its infancy and limited studies are reported, such as memory circuits (Vankamamidi *et al.*, 2008; Dehkordi *et al.*, 2011) and counters (Askari *et al.*, 2008). Using QCA memory cells to implement sequential elements, however, would be difficult in terms of hardware and latency (Huang *et al.*, 2007), so the design and application of RS, D, JK, and T flip-flops that are level or single-edge triggered (SET) have attracted much attention (Huang *et al.*, 2007; Venkataramani *et al.*, 2008; Shamsabadi *et al.*, 2009; Kong *et al.*, 2010; Yang *et al.*, 2010a; Torabi, 2011). An ideal DET flip-flop allows the same data throughput of a SET flip-flop while operating at half the clock pulse frequency and sampling data on both edges of the clock pulse, so a DET flip-flop shows higher performance than its SET counterpart in terms of data throughput. To date, only one DET D flip-flop structure in QCA has been reported (Yang *et al.*, 2010b). Within this paper, two novel implementations of QCA-based D and JK DET flip-flops are proposed for high performance sequential circuits, and their functionality is verified using the QCADesigner tool (Walus *et al.*, 2004).

2 Preliminaries

2.1 QCA cell

QCA circuits are constructed with an array of QCA cells. As shown in Fig. 1, each QCA cell (Amlani *et al.*, 1999; Zeng *et al.*, 2005) can be represented as a square with four quantum dots and two free electrons. There are two cell types corresponding to two orientations of dots, 90° and 45° orientations. A Schrodinger equation expressed as Hubbard-type Hamiltonian is used to describe the behaviour of the two electrons. These electrons can quantum-mechanically tunnel by modulating tunnel barriers between dots and tend to take up the diagonal dots (corresponding to two ground states) due to Coulombic repulsion (Lent *et al.*, 1994). The two electronic configurations, denoted as cell polarization P=−1 and P=+1, can be encoded as logic 0 and 1, respectively.

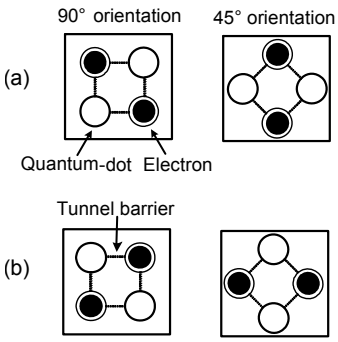

Fig. 1 QCA cell and its two electronic configurations: (a) P=−1, logic 0; (b) P=+1, logic 1

2.2 Logic gates

In QCA, there are two fundamental logic gates for logic completeness: majority gate and inverter (Amlani *et al.*, 1999). As shown in Fig. 2a, a majority gate consists of five QCA cells. The gate realizes a three-variable logic function as follows:

$$M(A,B,C) = AB + AC + BC. \quad (1)$$

According to Eq. (1), an AND or OR gate can be implemented by fixing one input to logic 0 or 1, respectively.

Electron configurations in two adjacent cells arranged diagonally from each other tend to anti-align. By employing this feature, various different inverters can be designed in QCA, but two are more commonly used. As shown in Fig. 2b, the most common inverter is built by arranging seven cells diagonally, while the other is constructed by removing one cell from a line of 90° orientation cells but replacing the missing cell

with two 45° orientation cells. The latter requires fewer cells, but adds the difficulty of manufacturing cells mixed with two different orientations.

Besides logic gates, two types of QCA wire are constructed to transfer data in QCA. One is the binary wire implemented with the cells of 90° orientation, and the other is the inverter chain composed of cells oriented at 45°. Fig. 2c illustrates the wire-crossing structure of two wire types, without destroying the data on either wire (Devadoss *et al.*, 2009). This is an attractive feature having significant applications in the fabrication of QCA.

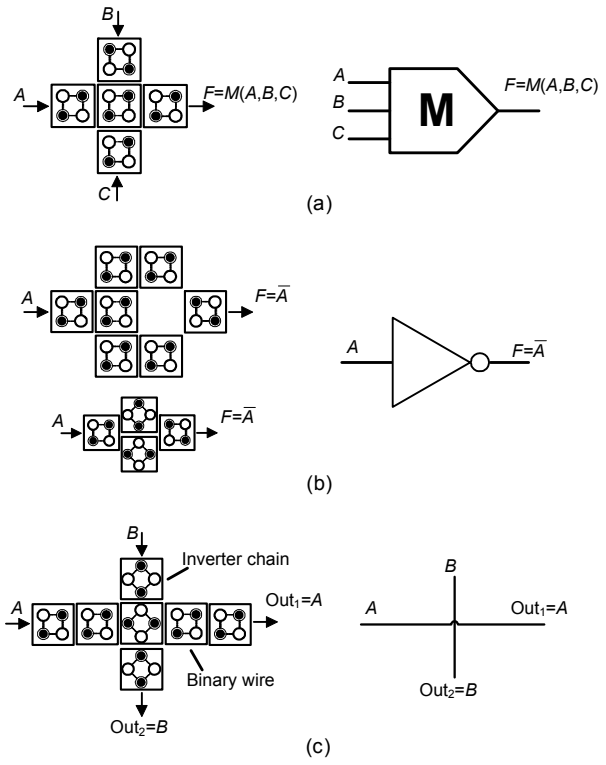

Fig. 2 Logic gates and symbols
(a) Majority gate; (b) Inverter; (c) QCA wire and coplanar wire-crossing

2.3 QCA clocking scheme

Unlike a CMOS circuit having an inherent directionality for information flow, direction of data flow in a QCA circuit is controlled by clock signals. To ensure QCA circuits close to a ground state, a widely adopted clocking scheme is adiabatic switching which utilizes an adiabatic periodic signal with four different phases: switch, hold, release, and relax. The clock signal affects the tunnel barriers between the dots, alternately prohibiting or allowing the electrons to tunnel. Fig. 3a shows its operation process when a clock signal affects an individual cell. During the switch phase, with the tunnel barriers between dots rising slowly, electron tunneling is gradually suppressed and electrons in the cell become localized according to the polarization of its input cell. Note that this is an essential calculation phase in which switching occurs by refreshing its state. During the hold phase, the barriers remain high and no electron tunneling exists. The cell's polarization is latched. Therefore, it can also be used as an input for cells of the next clock zone. With the barriers lowering slowly, the electrons gradually become free and the cell starts to lose its polarization. During the relax phase, the barriers are low, the electrons are free to tunnel and delocalize, and the cell has no polarization, i.e., P=0.

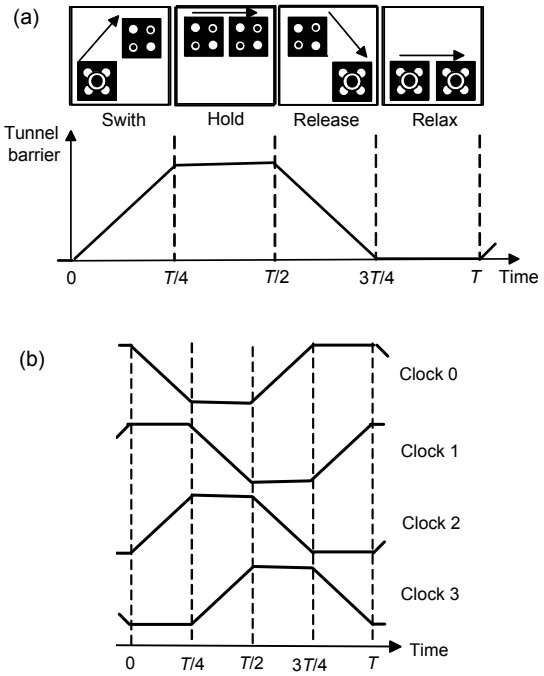

Fig. 3 QCA clocking scheme
(a) QCA clock with four phases; (b) Clock signals

To control data flow, four identical clock signals shifted in phase by 90° (Fig. 3b) are applied to adjacent groups of cells (referred to as clock zones). The clock signals that generate electric fields over QCA cells can be obtained by clock wires buried below the QCA plane. By using clock signals, data information is propagated through QCA circuits and computation is performed. Take a binary wire as an example. QCA cells in the wire are partitioned into four successive

clock zones. Initially, the cell in clock zone 0 is switching according to the fixed input, and then it enters the hold phase while the cell in clock zone 1 starts switching. As its adjacent cell in clock zone 2 is in the relax state, it will not influence the state of the cell in clock zone 1. At the next phase, the cell in clock zone 0 moves to a release phase. The one in clock zone 1 is in the hold state and acts as an input to the cell in clock zone 2 which is in the switch phase. Thus, data information transfers down the wire in a pipelined fashion (Fig. 4). Note that throughout this paper, different shades of QCA cells represent the different clock zones (clock zones 0, 1, 2, 3). More detailed explanations about clocking are available from the literature (Shamsabadi *et al.*, 2009; Yang *et al.*, 2010a). As cells in a binary wire are partitioned into different clock zones, each clock zone can be considered as a latch and latency is also introduced. One clock zone delay corresponds to a quarter of a clock cycle, so a binary wire divided into four consecutive clock zones acts as a delay unit with one clock cycle delay. In this paper, the clocked QCA wire is used to generate a delayed signal. Apart from controlling signal flow, clocking also provides power gain in QCA cells rather than power supply like in conventional circuits.

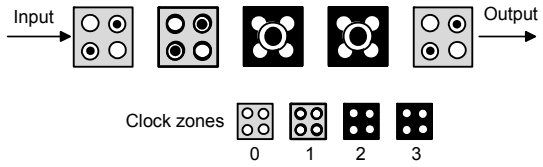

Fig. 4 A binary wire using a four-phase clocking

2.4 Simulation tool

For creating QCA circuits and verifying circuit functionality, a well-known simulation tool QCADesigner (Walus *et al.*, 2004) is used. The tool provides two simulation engines: bistable engine and coherence vector engine. By performing an iterative quantum mechanical simulation, the coherence vector engine can usually produce more accurate results than the bistable engine. Hence, all the designs presented in this paper were simulated by employing the coherence vector engine and its default parameter values: the diameter of quantum dot is 5 nm, the cell size is 18 nm×18 nm, and the cell distance is 2 nm.

2.5 Schemes for implementing DET flip-flops

To design QCA-based DET flip-flops with high performance, an efficient approach is to map existing structures of CMOS flip-flops into their majority logic counterparts. Thus, the major focus of this subsection is to introduce schemes of DET flip-flops in CMOS.

DET flip-flop design techniques in CMOS usually encompass the design of D flip-flops. Schemes for implementing DET D flip-flops can be categorized mainly into two distinct groups, the pulsed latch scheme and the latch/MUX scheme (Zhao *et al.*, 2007), shown in Figs. 5a and 5b, respectively. The pulsed latch scheme consists of one latch with a pulse generator. The purpose of the pulse generator is to create a narrow pulse, the CP_pulse, after each edge of clock signal CP, and then the CP_pulse is used as the clock input to drive the latch. The latch/MUX scheme generally uses two paralleled opposite level-sensitive flip-flops (D latches) with a multiplexer. When CLK=1, the upper latch receives input *D*, and then the multiplexer selects and outputs the data stored in the lower one as the DET flip-flop's output. Inversely, a complementary process occurs when CLK=0. Thus, the outputs of both the pulsed latch scheme and the latch/MUX scheme track the input *D* at both edges of the clock signal.

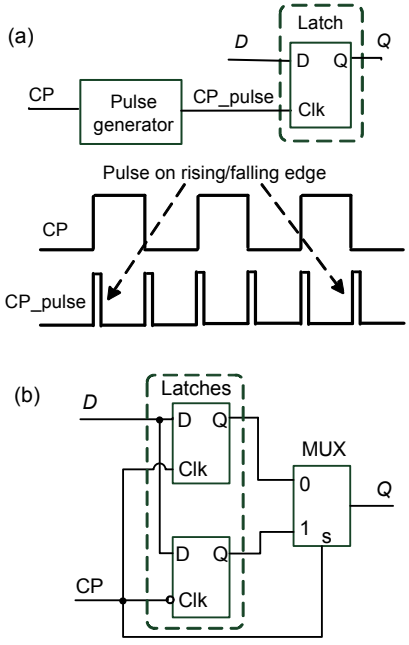

Fig. 5 Two DET D flip-flop schemes
(a) Pulsed latch scheme; (b) Latch/MUX scheme

3 DET JK flip-flop design based on QCA

Our proposed QCA-based DET JK flip-flop follows the aforementioned pulsed latch scheme except that the D latch is replaced with a JK latch (level-sensitive JK flip-flop). Fig. 6 shows the corresponding QCA structure, which utilizes one JK latch and a QCA pulse generator. An advanced JK latch proposed by Kong *et al.* (2010), in which output *Q* is fed through feedback paths (arrowhead feedback path) to two AND gates (dashed squares c and d), is adopted. The QCA layout of the pulse generator, originally proposed by Yang *et al.* (2010b), comprises three inverters, three majority voters, and three coplanar wire-crossings. Its detailed explanation of operation can be found in Yang *et al.* (2010b).

By viewing the simulation results illustrated in Fig. 7, the delay of the QCA pulse generator is two clock cycles because CP goes through eight clock zones for obtaining CP_pulse. Obviously, the QCA pulse generator correctly produces the desired pulse signal CP_pulse at a repetition rate determined by the value of the input signal CP. However, it must be pointed out that this CP is different from the QCA clock signal. The CP is an independent input of the flip-flop while the QCA clock signal is fixed to clock zones for modulating tunnel barriers of QCA cells. The advantage of introducing independent CP is that the design of QCA sequential circuits may be simplified by reducing the attention to timing constraints. Now, the CP_pulse goes through two AND gates (dashed squares a and b in Fig. 6) to conduct AND operations between CP_pulse and JK latch's inputs *J* and *K*, respectively. It means that only when CP_pulse attains high level '1' during the narrow transparent windows, can inputs *J*, *K* drive the JK latch and affect the latch's output *Q*. Thus, the output *Q* of the proposed flip-flop will change its state only in the narrow transparent windows of CP_pulse in correspondence with the transitions of the CP, and depends on the inputs *J*, *K*.

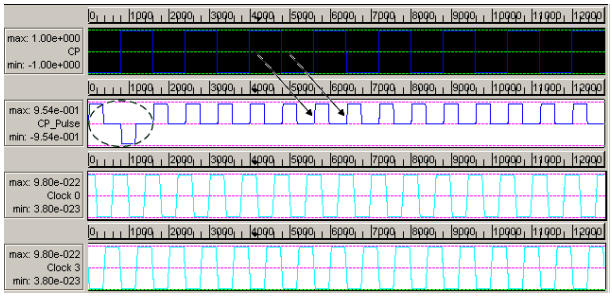

Fig. 7 Simulation waveforms for the QCA pulse generator
The generator has a delay of two clock cycles, labeled with a dashed ellipse on CP_pulse. The rising and falling edges of CP and the corresponding narrow transparent windows of CP_pulse are outlined with two arrowheads

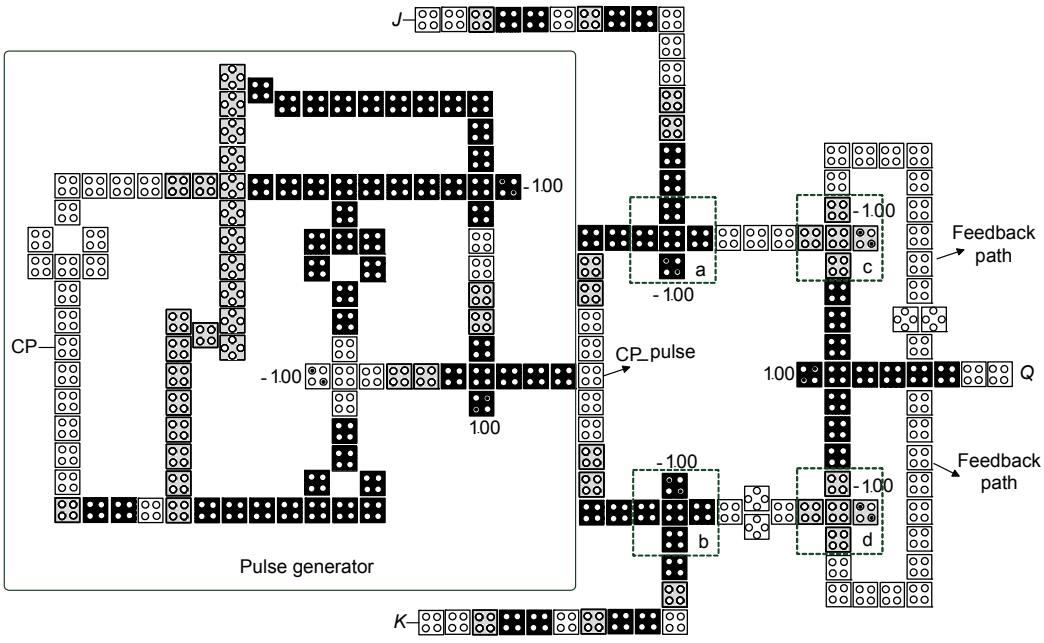

Fig. 6 Proposed QCA DET JK flip-flop structure which uses one JK latch and a QCA pulse generator as shown in the lined square

Fig. 8 shows the input and output simulation waveforms for the proposed DET JK flip-flop. The proposed DET JK flip-flop operates at the dual edge of the CP and has ideal logic functionality. Since the CP traverses eight clock zones of the pulse generator before arriving at the output cell, its delay is two clock cycles. Then CP_pulse triggers the JK latch and goes through another eight clock zones of JK latch, resulting in another delay of two clock cycles. Thus, the whole delay of the proposed flip-flop is four clock cycles and the first meaningful output Q appears after four clock cycles. The edge of CP and the corresponding state transfer of output Q are highlighted with four arrowheads. There are four edges of CP when J=K=1, and the output Q of the DET JK flip-flop changes its states (following $Q^{n+1}=\overline{Q^n}$) four times. Namely, the states of the proposed flip-flop output Q change at both falling and rising edges. Hence, the proposed design behaves as a DET JK flip-flop.

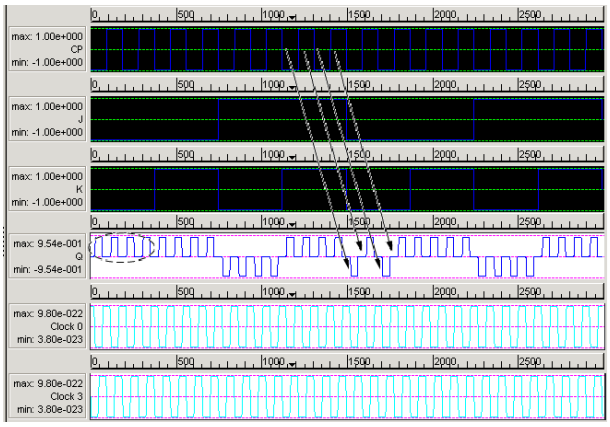

Fig. 8 Simulation waveforms for proposed DET JK flip-flop
The first three waveforms represent the input signals CP, J, and K, respectively; the fourth represents the output signal Q. The whole delay is four clock cycles, labeled with a dashed ellipse. The edge of CP and the corresponding state transfer of output Q are highlighted with four arrowheads

4 DET D flip-flop design based on QCA

As outlined previously, Yang *et al.* (2010b) proposed one QCA-based DET D flip-flop structure following a pulsed latch scheme as illustrated in Fig. 5a. Besides the pulsed latch scheme, an alternate DET D flip-flop structure is the latch/MUX scheme. In this section, we propose a QCA-based DET D flip-flop following a latch/MUX scheme. The proposed flip-flop (Fig. 9) uses five majority voters and two inverters. An important consideration is that two D latches are effectively buried in the two AND logic gates (dashed squares a, b), which conduct AND operations with input D. The MUX can be realized with two AND gates and one OR gate, which may selectively transmit its two input signals. More importantly, we insert a four-cell wire clocked by four consecutive clock zone signals (dashed ellipse) to produce a delayed signal CP_d, through which a signal propagates for one complete clock cycle as discussed earlier. After implementing $D\cdot CP$ and $D\cdot\overline{CP}$ by two AND gates, another two AND operations are conducted, and then an OR operation is applied by using AND gates (dashed squares c, d) and an OR gate (dashed square e) in MUX, which can be denoted as $D\cdot CP\cdot\overline{CP\_d}$, $D\cdot\overline{CP}\cdot CP\_d$, and $D\cdot(CP\cdot\overline{CP\_d}+\overline{CP}\cdot CP\_d)$, respectively. This means that when logical states of CP and CP_d are unequal (corresponding to a narrow transparent window after CP edges), output Q of the flip-flop tracks the input D.

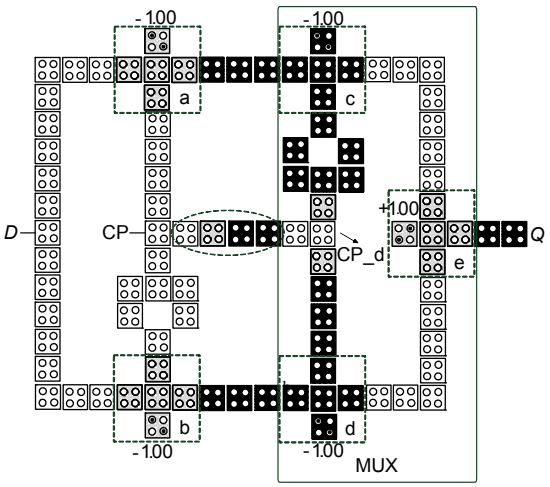

Fig. 9 Proposed QCA DET structure which consists of a latch and a MUX highlighted with a lined rectangle

The input and output waveforms are simulated to verify the function of our proposed DET D flip-flop. Fig. 10 shows that the overall delay of the proposed DET D flip-flop is 1.5 clock cycles because the input signals CP and D go through six clock zones. From the output Q, the proposed DET D flip-flop operates properly on both falling and rising edges of the CP.

For example, there are four edges of CP when *D* inputs logic '1', and *Q* of the DET D flip-flop outputs '1', which is equal to the input *D*. Hence, the proposed design behaves as a DET D flip-flop. Moreover, our design uses only 93 cells from the QCA layout. Compared with Yang *et al*. (2010b)'s DET D flip-flop structure, the number of cells, covered area, and time delay of the proposed DET D flip-flop are reduced by 20.5%, 23.5%, and 25%, respectively. Furthermore, coplanar wire-crossing is eliminated in our design while Yang's structure has three coplanar wire-crossings. The performance comparison of the two DET D flip-flops is illustrated in Table 1, showing that our design has lower delay and simpler structure than Yang's.

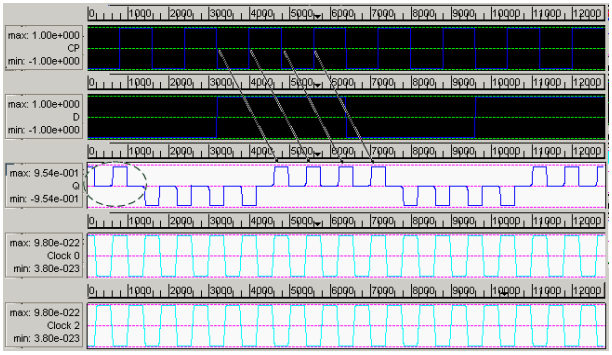

Fig. 10 Simulation waveforms for the proposed DET D flip-flop

The delay is 1.5 clock cycles, highlighted with a dashed ellipse. The edge of CP and the corresponding state transfer of output *Q* are labeled with four arrowheads

Table 1 Performance comparison of QCA-based DET D flip-flops between Yang *et al.* (2010b)'s design and our design

Parameter	Value	
	Yang *et al.*'s	Ours
Number of cells	117	93
Covered area (μm)	0.17	0.13
Time delay (clock)	2	1.5
Number of wire-crossings	3	0

5 Conclusions

QCA, one of the most promising nanotechnologies, offers a new computational paradigm which is suitable for logic circuits. A number of interesting QCA-based logic circuits with smaller feature size, higher operating frequency, and lower power consumption than CMOS have been presented. However, designs for QCA flip-flops, especially high performance DET flip-flops, have not been widely considered by QCA designers. In this paper, we propose two novel QCA-based DET flip-flops, a DET JK flip-flop with a pulse generator and a DET D flip-flop following the latch/MUX scheme. The logic functionality of the two proposed DET flip-flops is verified with the QCADesigner tool. Both of our proposed QCA-based DET flip-flops show higher performance than their SET counterparts in terms of data throughput. Furthermore, results of performance comparison indicate that our proposed DET D flip-flop has lower delay and simpler structure than Yang's DET D flip-flop. Using a lower clock frequency than SET flip-flops, the QCA-based DET flip-flop might be beneficial for design of high performance digital circuits and systems, which will be our future work.

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