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A new via chain design method considering confidence level and estimation precision*

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Abstract: For accurate prediction of via yield, via chains are usually fabricated on test chips to investigate issues about vias. To minimize the randomness of experiments and make the testing results more convincing, the confidence level and estimation precision of the via failure rate are investigated in this paper. Based on the Poisson yield model, the method of determining an adequate number of total vias is obtained using the law of large numbers and the de Moivre-Laplace theorem. Moreover, for a specific confidence level and estimation precision, the method of determining a suitable via chain length is proposed. For area minimization, an optimal combination of total vias and via chain length is further determined. Monte Carlo simulation results show that the method is in good accordance with theoretical analyses. Results of via failure rates measured on test chips also reveal that via chains designed using the proposed method has a better performance. In addition, the proposed methodology can be extended to investigate statistical significance for other failure modes.

Key words: Poisson yield model, Via chain, Via failure rate, Confidence level, Estimation precision
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1 Introduction

Typically, a large complete integrated circuit (IC) may have tens of millions of vias which allow metallic connection between different layers in nanometer technology (Hess *et al.*, 2003). An entire chip may experience complete failure owing to defect of a single via of predominant design. A via may fail partially or completely due to various reasons, such as random defects, electron migration, cut misalignment, and thermal stress induced voiding effects (Liang *et al.*, 2010). Thus, it is crucial to reduce the yield loss due to via failures, and via yield analysis indeed plays an important role in product yield analysis.

Specially designed test structures are used to investigate yield, extract characterization parameters, and control process steps. For vias, via chain test structures are usually fabricated on test chips to investigate issues about vias and sometimes to control the manufacturing process. Early in 1982, via chains had been used as a technique to control the electromigration of non-overlapping via holes (Rathore, 1982), and then to investigate factors that affect the yield and interconnection resistance (Shih *et al.*, 1992). Afterwards, via chain structures were proposed as part of a new set of test structures to investigate electro-migration in submicron technology (Morgan *et al.*, 1996). Subsequently, via chain test structures were used to evaluate optical proximity correction (OPC) (Nasuno *et al.*, 2004), categorize resistance by the OBIRCH image in 45-nm technology (Matsubara and Watanabe, 2006), and investigate the backside failure analysis technique (Li *et al.*, 2008). All the previous work took via chains as a method to test yield or control the fabrication process. Experiments were performed with a certain number of vias and via chains. However, few investigations had been done on the reasons why the authors chose

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those sample sizes of vias and via chains. The statistical theoretical bases of their choice were not explained. Their results might be subject to stochastic noise, so further analyses were necessary.

In this paper we propose a new via chain design method considering confidence level and estimation precision. Via failure mechanisms and via yield models are presented, which are the bases for subsequent analyses. The method to determine an appropriate amount of total vias and the number of vias in each via chain is proposed. Statistical analyses interpret this method theoretically. Simulation results show good accordance with theoretical analyses. Wafer experiment results in SMIC 45-nm technology and hypothesis testing of the measured results also validate the performance of this method.

2 Via failure mechanism and via yield model

Particles may originate from various sources including people, machines, chemicals, and process gases. Such particles may be airborne or may be suspended in liquids or gases (Plummer *et al.*, 2000). The influence of a particle defect on a via is mainly reflected in its coverage area to a via, which can be sorted into two types: complete covering and partial covering. The two types of covering correspond to open failure and reliability failure respectively, whose examples are shown in Fig. 1. The complete covering defect type causes the vertical conducting cooper in a via hole completely open and the yield of vias is brought down. In the partial covering situation, the defect covers only part of a via hole and the width of the vertical conducting cooper has been narrowed. Since reliability is strongly related to yield and reliability testing is more expensive and more time consuming, we focus on via yield in this paper.

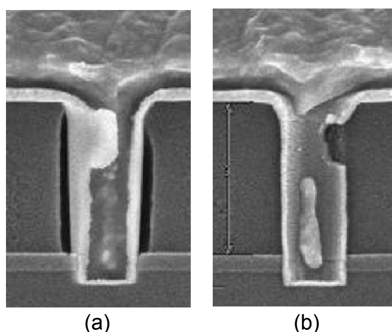

Fig. 1 Vias with a reliability failure (a) or open failure (b)

A yield model is a bridge between test structures and products. The Poisson yield model is one of the most frequently used models. This yield model assumes that the distribution of defects is random and that the occurrence of a defect is independent of the occurrence of other faults. The Poisson distribution is as follows (Stapper, 1983):

$$P_c(M=k)=\frac{e^{-\lambda_c}\cdot\lambda_c^{\,k}}{k!}. \tag{1}$$

In the case of via analysis, $P_c(M=k)$ is the probability of a via chain having M faults (M=0, 1, 2, …) and λ_c is the average value of faulty vias.

The $P_c(M=0)$ is equal to via chain yield Y_c. Hence, the via chain yield Y_c can be written as

$$Y_c=e^{-\lambda_c}. \tag{2}$$

If the number of vias in each via chain is n, according to the relationship between binominal distribution and Poisson distribution, Eq. (2) can be rewritten as

$$Y_c=e^{-np}, \tag{3}$$

where p is the failure rate for each single via. Hence, p can be estimated in the following way:

$$p=-\frac{\ln(H_c/N_c)}{n}, \tag{4}$$

where N_c is the number of via chains and H_c is the number of faulty via chains. The value of p for a specific technology can be obtained using the measured results of test structures. Subsequently, the measured p can be used to predict via yield for a product fabricated in the same technology.

3 Via chain design considering confidence level and estimation precision

Intuitively, when designing via chains, care has to be taken in the choice of the number of total vias as the statistical randomness of the via yield result becomes significant for a very small number of total vias. On the other hand, in an actual production process, the number of total vias cannot be too large when

testing costs and utilization efficiency of the wafer area are taken into account. Besides the number of total vias, another important factor needed to be investigated is the number of vias in each via chain. A shorter via chain will prevent the occurrence of multiple via defects in a via chain and thus will lead to a more precise yield testing result, but it requires more area of pads. Conversely, in excessively long via chains, the number of via chains without defects will be very small, which will decrease the precision of the tested via yield. Therefore, to increase the estimation precision of the testing results and make the yield more convincing, it is important to consider the confidence level and estimation precision when designing via chains.

3.1 Number of total vias

If the probability of the occurrence of an open failure for a single via is denoted by via failure rate p, the probability of not opening is $1-p$. The testing result of each via can be taken as the result of a Bernoulli trial. The failure of each via is independent of others, so the results of N vias are the results of N Bernoulli trials. Assuming M is the frequency of open vias in N Bernoulli trials, then M is a random variable and it obeys the binominal distribution, which can be denoted by $M\sim B(N, p)$, where N is the sample size. Hence, the determination of an appropriate number of total vias is turned into the determination of the sample size N. Given a confidence level $1-\alpha$ ($0<\alpha<1$) and an estimation precision ε_v, the requirements of the total number of vias N can be expressed using the law of large numbers (de Cooman and Miranda, 2008; Zhu *et al.*, 2012):

$$P\{|\hat{p}-p|<\varepsilon_\text{v}\}=P\{|M/N-p|<\varepsilon_\text{v}\}>1-\alpha. \quad (5)$$

According to the de Moivre-Laplace theorem (Konno, 2002), if random variable η_n obeys binominal distribution with parameters of n and p, for any x, we have

$$\lim_{x\to\infty}P\left\{\frac{\eta_n-np}{\sqrt{np(1-p)}}\le x\right\}=\int_{-\infty}^{x}\frac{1}{\sqrt{2\pi}}\text{e}^{-t^2/2}\text{d}t=\Phi(x). \quad (6)$$

With the use of Eq. (6), Eq. (5) can be rewritten as

$$P\{|\hat{p}-p|<\varepsilon_\text{v}\}\approx 2\Phi\left(N\varepsilon_\text{v}\Big/\sqrt{Np(1-p)}\right)-1. \quad (7)$$

Letting $2\Phi\left(N\varepsilon_\text{v}\Big/\sqrt{Np(1-p)}\right)-1>1-\alpha$, the requirement of N can be obtained:

$$N>\frac{z_{\alpha/2}{}^2\cdot p(1-p)}{\varepsilon_\text{v}{}^2}, \quad (8)$$

where $z_{\alpha/2}$ is the upper fractile of the standard normal distribution.

By carefully selecting the value of ε_v and α according to actual requirements, the number of total vias can be obtained using Eq. (8). N is inversely proportional to the square of the estimation precision. If estimation precision is increased tenfold, the total number will become one hundred times larger. N is proportional to p and square of $z_{\alpha/2}$. The larger the p and $z_{\alpha/2}$, the more the vias needed.

Usually the value of p is very small, so Eq. (8) can be expressed as

$$N>\frac{z_{\alpha/2}{}^2\cdot p}{\varepsilon_\text{v}{}^2}. \quad (9)$$

Eqs. (8) and (9) are the requirements of the number of total vias N. As long as the inequality above is satisfied, Eq. (5) is satisfied. Therefore, the tested via failure rate $\hat{p}$ is very close to the actual via failure rate p and lies in the interval ($p-\varepsilon_\text{v}$, $p+\varepsilon_\text{v}$) with a probability higher than $1-\alpha$.

3.2 Number of vias in the via chain

To test the via failure rate, vias are usually connected in the form of via chains. The via chain yield Y_c is given in Eq. (3). Taking the derivative of Y_c, the following equation can be obtained:

$$\Delta Y_\text{c}=-n\text{e}^{-np}\cdot\Delta p, \quad (10)$$

where Δp is the change in p and ΔY_c is the change in Y_c. From Eq. (5), the precision requirement of p is $\Delta p=|\hat{p}-p|<\varepsilon_\text{v}$, so Eq. (10) can be expressed as

$$|\Delta Y_\text{c}|<n\cdot\text{e}^{-np}\cdot\varepsilon_\text{v}. \quad (11)$$

To guarantee the testing precision of Y_c, the following inequality should be satisfied:

$$P\{|\hat{Y}_\text{c}-Y_\text{c}|<\varepsilon_\text{c}\}=P\{|H_\text{c}/N_\text{c}-Y_\text{c}|<\varepsilon_\text{c}\}>1-\beta, \quad (12)$$

where $\widehat{Y}_c$ is the tested yield of via chains and Y_c is the actual value of the via chain yield. ε_c is the estimation precision of the tested via chain yield. It can be inferred from Eq. (11) that ε_c is $n\mathrm{e}^{-np}\varepsilon_v$. $1-\beta$ ($0<\beta<1$) is the confidence level for via chain yield. Using the de Movire-Laplace theorem in Eq. (6), when the premise of the normal distribution approximation

$$N_c Y_c = (N/n)\mathrm{e}^{-np} > 5 \tag{13}$$

is satisfied, Eq. (12) can be treated in the same way as Eq. (5). Hence, the requirement of N_c can be obtained:

$$N_c > \frac{z_{\beta/2}^2 \cdot Y_c(1-Y_c)}{\varepsilon_c^2}. \tag{14}$$

Using Eq. (3), Eq. (11), and $N_c=N/n$, Eq. (14) can be rewritten as

$$N \cdot \varepsilon_v^2 / z_{\beta/2}^2 > (1-\mathrm{e}^{-np})/(n \cdot \mathrm{e}^{-np}). \tag{15}$$

Thus, the requirement of n is

$$\begin{cases} (N/n)\cdot \mathrm{e}^{-np} > 5, \\ N \cdot \varepsilon_v^2 / z_{\beta/2}^2 > (1-\mathrm{e}^{-np})/(n \cdot \mathrm{e}^{-np}), \end{cases} \tag{16}$$

where N is a specific value which satisfies Eq. (9). Solving this set of inequalities the upper level of n (i.e., the number of vias in each via chain) can be determined. Unfortunately, this set of inequalities has no explicit solutions. But numerical solutions can still be obtained by numerical software.

3.3 Determining optimal *N* and *n*

So far, the range requirements of N and n have been obtained. As long as Eqs. (9) and (16) are satisfied, the tested via failure rate is precise enough and can be used to predict the via yield of product. However, for different combinations of N and n, the area occupied by via chains differs significantly. It is not expected that the wafer be wasted by an inappropriate combination of N and n, so the investigation of optimal N and n is needed.

For Eq. (9), $z_{\alpha/2}^2 \cdot p / \varepsilon_v^2$ can be expressed as N_b. Thus, N can be denoted as $K_v N_b$ or $K_v \cdot z_{\alpha/2}^2 \cdot p / \varepsilon_v^2$, where K_v is a coefficient larger than 1. Hence, Eq. (16) can be rewritten as

$$\begin{cases} K_v \cdot z_{\alpha/2}^2 \cdot p \cdot \mathrm{e}^{-np} / (n \cdot \varepsilon_v^2) > 5, \\ K_v \cdot z_{\alpha/2}^2 \cdot p / z_{\beta/2}^2 > (1-\mathrm{e}^{-np})/(n \cdot \mathrm{e}^{-np}). \end{cases} \tag{17}$$

If α and β take the same value, Eq. (17) can be further simplified as

$$\begin{cases} K_v \cdot z_{\alpha/2}^2 \cdot p \cdot \mathrm{e}^{-np} / (n \cdot \varepsilon_v^2) > 5, \\ K_v \cdot p > (1-\mathrm{e}^{-np})/(n \cdot \mathrm{e}^{-np}). \end{cases} \tag{18}$$

Usually, via chains have to be connected by pads, which are organized in the form of pad frame. Each via chain has two pins, so a couple of pads in a pad frame is needed to test a via chain. The total area A_{total} occupied by via chain test structures can be expressed in the following way:

$$A_{total} = A_{pc} \cdot N_c + A_{via} \cdot N = K_v \cdot N_b (A_{pc}/n + A_{via}), \tag{19}$$

where A_{pc} is the area of a pad couple and A_{via} is the area each via occupies.

Solving Eq. (18), which can be abbreviated as IDUL*n* (inequalities determining the upper limit of n), the numerical solutions of n corresponding to each K_v can be obtained. Substituting these numerical solutions into Eq. (19), the value of a series of A_{total} can be acquired. The minimum area value can be found among these area values. If the minimum value is denoted as A_{total_min}, the corresponding n and K_v are just the optimal n_{opt} and K_{v_opt}. Hence, the optimal number of total vias can be calculated by $K_{v_opt} \cdot N_b$.

4 Simulations and wafer experiments

Monte Carlo simulations are performed on computers with Matlab R2010b. At the beginning of simulations, only the number of total vias or only via chain length is considered. Subsequently, the effects of both total vias and via chain length are considered. To facilitate comparison, actual via failure rates used in the simulations are all 5×10^{-4}.

Eight groups of simulations are conducted using different numbers of total vias (Fig. 2) to illustrate Eq. (9). The deviation of measured p becomes more and more significant with the decrease of N. The

lower limit of N can be determined by Eq. (9). Another eight sets of simulations are conducted considering only the via chain length (Fig. 3) to illustrate Eq. (16). As n increases, the deviation of p becomes larger. The upper limit of the via number in each via chain can be determined by Eq. (16).

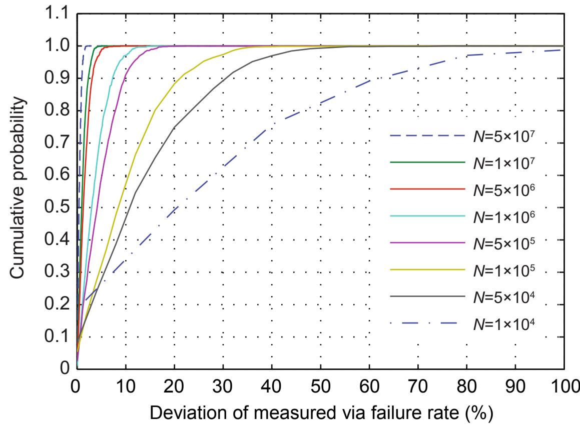

Fig. 2 Cumulative probability versus deviation of measured via failure rate (n is the same)

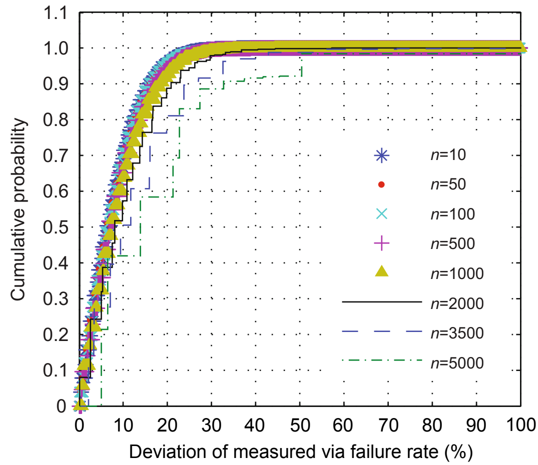

Fig. 3 Cumulative probability versus deviation of measured via failure rate (N is the same)

When both N and n are considered and α and β take the same value, IDULn can be obtained. For convenient analysis and prediction the range of ε_v is between the same order of magnitude as p and two orders of magnitude smaller than p. In this study, p is set to 10^{-4}. Thus, for precision consideration, ε_v is taken as 10^{-5}. The solutions of IDULn are shown in Fig. 4. When K_v is small, the upper limit of n increases rapidly with the growth of K_v. When K_v increases, however, the increasing rate of the upper limit of n is slowed down.

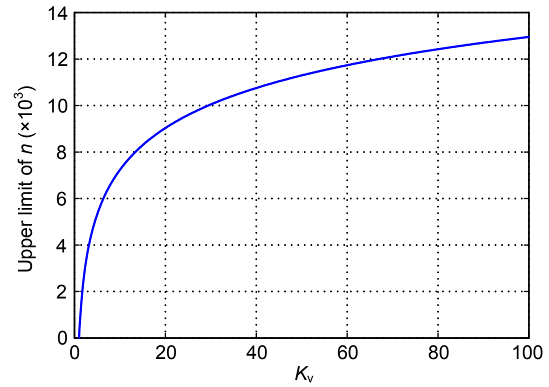

Fig. 4 Upper limit of n for IDULn

To further verify the consistency between simulations and IDULn, four groups of tests are carried out (Table 1). All groups have the same theoretical p (5×10^{-4}), ε_v (10^{-5}), α (0.05), β (0.05), and number of tests (10000). Different K_v in each group leads to different N and different upper limits of n. For K_v in groups 1, 3, and 4, the percentages of tests with deviations within ε_v are larger than 95%. Group 2 is a reference group relative to group 1. The via chain length in group 2 is slightly longer than the upper limit of n, which means that the percentage of tests with deviations within ε_v does not meet the requirement of the confidence level $1-\alpha$. Hence, the precision of IDULn is pretty good.

Table 1 Verification of consistency between simulations and IDULn*

Parameter	Value			
	Group 1	Group 2	Group 3	Group 4
K_v	1.1	1.1	5	25
N	21128801	21128801	96040001	480200001
Upper limit of n	375.4	375.4	5320.8	9589.4
n in tests	375	380	5320	9589
Deviation within ε_v	95.01%	94.94%	95.02%	95.00%

* All groups have the same theoretical p (5×10^{-4}), ε_v (10^{-5}), α (0.05), β (0.05), and number of tests (10000)

The methodology proposed above to determine N and n also helps save the wafer area. Optimal N and n can be found using Eq. (19). When p is 5×10^{-4}, α and β are 0.05, and ε_v is 10^{-5}, the calculated N_b is 19208001. In SMIC 45-nm technology, the relationship between A_{total} and K_v is shown in Fig. 5. When K_v is 2.4 and n is 3107, the minimum A_{total} obtained is 340519522.8 μm^2.

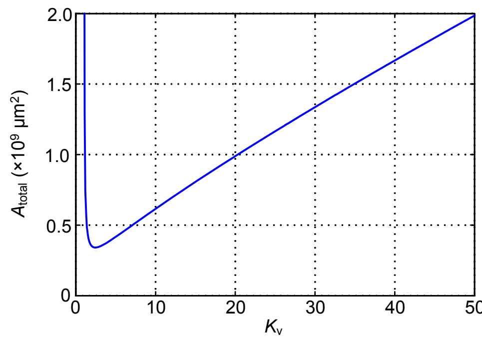

Fig. 5 Relationship between total area of via chains and K_v

In the wafer experiments, two types of via chain test structures are designed on test chips. One is the original via chain test structure (OVCTS), which is performed using the previous via chain design method; the other is the new via chain test structure (NVCTS) considering confidence level and estimation precision. OVCTS and NVCTS occupy a small area of the test chip whose area is 1 cm^2. The test chip also includes many other types of test structures fabricated in SMIC 45-nm technology. The locations of OVCTS and NVCTS are close to each other on each test chip to synchronize the occurrence of random defects.

In OVCTS, the number of vias in each via chain is 99 840 and the number of via chains is 2688, resulting in totally 274 560 000 vias used to test the via failure rate. The area occupied by OVCTS in each test chip is 1.4 mm^2, and 56 test chips are needed to fabricate all the vias. The number of total vias and the number of vias in each via chain, however, are determined according to experience of designers.

In NVCTS, the confidence level used is 95% and the estimation precision used is 10^{-7}. The K_{v_opt} is 1.74 and is obtained when minimum A_{total} is acquired using Eq. (19). Thus, the number of total vias is 2 139 187 034 and the number of vias in each via chain is 319 234. The area occupied by NVCTS in each test chip is 4.6 mm^2, and 56 test chips are needed to fabricate all the vias. The 56 test chips containing NVCTS are the same 56 chips containing OVCTS.

These via chains are fabricated in the Via-1 layer, connected by Metal-1 and Metal-2. The layout of four via chain test structures used in test chips of NVCTS is shown in the lower part of Fig. 6. A via chain test structure unit is boxed by a dotted line in the lower right of Fig. 6. As shown in this figure, a via chain test structure is composed of n vias and two pads, labeled as pad_A and pad_B. A small part of a via chain is marked by a circle on the layout of the first via chain test structure located in the left side. This small part of the via chain is zoomed in, as shown in the upper part of Fig. 6. Parameters of the area of a pad couple A_{pc} and the area of each via A_{via} are also marked by dotted lines.

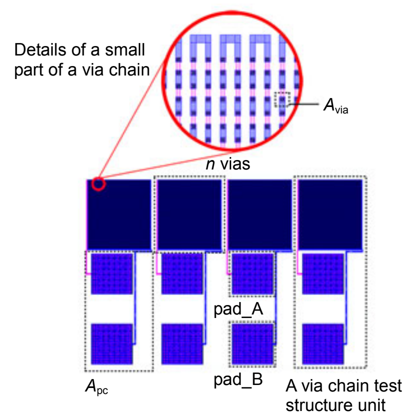

Fig. 6 Layout of four via chain test structures

When being tested, pad_A and pad_B of a via chain test structure are connected to two probe pins of a testing machine. A fixed voltage is applied to a via chain through a switching matrix, and the current flowing through it is measured. Hence, the resistance of the via chain is calculated by V/I. The basic schematic of the test setup to measure a via chain is shown in Fig. 7. The number of vias in each via chain and the resistance of each via are known, so the theoretical via chain resistance is obtained. Based on this resistance value, a threshold resistance value R_{th} is determined to judge whether a via chain is open or not. Usually, threshold resistance is set to at least one order of magnitude larger than the theoretical resistance of the

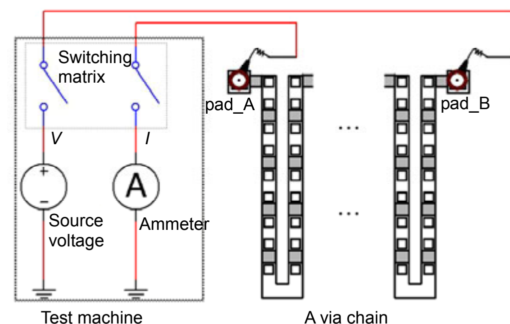

Fig. 7 Basic schematic of test setup to measure a via chain

via chain. If the measured resistance is larger than R_{th}, the via chain is considered to be open. When the measured resistance is smaller than R_{th}, the via chain is thought to have no open vias.

To compare the testing results of the two types of via chains, 16 groups of experiments are performed. Each group contains 56 test chips, so there are 896 test chips in total. A via failure rate obtained by OVCTS and a via failure rate obtained by NVCTS are acquired in each group, and there are 32 tested via failure rates totally. Table 2 shows the testing results.

Table 2 Testing results of 16 groups of wafer experiments

Group No.	N_{open}		Y_c		p	
	OVCTS	NVCTS	OVCTS	NVCTS	OVCTS	NVCTS
1	745	4270	0.7228	0.3628	3.25E-06	3.18E-06
2	732	4244	0.7277	0.3667	3.18E-06	3.14E-06
3	742	4289	0.7240	0.3599	3.24E-06	3.20E-06
4	734	4272	0.7269	0.3625	3.19E-06	3.18E-06
5	705	4313	0.7377	0.3564	3.05E-06	3.23E-06
6	739	4268	0.7251	0.3631	3.22E-06	3.17E-06
7	714	4255	0.7344	0.365	3.09E-06	3.16E-06
8	752	4279	0.7202	0.3614	3.29E-06	3.19E-06
9	775	4350	0.7117	0.3508	3.41E-06	3.28E-06
10	729	4226	0.7288	0.3693	3.17E-06	3.12E-06
11	735	4295	0.7266	0.3591	3.20E-06	3.21E-06
12	730	4292	0.7284	0.3595	3.17E-06	3.21E-06
13	743	4306	0.7236	0.3574	3.24E-06	3.22E-06
14	715	4261	0.7340	0.3641	3.10E-06	3.17E-06
15	725	4332	0.7303	0.3535	3.15E-06	3.26E-06
16	694	4317	0.7418	0.3558	2.99E-06	3.24E-06

N_{open}: number of tested open via chains; Y_c: yield of via chain; p: tested via failure rate

To evaluate the statistical significance of the testing results of the two structures, hypothesis testing is used. The F-test is used to evaluate whether the results of these two structures have the same variance (Montgomery and Runger, 2002). When null hypothesis H_{01} is $\sigma_1^2=\sigma_2^2$ and the alternative hypothesis is $\sigma_1^2\neq\sigma_2^2$, the F statistic is defined as

$$F=S_1^2\big/S_2^2, \tag{20}$$

where S_1^2 and S_2^2 are sample variances of the two structures, respectively. The degrees of freedom for the numerator and denominator are both 15. The results of F-test are shown in Table 3. Both the F statistic and 2-tail P-value indicate that the variances of the two structures are significantly different. As shown in Table 3, the variance of NVCTS is much smaller than the variance of OVCTS. Hence, NVCTS is more stable than OVCTS.

Table 3 Two-sample F-test for variances*

Statistic	OVCTS	NVCTS
Mean	3.18E-06	3.20E-06
Variance	9.71E-15	1.82E-15
Number of observations	16	16
Degrees of freedom	15	15
F statistic	5.3307	
2-tail P-value	0.0025	
2-tail F critical	2.8600	

* Significance level is 0.05

To further assess the statistical significance of the means of the two structures, Welch's t test is used (Welch, 1947). When null hypothesis H_{02} is $\mu_1=\mu_2$ and the alternative hypothesis is $\mu_1\neq\mu_2$, the t statistic is given by

$$t=(\overline{X_1}-\overline{X_2})\Big/\sqrt{S_1^2/n_1+S_2^2/n_2}, \tag{21}$$

where $\overline{X_1}$ and $\overline{X_2}$ are sample means of the two structures respectively, and n_1 and n_2 are the numbers of observations of the two structures respectively. The degrees of freedom υ associated with Welch's t test is approximated using the Welch-Satterthwaite equation:

$$\upsilon=\frac{(S_1^2/n_1+S_2^2/n_2)^2}{(S_1^2/n_1)\big/(n_1-1)+(S_2^2/n_2)\big/(n_2-1)}. \tag{22}$$

If υ is not an integer, it is rounded to calculate two-tail probabilities. When the significance level is 0.05, results of t-test are shown in Table 4. The t statistic and 2-tail P-value both indicate that the means of the two structures are not significantly different, which is consistent with the reality as the two via chain test structures are fabricated on the same test chips and the tested via failure rates should be close to each other.

Results of the two hypothesis tests reveal that means of the two structures do not show statistical significance while the variances of the two structures are significantly different. Due to careful choice of the number of total vias and the number of vias in each via chain, NVCTS has a more stable tested via

failure rate. In addition, it is convincing to say that the deviation between tested p and actual p is within 10^{-7} with a probability larger than 95%. Hence, NVCTS which is designed using the method proposed in this paper has a better performance.

Table 4 Two-sample Welch's *t*-test for means

Statistic	OVCTS	NVCTS
Mean	3.18E-06	3.20E-06
Variance	9.71E-15	1.82E-15
Number of observations	16	16
Degrees of freedom	20	20
t statistic	−0.4862	
2-tail *P*-value	0.6321	
2-tail *t* critical	2.0860	

5 Discussion

The via chain design method proposed in this paper increases the evaluation precision of the measured via failure rate and makes the tested via yield more convincing. Some relevant points are worth discussing before using the equations derived in this paper.

Strictly speaking, the via failure rate depends on the sizes of vias, the expected sizes of failures, and the physical mechanism that determines failures (Gill *et al.*, 2002). Furthermore, in deep submicron technologies failure is also pattern-dependent. Hence, the via chain design method is not applicable to every chain pattern (Cabrini *et al.*, 2006). For different manufacturing processes, or a manufacturing process with different sizes of vias, the assumption that the failure of each via is independent of others is not established. Thus, for these situations, equations derived in this paper are no longer applicable. However, in a specific via layer of via chain test structures, the sizes of vias are usually the same, and the expected failure size and the via failure mechanisms are also the same. Hence, the assumption that the failure of each via is independent of others is still established and equations derived in this paper are still applicable. Furthermore, for vias in other via layers in via chain test structures, as long as the sizes of vias, the expected failure size, and the via failure mechanisms are the same between vias in that layer, the method proposed in this paper can also be used. The only change needed is to find parameters p, A_{pc}, and A_{via} for that via layer before using the same calculation method again.

To maintain a specific confidence level and estimation precision, various combinations of N and n can be chosen as shown in Eq. (16). For a larger N, the via chain length n also becomes larger. As a result, more via failures occur in a via chain, making it more different to locate a via failure. However, the localization of failures in via chains is not mainly concerned in this proposed method. The greatest concern in this study is area optimization. For the optimal combination of N and n calculated by this area optimization method, there usually will be more than one via failure in a via chain.

A further interesting discussion is about testing time optimization. If the minimum testing time is mainly concerned instead of minimum testing area, the choice of optimal N and n will be slightly different. The total testing time T_{total} for all via chain test structures can be expressed as

$$T_{total} = T_c \cdot N_c = K_v \cdot N_b (T_c/n), \tag{23}$$

where T_c is the time used to test a via chain. Substituting numerical solutions of n corresponding to each K_v into Eq. (23), a series of T_{total} can be acquired. The minimum testing time can be found among these values. If the minimum testing time value is denoted as T_{total_min}, the corresponding n and K_v are just the optimal n_{T_opt} and K_{vT_opt}. For a specific confidence level and estimation precision, N_b is constant. For a specific testing machine, T_c is constant. Thus, solving minimum T_{total} is reduced to solving minimum $K_v \cdot (1/n)$. Eq. (19) can be rewritten as

$$A_{total} = N_b \cdot A_{pc} \cdot K_v (1/n + A_{via}/A_{pc}), \tag{24}$$

and the problem of solving minimum A_{total} can also be reduced to the problem of solving minimum $K_v(1/n+A_{via}/A_{pc})$. Usually, the area of two pads A_{pc} is much larger than the area occupied by a via. With the scaling down of the technology process, A_{via} is becoming smaller and smaller, while A_{pc} remains stable. Thus, the value of A_{via}/A_{pc} is approaching zero. The optimal n_{T_opt} and K_{vT_opt} for testing time optimization are very close to the optimal n_{opt} and K_{v_opt} for testing area optimization. Hence, when designing the via chain test structure, the area optimization method proposed here is also good for testing time optimization.

6 Conclusions

The presented method of determining the number of total vias and the number of vias in each via chain increases the evaluation precision of the measured via failure rate. This method changes the status of designing via chain test structures purely based on past experience and makes the tested via failure results more convincing. By selecting parameters according to the actual requirements of confidence level and estimation precision, adequate combinations of total vias and via chain length can be obtained. The optimal combination can be acquired when the area occupied by via chains is minimized. Monte Carlo simulations show that the number of total vias and the number of vias in each via chain do affect the confidence level and estimation precision of the tested via failure rates. Various simulation results are consistent with those obtained using the proposed method of designing via chains. Furthermore, 16 groups of wafer experiments are performed by 45-nm technology. *F*-test and Welch's *t*-test indicate that the proposed method has a better performance. Some important notes about the proposed method are discussed. Although we focus on the via open failure in this paper, the proposed methodology can be extended to investigate statistical significance for other failure modes.

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