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A novel ternary JK flip-flop using the resonant tunneling diode literal circuit

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Abstract: A literal circuit with a three-track-output structure is presented based on resonant tunneling diodes (RTDs). It can be transformed conveniently into a single-track-output structure according to the definition and properties of the literal operation. A ternary resonant tunneling JK flip-flop is created based on the RTD literal circuit and the module-3 operation, and the JK flip-flop also has two optional types of output structure. The design of the ternary RTD JK flip-flop is verified by simulation. The RTD literal circuit is the key design component for achieving various types of multi-valued logic (MVL) flip-flops. It can be converted into ternary D and JK flip-flops, and the ternary JK flip-flop can also be converted simply and conveniently into ternary D and ternary T flip-flops when the input signals satisfy certain logical relationships. All these types of flip-flops can be realized using the traditional Karnaugh maps combined with the literal and module-3 operations. This approach offers a novel design method for MVL resonant tunneling flip-flop circuits.

Key words: Resonant tunneling diode (RTD), Ternary logic, Literal circuit, Module-3 operation, JK flip-flop
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1 Introduction

In traditional binary sequential digital systems, various structures and types of flip-flop circuits have been successfully developed, especially the JK flip-flop, which has the best performance and the most powerful function in all types of flip-flop circuits. Compared with binary logic, multi-valued logic (MVL) has a greater signal volume rate and can reduce the number and complexity of interconnections. It can also greatly increase density as well as processing speed, and uses fewer signals to realize more functions. MVL has more obvious advantages in the process of transmission and storage than binary logic. Therefore, the subject of MVL is very important for research and has been receiving increasing attention (Homma *et al*., 2012; Sasao, 2012; Wu *et al*., 2012; Yuminaka and Okui, 2012). However, in current multi-valued flip-flop design, almost all circuits are realized based on complementary metal oxide semiconductor (CMOS). There are not many reports of multi-valued flip-flops, especially JK flip-flop circuits, based on resonant tunneling devices. A resonant tunneling diode (RTD) has a unique negative differential resistance (NDR) characteristic, which allows for diverse multiple-valued application areas (Berezowski and Vrudhula, 2005; 2007; Lin *et al*., 2007; 2011b; Núñez *et al*., 2008). Thus, in this paper, an edge-triggered ternary JK flip-flop based on RTDs is presented. The circuit can be converted simply and conveniently into the ternary D flip-flop or the ternary T flip-flop, and further enriches the types of multi-valued resonant tunneling flip-flops available.

First, the module-3 operation, literal operation and their properties in the ternary algebra system are described. Second, the characteristics of RTDs are introduced. RTD is one of the most popular quantum devices in recent research. Its unique NDR characteristic leads to broad applications. A literal circuit composed of RTDs with three-track-output structure

is presented. Third, based on the RTD literal circuit, a ternary JK flip-flop with three-track-output structure is created. Simulation results verify the correctness of the design. A ternary T flip-flop is also designed, and the conversion relationships in the RTD literal circuit and ternary JK flip-flop, D flip-flop, and T flip-flop are established.

2 Operations and properties in the ternary algebra system

In ternary logic, the operations module-3 plus and module-3 multiplication are defined as shown in Eqs. (1) and (2), and the literal operation is defined as in Eq. (3) (Wu, 1994; Zhang and Wu, 2008; Hang and Zhou, 2011):

$$x \oplus y = (x + y)_{\text{mod-3}}, \tag{1}$$

$$x \bullet y = (x \cdot y)_{\text{mod-3}}, \tag{2}$$

$${}^{i}x^{i} = \begin{cases} 2, & x = i, \\ 0, & x \neq i, \end{cases} \quad i \in \{0,\ 1,\ 2\}. \tag{3}$$

In Eqs. (1) and (2), '+' is a plus operation and '·' is a multiplication operation.

The main properties of module-3 operations and literal operations are as follows:

Mutually exclusive property:

$${}^{i}x^{i} \cdot {}^{j}x^{j} = 0, \quad i \neq j. \tag{4}$$

Complementary property:

$$\begin{cases} x \oplus \overline{x} = 2, \\ \overline{x} = 2x \oplus 2, \end{cases} \quad x \in \{0,\ 1,\ 2\}, \text{ and } \overline{0} = 2,\ \overline{1} = 1,\ \overline{2} = 0. \tag{5}$$

$${}^{0}x^{0} + {}^{1}x^{1} + {}^{2}x^{2} = 2. \tag{6}$$

Reducibility property:

$$\begin{cases} x = {}^{2}x^{2} + 1 \cdot {}^{1}x^{1}, \\ x = \overline{{}^{0}x^{0}}(1 + \overline{{}^{1}x^{1}}). \end{cases} \tag{7}$$

$$\begin{cases} i(ix) = x, \ \ x \in \{1,\ 2\}, \\ 2i \oplus (i \oplus x) = x, \ \ x \in \{0,\ 1,\ 2\}. \end{cases} \tag{8}$$

$${}^{i}x^{i} = \overline{{}^{j}x^{j} + {}^{k}x^{k}} = \overline{{}^{j}x^{j}} \cdot \overline{{}^{k}x^{k}}, \ i \neq j \neq k. \tag{9}$$

In the next section, we will design the ternary JK flip-flop according to the above properties of the literal and module-3 operations, combined with RTDs. The ternary RTD T flip-flop is also created.

3 RTD literal circuit

RTD is one of the most popular quantum devices and has the properties of bistability and self-latching. It can reduce a large number of devices constituting circuits, sometimes needing only 1/3–1/5 of the number of components compared with traditional digital circuits. These properties further reduce parameters such as the number of nodes, line length, parasitic effects, and power consumption. In addition, the capacitance of the RTD is very small and dynamic power loss is low. The RTD always operates in a low current maintenance status, so the circuits based on RTD have very low power consumption (Guo, 2009). When an RTD is combined with three-terminal devices such as high electron mobility transistors (HEMTs), field effect transistors (FETs), and hetero-junction bipolar transistors (HBTs) to acquire three-terminal devices, it can produce very high speed circuits with excellent performance (Li, 2009). Its working frequency is generally in the range of a few to dozens of GHz. It maintains a very high work speed, and by changing only the control voltage of HEMT, FET, or HBT, the circuits can achieve a variety of logic functions. Therefore, the properties of ultra-high speed, ultra-high frequency, ultra-high integration density, high efficiency, and low power loss make RTDs an extremely important prospect for application in future very-large-scale integrations (VLSI) (Ebata *et al*., 2010; Lee *et al*., 2010; Liang *et al*., 2010; Suzuki *et al*., 2010). The use of RTD+HEMT will be described in this paper. The symbols and *I-V* characteristic curves of RTD and RTD+HEMT are shown in Fig. 1. The characteristic curve of RTD+ HEMT is similar to that of an RTD. It has the negative differential resistance characteristic, and its peak current I_p is controlled by the input signal, which increases with increasing input signal V_G. In this study, the simulation of the RTD is implemented using the MOS-NDR RTD emulator (Bhattacharya *et al*., 2000; González *et al*., 2001). The V_p of the RTD is about 0.37 V, V_v is about 0.56 V, and the peak/valley ratio of the current is about 10:1. The threshold value V_t of the HEMT is 0.3 V.

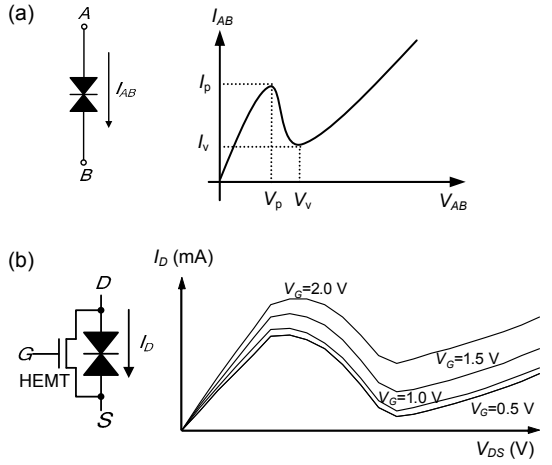

Fig. 1 Symbols and *I-V* characteristics of the resonant tunneling diode (RTD) (a) and the RTD+HEMT (b)

The RTD literal circuit with three-track-output structure controlled by HEMTs (Fig. 2a) was proposed in our previous study (Lin *et al*., 2011a). It is composed of three similar units built up in a loop, and each output track is a (0, 2) literal operation. The units comprising the literal circuit are the RTD binary NOR, NAND circuits (Lin *et al*., 2004), and the MOBILE inverter (Núñez *et al*., 2007). V_{CK} is a pulse signal. All these units are rising-edge-triggered units of V_{CK}; when V_{CK} is fixed at high voltage, the outputs remain unchanged. The simplified structure of the RTD literal circuit is shown in Fig. 2b.

The output results of the RTD literal circuit are

$$\begin{cases} {}^2Q^2 = \overline{({}^1Q^1 + {}^0Q^0)\cdot L_{2D}}, \\ {}^1Q^1 = \overline{({}^2Q^2 + {}^0Q^0)\cdot L_{1D}}, \\ {}^0Q^0 = \overline{({}^1Q^1 + {}^2Q^2)\cdot L_{0D}}. \end{cases} \tag{10}$$

Though Eq. (10) has connections not only with the other two previous outputs ${}^iQ^i$, but also with the input signals L_{iD} from the rising-edge trigger of V_{CK}, not all the combinations of L_{iD} are suitable. According to the definition and properties of the literal operation, some combinations of L_{iD} are forbidden. The different effects on the outputs by the different settings of the input L_{iD} are described in Table 1. When two or three inputs L_{iD} are logic '0', Eqs. (4), (6), (7), and (9) will be invalid. Therefore, at most one input signal can be logic '0', or at least two input signals should be logic '2'.

$$L_{iD} + L_{jD} = 2, \text{ or } \overline{L_{iD}}\cdot\overline{L_{jD}} = 0, \quad i \neq j. \tag{11}$$

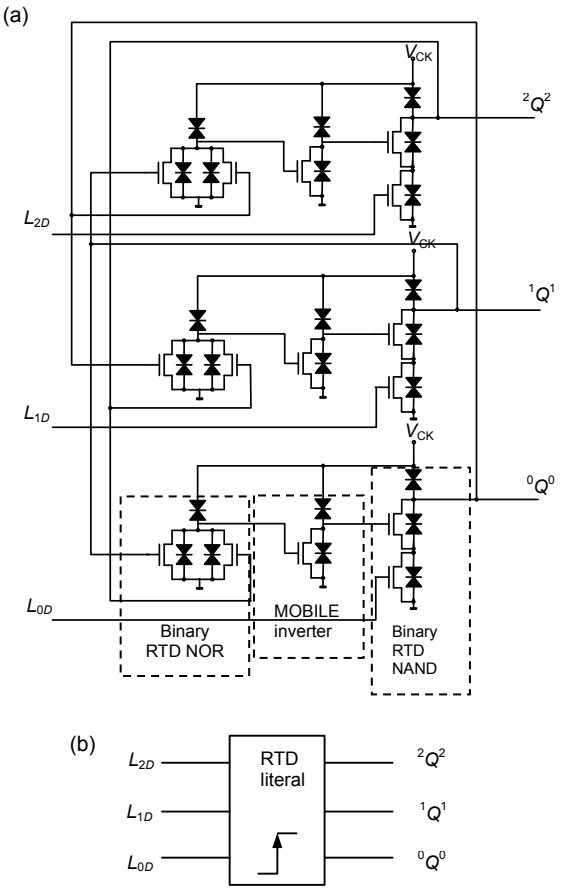

Fig. 2 The RTD literal circuit with three-track output (a) and its simplified model (b)

Table 1 Logic functions of a resonant tunneling diode (RTD) literal circuit

L_{2D}	L_{1D}	L_{0D}	${}^2Q'^2$	${}^1Q'^1$	${}^0Q'^0$	Q'
0	0	0	×	×	×	×
0	0	2	×	×	×	×
0	2	0	×	×	×	×
0	2	2	2	0	0	2
2	0	0	×	×	×	×
2	0	2	0	2	0	1
2	2	0	0	0	2	0
2	2	2	${}^2Q^2$	${}^1Q^1$	${}^0Q^0$	Q

×: forbidden state

Each output track signal ${}^iQ^i$ of the RTD literal is a (0, 2) signal. Combined with Eq. (7), the three-track-output structure can be transformed into a single-track-output structure with the ultimate trivalued signal of Q.

After simplification by the Karnaugh maps of Table 1, it can be concluded that the corresponding

next state equations with restriction relationships are as follows:

$$\begin{cases} Q' = \overline{L_{2D}} + 1 \cdot \overline{L_{1D}} + L_{1D} \cdot L_{0D} \cdot Q, \\ {}^2Q'^2 = \overline{L_{2D}} + L_{1D} \cdot L_{0D} \cdot {}^2Q^2, \\ {}^1Q'^1 = \overline{L_{1D}} + L_{2D} \cdot L_{0D} \cdot {}^1Q^1, \\ {}^0Q'^0 = \overline{L_{0D}} + L_{2D} \cdot L_{1D} \cdot {}^0Q^0. \end{cases} \tag{12}$$

The RTD literal circuit is the core component of the ternary flip-flops design. In the following section, we will design novel ternary resonant tunneling flip-flop circuits based on this literal operation circuit.

4 Study of Ternary RTD JK flip-flop

4.1 Ternary RTD JK flip-flop

Wu and Bi (1984) proposed the next state equation of a ternary JK flip-flop:

$$Q' = J \oplus (1 \oplus J \oplus K) \bullet Q. \tag{13}$$

According to module-3 operations, we can draw the Karnaugh map of the next state Q' when Q has different values (Fig. 3).

The three literal operations ${}^0Q'^0$, ${}^1Q'^1$, ${}^2Q'^2$ of Q' can be derived from the Karnaugh map shown in Fig. 3 combined with the definition of literal and module-3 operations. Taking ${}^0Q'^0$ as an example, its Karnaugh map is as shown in Fig. 4, with all '0' circled in the figure.

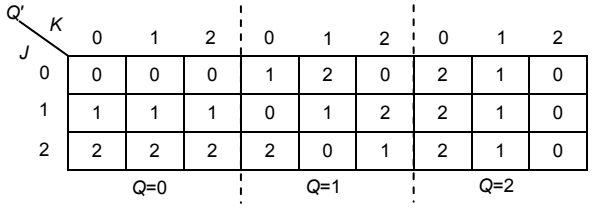

Fig. 3 Karnaugh map of a ternary JK flip-flop

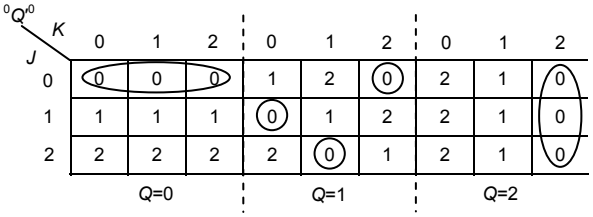

Fig. 4 Karnaugh map of ${}^0Q'^0$

So, the expression of ${}^0Q'^0$ can be expressed as

$$\begin{aligned} {}^0Q'^0 = {}& {}^0J^{0\,0}Q^0 + ({}^0J^{0\,2}K^2 + {}^1J^{1\,0}K^0 + {}^2J^{2\,1}K^1)\,{}^1Q^1 \\ & + {}^2K^{2\,2}Q^2. \end{aligned} \tag{14}$$

Likewise, the expressions of ${}^1Q'^1$ and ${}^2Q'^2$ are

$$\begin{aligned} {}^1Q'^1 = {}& {}^1J^{1\,0}Q^0 + ({}^0J^{0\,0}K^0 + {}^1J^{1\,1}K^1 + {}^2J^{2\,2}K^2)\,{}^1Q^1 \\ & + {}^1K^{1\,2}Q^2, \end{aligned} \tag{15}$$

$$\begin{aligned} {}^2Q'^2 = {}& {}^2J^{2\,0}Q^0 + ({}^0J^{0\,1}K^1 + {}^1J^{1\,2}K^2 + {}^2J^{2\,0}K^0)\,{}^1Q^1 \\ & + {}^0K^{0\,2}Q^2. \end{aligned} \tag{16}$$

Comparing Eqs. (14)–(16) with the outputs of the RTD literal circuit shown in Eq. (12) and making them be equal, we can obtain the expression of the ternary JK flip-flop with the RTD literal circuit as follows:

$$\begin{cases} \overline{L_{0D}} = ({}^0J^{0\,2}K^2 + {}^1J^{1\,0}K^0 + {}^2J^{2\,1}K^1)\,{}^1Q^1 + {}^2K^{2\,2}Q^2, \\ \overline{L_{1D}} = {}^1J^{1\,0}Q^0 + {}^1K^{1\,2}Q^2, \\ \overline{L_{2D}} = {}^2J^{2\,0}Q^0 + ({}^0J^{0\,1}K^1 + {}^1J^{1\,2}K^2 + {}^2J^{2\,0}K^0)\,{}^1Q^1. \end{cases} \tag{17}$$

So, as long as we make the three inputs L_{0D}, L_{1D}, and L_{2D} of the RTD literal circuit correspond respectively to the three values in Eq. (17), the literal circuit can be used in the design of a ternary JK flip-flop.

When any two equations in Eq. (17) are multiplied, the results shown in Eq. (18) are produced. The results indicate that the application of the RTD literal circuit in the ternary JK flip-flop fully satisfies the restrictions given in Eq. (11).

$$\begin{cases} \overline{L_{1D}} \cdot \overline{L_{0D}} = ({}^1J^{1\,0}Q^0 + {}^1K^{1\,2}Q^2) \cdot ({}^0J^{0\,2}K^{2\,1}Q^1 \\ \qquad + {}^1J^{1\,0}K^{0\,1}Q^1 + {}^2J^{2\,1}K^{1\,1}Q^1 + {}^2K^{2\,2}Q^2) = 0, \\ \overline{L_{2D}} \cdot \overline{L_{1D}} = ({}^2J^{2\,0}Q^0 + {}^0J^{0\,1}K^{1\,1}Q^1 + {}^1J^{1\,2}K^{2\,1}Q^1 \\ \qquad + {}^2J^{2\,0}K^{0\,1}Q^1) \cdot ({}^1J^{1\,0}Q^0 + {}^1K^{1\,2}Q^2) = 0, \\ \overline{L_{2D}} \cdot \overline{L_{0D}} = ({}^2J^{2\,0}Q^0 + {}^0J^{0\,1}K^{1\,1}Q^1 + {}^1J^{1\,2}K^{2\,1}Q^1 \\ \qquad + {}^2J^{2\,0}K^{0\,1}Q^1) \cdot ({}^0J^{0\,2}K^{2\,1}Q^1 + {}^1J^{1\,0}K^{0\,1}Q^1 \\ \qquad + {}^2J^{2\,1}K^{1\,1}Q^1 + {}^2K^{2\,2}Q^2) = 0. \end{cases} \tag{18}$$

The simulation curves of the ternary JK flip-flop with three-track-output structure given by SPICE are shown in Fig. 5.

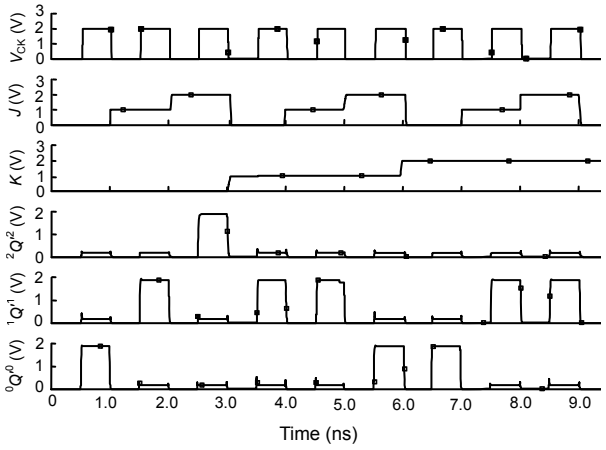

Fig. 5 Simulation curves of a ternary three-track-output JK flip-flop

Supposing that the initial value of Q is '0' and V_{CK} is a 2 V pulse signal, then τ of the MOS-NDR RTD net is about 22 ps, the rising time (TR) of V_{CK} is about 3τ–5τ, the high voltages of input signals J and K are 2 V, the middle voltages of J and K are about 1 V, the high voltage of ${}^iQ'^i$ is about 1.9 V, the low voltage is about 0.29 V, and the frequency is about 1 GHz. Here the output is a three-track-output structure and each track is a (0, 2) value. If required, according to Eq. (7), using the RTD NOR, NAND circuits, and MOBILE inverters, it could conveniently realize (0, 1, 2) ternary logic output.

The ${}^2J^2$, ${}^2K^2$, ${}^0J^0$, and ${}^0K^0$ in Eq. (17) can be expressed by two MOBILEs (Uemura and Baba, 2000) (Figs. 6a and 6b). According to Eq. (9), the literal operation ${}^1x^1$ can also be expressed by ${}^2x^2$ and ${}^0x^0$, so the structure of ${}^1J^1$, ${}^1K^1$ is as shown in Fig. 6c.

Considering the effects of V_{CK}, Eqs. (14)–(16) can further be rewritten as

$$\begin{cases} {}^2Q'^2 = [{}^2J^2\,{}^0Q^0 + ({}^0J^0\,{}^1K^1 + {}^1J^1\,{}^2K^2 + {}^2J^2\,{}^0K^0)\,{}^1Q^1 \\ \quad + {}^0K^0\,{}^2Q^2]V_{CK\uparrow} + {}^2Q^2 \cdot V_{CKH}, \\ {}^1Q'^1 = [{}^1J^1\,{}^0Q^0 + ({}^0J^0\,{}^0K^0 + {}^1J^1\,{}^1K^1 + {}^2J^2\,{}^2K^2)\,{}^1Q^1 \\ \quad + {}^1K^1\,{}^2Q^2]V_{CK\uparrow} + {}^1Q^1 \cdot V_{CKH}, \\ {}^0Q'^0 = [{}^0J^0\,{}^0Q^0 + ({}^0J^0\,{}^2K^2 + {}^1J^1\,{}^0K^0 + {}^2J^2\,{}^1K^1)\,{}^1Q^1 \\ \quad + {}^2K^2\,{}^2Q^2]V_{CK\uparrow} + {}^0Q^0 \cdot V_{CKH}. \end{cases} \tag{19}$$

4.2 Interconversion between ternary JK and ternary D flip-flops

In the previous discussion of the ternary D flip-flop, by making L_{2D}, L_{1D}, and L_{0D} respectively the three literal operations $\overline{{}^2D^2}$, $\overline{{}^1D^1}$, and $\overline{{}^0D^0}$ of signal D, the D flip-flop function can be realized (Lin *et al.*, 2011a):

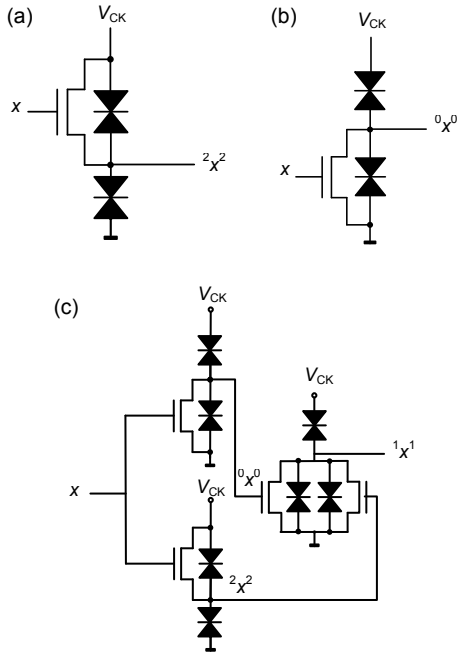

Fig. 6 Structure of the literal operations ${}^2x^2$ (a), ${}^0x^0$ (b), and ${}^1x^1$ (c)

$$\begin{cases} {}^2Q'^2 = {}^2D^2 + \overline{{}^1D^1} \cdot \overline{{}^0D^0} \cdot {}^2Q^2 = {}^2D^2, \\ {}^1Q'^1 = {}^1D^1 + \overline{{}^2D^2} \cdot \overline{{}^0D^0} \cdot {}^1Q^1 = {}^1D^1, \\ {}^0Q'^0 = {}^0D^0 + \overline{{}^2D^2} \cdot \overline{{}^1D^1} \cdot {}^0Q^0 = {}^0D^0. \end{cases} \tag{20}$$

Comparing Eq. (20) with Eqs. (14)–(16), and making the three literal operations be equal, we obtain

$$\begin{aligned} {}^0Q'^0 = {}^0D^0 + \overline{{}^2D^2} \cdot \overline{{}^1D^1} \cdot {}^0Q^0 = {}^0J^0\,{}^0Q^0 \\ + ({}^0J^0\,{}^2K^2 + {}^1J^1\,{}^0K^0 + {}^2J^2\,{}^1K^1)\,{}^1Q^1 + {}^2K^2\,{}^2Q^2. \end{aligned} \tag{21}$$

So, from Eq. (9),

$$\overline{{}^2D^2} \cdot \overline{{}^1D^1} = {}^0D^0 = {}^0J^0. \tag{22}$$

$$\begin{aligned} {}^2Q'^2 = {}^2D^2 + \overline{{}^1D^1} \cdot \overline{{}^0D^0} \cdot {}^2Q^2 = {}^2J^2\,{}^0Q^0 \\ + ({}^0J^0\,{}^1K^1 + {}^1J^1\,{}^2K^2 + {}^2J^2\,{}^0K^0)\,{}^1Q^1 + {}^0K^0\,{}^2Q^2. \end{aligned} \tag{23}$$

Similarly, from Eq. (9),

$$\overline{{}^1D^1}\cdot\overline{{}^0D^0}={}^2D^2={}^0K^0. \tag{24}$$

According to Eqs. (22) and (24), it can be assumed that in the ternary JK flip-flop and D flip-flop,

$$J=D,\ \ K=\overline{D}. \tag{25}$$

The logic equations in Eq. (25) make the equation tenable as shown in Eq. (26), so the logic relationship of Eq. (25) is verified.

$$\begin{aligned}{}^1Q'^1 &= {}^1D^1+\overline{{}^2D^2}\cdot\overline{{}^0D^0}\cdot{}^1Q^1={}^1J^1\,{}^0Q^0\\ &\quad+({}^0J^0\,{}^0K^0+{}^1J^1\,{}^1K^1+{}^2J^2\,{}^2K^2)\,{}^1Q^1+{}^1K^1\,{}^2Q^2.\end{aligned} \tag{26}$$

4.3 Interconversion between ternary JK and ternary T flip-flops

The next state equation of the ternary T flip-flop is $Q'=T\oplus Q$. We can deduce the three literal operations of the T flip-flop (Table 2).

Table 2 Logic functions of the ternary T flip-flop

T	Q	$T\oplus Q$	${}^0(T\oplus Q)^0$	${}^1(T\oplus Q)^1$	${}^2(T\oplus Q)^2$
0	0	0	2	0	0
0	1	1	0	2	0
0	2	2	0	0	2
1	0	1	0	2	0
1	1	2	0	0	2
1	2	0	2	0	0
2	0	2	0	0	2
2	1	0	2	0	0
2	2	1	0	2	0

From Table 2, we obtain

$$\begin{cases}{}^2Q'^2={}^2(T\oplus Q)^2={}^0T^0\,{}^2Q^2+{}^1T^1\,{}^1Q^1+{}^2T^2\,{}^0Q^0,\\ {}^1Q'^1={}^1(T\oplus Q)^1={}^0T^0\,{}^1Q^1+{}^1T^1\,{}^0Q^0+{}^2T^2\,{}^2Q^2,\\ {}^0Q'^0={}^0(T\oplus Q)^0={}^0T^0\,{}^0Q^0+{}^1T^1\,{}^2Q^2+{}^2T^2\,{}^1Q^1.\end{cases} \tag{27}$$

Comparing Eq. (27) with Eqs. (21), (23), and (26), we obtain

$$J=T,\ \ K=2T.$$

This is consistent with the results described by Wu (1994), and verifies the correctness of the ternary JK flip-flop design.

According to above analysis, the model can create the relationships among several ternary flip-flops and the RTD literal circuit (Fig. 7). As long as the logic relationships are satisfied, the ternary JK, D, and T flip-flops can be converted conveniently.

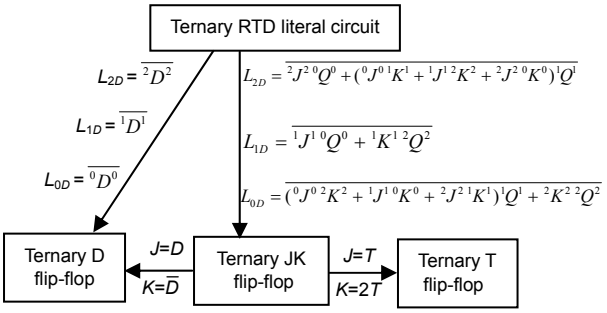

Fig. 7 Transformation relational graph of several ternary flip-flops

5 Conclusions

A ternary JK flip-flop has been created based on the RTD literal circuit and the definition and properties of the module-3 operation. It can realize both one-track-output and three-track-output structures according to the properties of literal operations. The JK flip-flop has a powerful function, the input signals J and K have no restrictions, and the ternary JK flip-flop can be converted into a ternary D or ternary T flip-flop when it satisfies certain conditions. The designed circuits have simple structures, and can be realized by traditional Karnaugh maps. This approach offers a novel way to design multi-valued flip-flops of RTD circuits.

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