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A multimode digital controller IC for flyback converter with high accuracy primary-side feedback

Jian-ping QIU[†], Le-nian HE[†‡], Yu-lin WANG

(*Institute of Very Large Scale Integrated Circuits Design, Zhejiang University, Hangzhou 310027, China*)

[†]E-mail: {qiujp, helenian}@vlsi.zju.edu.cn

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Abstract: A digital controller IC for the flyback converter with primary-side feedback is proposed. The controller is used for adapter charger or LED driver applications. To obtain high accuracy for the primary-side feedback, a digital primary-side sensing technology is adopted, which can auto-track the knee point of the primary auxiliary winding voltage. Furthermore, an internal digital compensator eliminates the need for external loop compensation components while achieving excellent line and load regulation. The controller could output both constant voltage and constant current depending on the load current. Pulse width modulation and pulse frequency modulation are used in constant voltage mode while quasi-resonant control is used in constant current mode. The digital controller is validated by using FPGA.

Key words: Multimode, Digital control, Primary-side sensing, Quasi-resonant control, Constant voltage (CV), Constant current (CC), LED driver

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1 Introduction

Power management integrated circuits (ICs) have been studied for a long time. In early times, a simple input voltage feed forward control scheme was used to regulate the output voltage (Kazimierczuk and Massarini, 1997; Kazimierczuk and Starman, 1999; Weimer *et al*., 1999). To obtain more stability of the output voltage when its input or its load changes, an output voltage feedback control scheme has been widely used. Much research has been done on feedback control models (Erickson and Maksimovic, 2001; Bryant and Kazimierczuk, 2005a; 2005b; 2006; 2007; Kazimierczuk, 2008; Kondrath and Kazimierczuk, 2010; 2011; 2012). Traditionally analog control is used in these models. Digital control, which is a thriving control, is bringing more advantages, including insensitivity to parameter variation, programmability, and even fewer external components (Peterchev *et al*., 2003; Zhang and Maksimovic, 2010).

On the other hand, the accuracy of feedback is a key issue in feedback control schemes, whether analog control or digital control. In non-isolated power converters, such as buck, boost, or buck-boost, the output voltage could be fed back to the controller directly and accurately. But in some isolated power converters, such as flyback, the output voltage usually could not be fed back directly and then more attention should be paid to the output voltage feedback.

Flyback converters have been widely used in low power applications because of their simple structures, low cost, reduced components, and perfect isolation between input and output (Murthy and Kazimierczuk, 2005). Therefore, it is immensely beneficial to design a high accuracy feedback circuit for the flyback converter. Fig. 1 shows a traditional flyback converter in which an opto-coupler is used to feed back the output voltage without breaking the isolation between input and output. However, the current transfer ratio of the opto-coupler varies with temperature and time

‡ Corresponding author

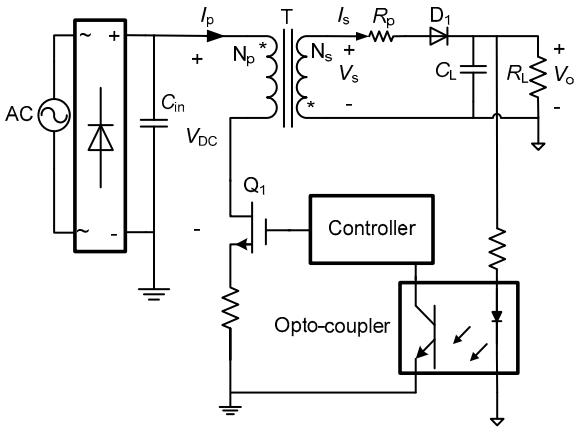

Fig. 1 Traditional flyback converter

(Sayani *et al*., 1988). In addition, integrating an opto-coupler into a chip is impractical. Another feedback technique called primary-side feedback was proposed by Zhang *et al*. (2005), Chang *et al*. (2009), Xiao *et al*. (2009), and Kang and Maksimovic (2012). The output voltage is sampled from the primary side at a fixed time while Q_1 is turned off (Zhang *et al*., 2005; Xiao *et al*., 2009). In this process, an error between the output and feedback voltage will be introduced by the voltage drop on the parasitic resister and the forward voltage of the output diode (Chang and Tzou, 2009). To achieve higher accuracy, Chang *et al*. (2009) proposed a solution which can eliminate the error attributed to the parasitic resister, while the error (usually hundreds of millivolts) due to the forward voltage of the diode still exists. A pipeline analog-to-digital converter (ADC) is applied to sample the voltage when the current of the secondary winding is nearly zero (Kang and Maksimovic, 2012). Though the feedback error is minimized, it will be influenced by the matching between the clock period of the pipeline ADC and the resonant period of the transformer. This resonant period is never the same in different applications. Moreover, implementing a pipeline ADC is costly.

Considering the widespread applications of flyback converters in adapter chargers, it is necessary to design converters that can output both constant voltage (CV) and constant current (CC). However, the converters proposed by Zhang *et al*. (2005), Chang *et al*. (2009), Xiao *et al*. (2009), Kang and Maksimovic (2012), and Zhang *et al*. (2012) could work only in either CV mode or CC mode. This paper presents a multimode digital controller for the flyback converter with a novel primary-side sensing (PSS) technology which achieves high accuracy. The controller operates in pulse width modulation (PWM) CV mode during normal load, while in pulse frequency modulation (PFM) CV mode during light load. If the load current is larger than the preset value, quasi-resonant controlled CC mode is adopted. The modes could automatically switch between each other depending on the load current.

2 Proposed digital controller

Primary-side feedback flyback with the proposed digital controller has been presented in Fig. 2, which is a high performance AC to DC power supply. The function block diagram of the digital controller is shown in Fig. 3. The novel PSS circuit consists of four comparators, a digital-to-analog converter (DAC), and a real-time waveform analyzer. The output of the PSS circuit is connected to the input of the CV control circuit, which contains a digital compensator, an on/off time calculator, and a digital PWM (DPWM). PWM_CV, which is the output pulse signal of the CV control circuit, is used to control the power switch Q_1 in PWM and PFM CV mode. In CC mode, Q_1 is regulated by PWM_CC, which is the output signal of the CC control circuit. An automatic mode switch module is used to determine the operation mode depending on the load current.

As shown in Fig. 4, the load current is the key parameter for deciding in which mode the converter

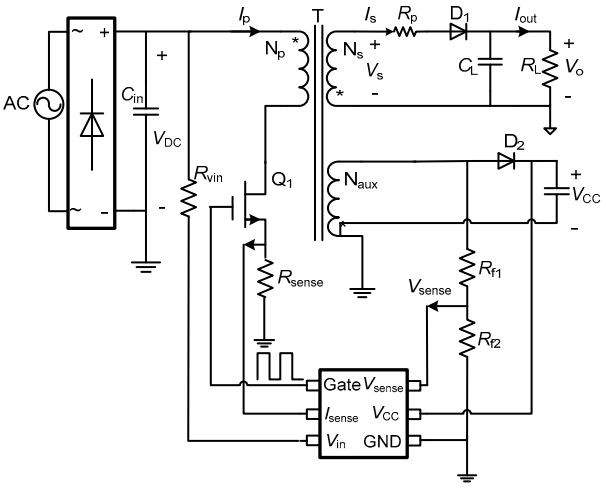

Fig. 2 Primary-side feedback flyback with the proposed digital controller

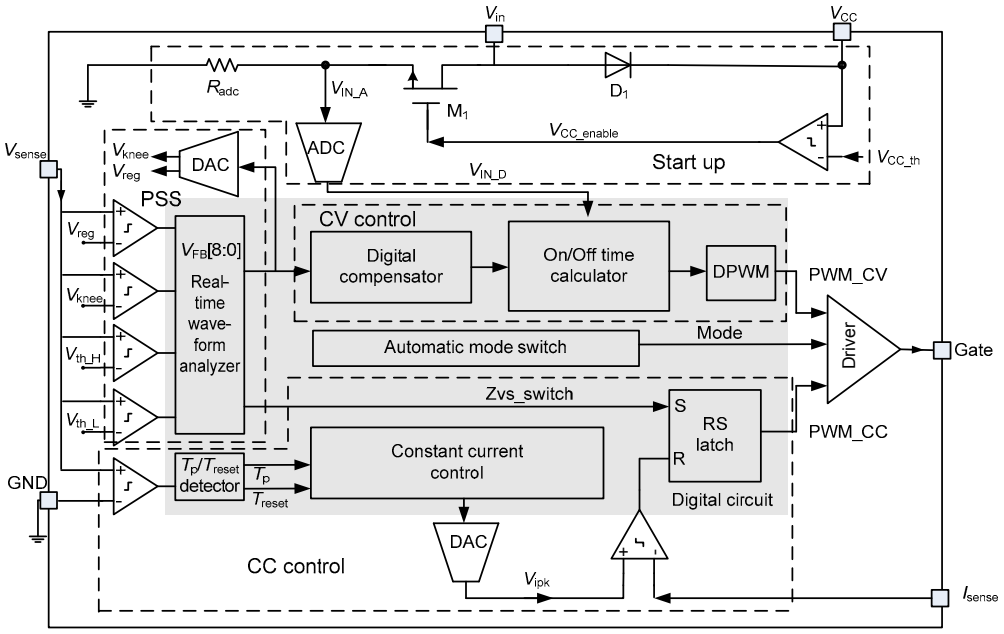

Fig. 3 Function block diagram of the controller

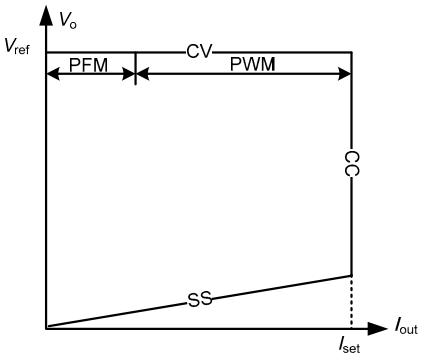

Fig. 4 Operation mode of the controller

will be operating. When powered on, the converter will operate in soft start (SS) mode first. In SS mode, the on-time of the power switch Q_1 is limited. If the load current is less than the preset current I_{set}, the converter will operate in PWM or PFM CV mode and the output voltage is regulated to a preset reference voltage V_{ref}. Otherwise, it will operate in CC mode and the output current will be regulated to I_{set}.

During CV operation, the converter will operate in PWM CV mode unless the load current is less than 5% of the maximum current; in this circumstance PFM CV mode will be applied to improve the efficiency. In CC mode, quasi-resonant control is adopted to minimize the electro magnetic interference (EMI) and switching loss.

3 Principle of operation

In this section the detailed principle of the proposed digital controller will be analyzed.

3.1 Principle of start up

When power turns on, V_{in} will charge V_{cc} through the diode between them (Fig. 3). When V_{cc} is charged to a voltage higher than the start-up threshold V_{cc_th}, the V_{cc_enable} signal will enable the digital controller. At the same time, the MOSFET M_1 will turn on and the ADC will start to convert the input voltage.

3.2 Novel primary-side sensing

The primary-side sensing technology aims to feed back a highly accurate output voltage signal by sensing the voltage at the primary auxiliary winding (Fig. 2). When the flyback converter operates in discontinuous conduction mode (DCM), the switch Q_1 will not turn on until the current through the secondary winding becomes zero. Fig. 5 shows some key waveforms. Here one switch cycle can be divided into three intervals named T_1, T_2, and T_3.

During T_1, Q_1 is turned on to make the transformer store energy at the primary-side winding. In this interval,

$$V_{sense} = -\frac{R_{f2}}{R_{f1}+R_{f2}}\frac{N_{aux}}{N_p}V_{DC}, \quad (1)$$

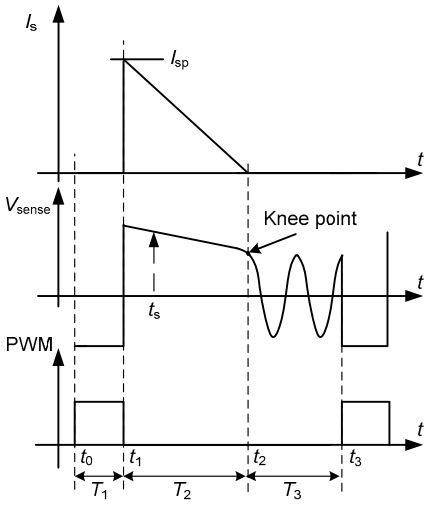

Fig. 5 Operation waveforms of the flyback

where N_p and N_{aux} mean the winding turns of primary-side winding and auxiliary winding, respectively.

During T_2, Q_1 is turned off to let the energy translate from the primary side to the secondary side. The current of the secondary winding I_s will rapidly rise to a peak current I_{sp} and then decrease to zero gradually. In this interval,

$$V_{sense}(t)=\frac{R_{f2}}{R_{f1}+R_{f2}}\frac{N_{aux}}{N_s}(V_o+V_D+I_sR_p), \quad (2)$$

where V_D is the forward voltage of the output diode D_1, R_p is the parasitic resistor of the secondary side winding, and V_o is the output voltage.

During interval T_3, I_s has decreased to zero, which means the energy stored in the transformer has been reset to zero. But there is still energy stored in the drain-source capacitance of transistor Q_1. This energy then resonantly oscillates with the magnetizing inductance of the primary-side winding at a resonant frequency determined by the capacitance and inductance values.

According to Eq. (2), if the controller senses the voltage at moment t_s during T_2, the feedback voltage will contain an error voltage compared to the output voltage, as given by (Chang and Tzou, 2009)

$$V_{error}=\frac{R_{f2}}{R_{f1}+R_{f2}}\frac{N_{aux}}{N_s}(V_D+I_sR_p). \quad (3)$$

This error voltage decreases as current I_s decreases.

However, at t_2 when I_s has reached zero, the forward voltage of the output diode and voltage drop on the parasitic resistor also decrease to zero. This moment is well known as the knee point, and then

$$V_{sense}(t_2)=\frac{R_{f2}}{R_{f1}+R_{f2}}\frac{N_{aux}}{N_s}V_o. \quad (4)$$

If the knee point can be sampled precisely, the primary-side sensing can also achieve high accuracy.

Thus, a novel PSS technology is designed to auto-track the knee point and to accurately convert this knee point voltage into a digital signal. The technology could be implemented as shown in Fig. 6, consisting of a DAC, four comparators, and a real-time waveform analyzer. This PSS circuit will track the knee point of V_{sense} and convert this analog voltage to a nine-bit digital signal V_{FB}. Also, V_{FB} is fed back to V_{sense} to detect whether this V_{FB} is accurate.

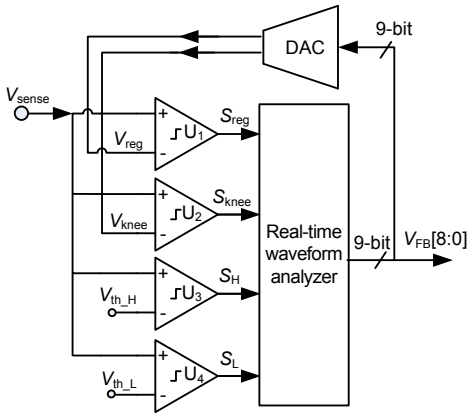

Fig. 6 The proposed primary-side sensing circuit

As Fig. 6 shows, four parallel comparators are connected to V_{sense}. U_3 and U_4 have fixed reference voltages V_{th_H} and V_{th_L}, which are the maximum and minimum limitations of the detectable V_{sense}, respectively. The voltages V_{reg} and V_{knee} are fed back from V_{FB}. There is a constant gap ΔV between them, as given by

$$V_{knee}=\frac{V_{FB}}{511}V_{ref\_DAC}, \quad (5)$$

$$V_{reg}=V_{knee}+\Delta V, \quad (6)$$

where V_{ref_DAC} is the reference voltage of the DAC. In this design a simple voltage scaling based DAC is used, and the reference is set to be 1.0 V.

S_{reg} and S_{knee} are used for knee point tracking. Three typical waveforms of S_{reg} and S_{knee} are shown in Fig. 7. Because the slope of V_{sense} is apparently

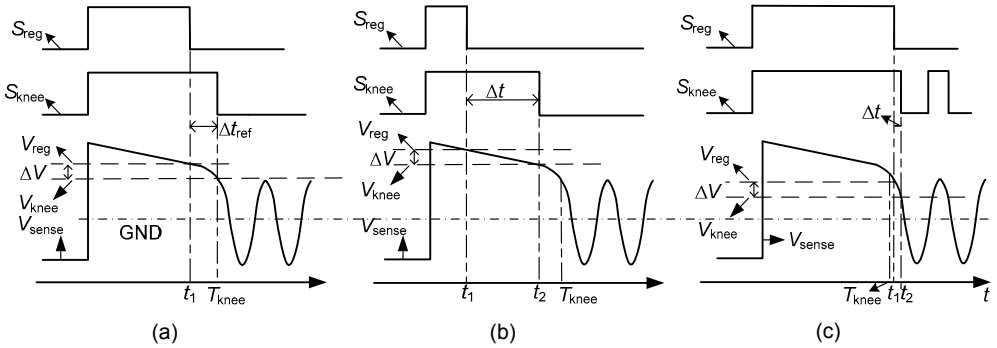

Fig. 7 Operation waveforms of the proposed primary-side sensing circuit
(a) V_{FB} is equal to the knee point voltage; (b) V_{FB} is too large; (c) V_{FB} is too small

different before and after the knee point, a constant ΔV between V_{reg} and V_{sense} will result in a totally different Δt. If V_{knee} is larger than the knee point voltage, then Δt will be large (Fig. 7b). If V_{knee} is smaller than the knee point voltage, then Δt will be small (Fig. 7c). Only when the detected $\Delta t=\Delta t_{ref}$, is the V_{knee} the knee point voltage (Fig. 7a). In general, ΔV and Δt_{ref} are determined by the forward voltage and recovery time of the output diode, respectively.

To catch the knee point as precisely as possible, the real-time waveform analyzer will analyze S_{reg} and S_{knee} every cycle (Fig. 8).

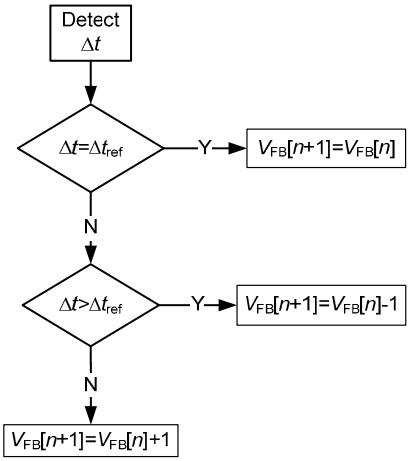

Fig. 8 Real-time waveform analyzer

At the beginning, V_{FB} and Δt_{ref} are set to default values, respectively. V_{FB} will be refreshed according to the detected Δt during every switching cycle.

If $\Delta t=\Delta t_{ref}$, which means that the V_{FB} signal equals the knee point voltage, then in the next switching cycle,

$$V_{FB}[n+1]=V_{FB}[n], \tag{7}$$

where $V_{FB}[n]$ means the V_{FB} at the nth cycle.

If $\Delta t>\Delta t_{ref}$, which means that the V_{FB} signal is too large, then in the next switching cycle,

$$V_{FB}[n+1]=V_{FB}[n]-1. \tag{8}$$

If $\Delta t<\Delta t_{ref}$, which means that the V_{FB} signal is too small, then in the next switching cycle,

$$V_{FB}[n+1]=V_{FB}[n]+1. \tag{9}$$

After several switching cycles, the knee point voltage can be sensed.

3.3 Digital constant voltage operation

The proposed digital constant voltage operation has been implemented as shown in Fig. 9. First, an error signal between V_{FB} and the reference V_{ref_D} is calculated and input to a digital compensator. The digital compensator operates as an analog error amplifier. In this study a digital PI compensator is adopted (Fig. 9). The design details of the digital compensator have been described in Lin *et al*. (2011). The digital PI compensator follows

$$P[n]=k_a e[n]-k_b e[n-1]+P[n-1], \tag{10}$$

$$e[n]=V_{ref\_D}-V_{FB}[n], \tag{11}$$

where k_a and k_b are the compensator parameters, $P[n]$ is output of the digital compensator at the nth cycle, $e[n]$ is the error of V_{FB} at the nth cycle, and $P[n-1]$, $e[n-1]$ mean the values at the previous cycle. Here V_{ref_D} is a nine-bit digital value; in this work, V_{ref_D} is set to be 380.

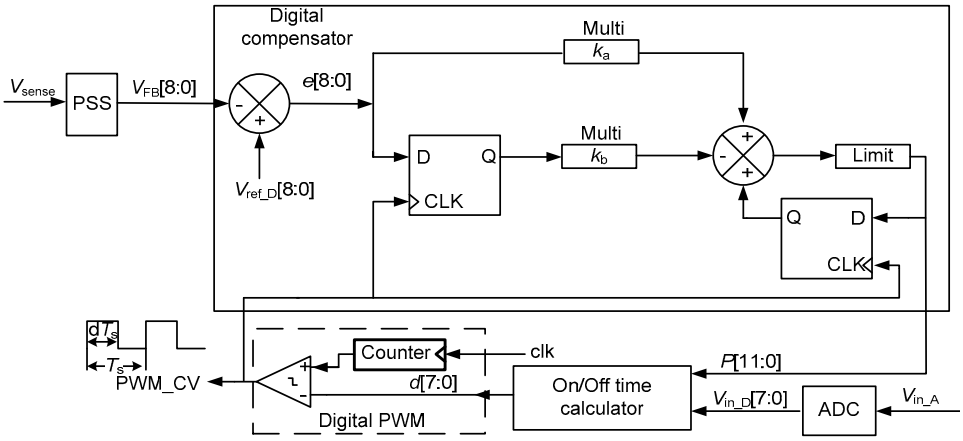

Fig. 9 Function diagram of digital constant voltage control

The output of the digital compensator is used to calculate the duty of the PWM_CV, which will be output to control Q_1 in PWM and PFM CV mode, as given by

$$d[n]=\frac{k_1(P[n]-k_2)}{V_{\text{in\_D}}[n]}, \tag{12}$$

where k_1 and k_2 are constant, and the frequency of the PWM_CV is fixed to 40 kHz. $V_{\text{in\_D}}$ means the input voltage of the flyback and is introduced into the calculation of the duty cycle so as to implement the input voltage feed forward (IVFF) control. The benefits of IVFF are well known (Calderone *et al*., 1992; Arbetter and Marksimovic, 1997; Kazimierczuk and Massarini, 1997; Kazimierczuk and Starman, 1999). It is effective in reducing the effect of source disturbances on converter outputs and improving steady-state and dynamic responses.

An 8-bit counter based digital PWM module (Syed *et al*., 2004) takes the digital value $d[n]$ and produces the pulsating waveform PWM_CV. The counter needs a high frequency clock. In this work, the frequency of PWM_CV is 40 kHz, and thus a 10 MHz clock is needed.

Eqs. (10)–(12) show two facts. First, when the output voltage is lower than the reference, $P[n]$ will get larger and larger in every switching cycle. Second, $P[n]$ is directly proportional to the load current at the same input voltage, because larger load current means larger duty. So, we can detect the load voltage or current by detecting $P[n]$. These can be used to automatically switch modes.

On the other hand, the controller will operate in PFM CV mode during light load. Thereafter, the on-time (T_{on}) of PWM_CV will be modulated by the line voltage and the off-time (T_{off}) by the load current:

$$T_{\text{on}}[n]=\frac{P_{\text{pfm}}}{V_{\text{in\_D}}[n]}, \tag{13}$$

$$T_{\text{off}}[n]=\frac{K_{\text{pfm}}}{P[n]}, \tag{14}$$

where P_{pfm} and K_{pfm} are constant parameters.

3.4 Digital constant current operation

The constant current mode is useful in battery charging or LED driver applications. This controller automatically switches to CC mode when the load has reached the preset current I_{set} as shown in Fig. 4. To achieve constant current, the controller senses the load current indirectly through the primary-side current. The primary-side current is detected by the I_{sense} pin through a resistor R_{sense} from the MOSFET source to ground, as shown in Fig. 2. Fig. 10 shows the waveforms when the controller operates in CC mode. When I_{sense} reaches V_{ipk}, the PWM_CC will be zero and output to shut down the MOSFET Q_1. The peak voltage V_{ipk} is calculated cycle by cycle as follows.

According to Fig. 10, the output current I_{out} is the average of the current I_{s} throughout the secondary side winding. Then

$$I_{\text{out}}=\frac{1}{2}I_{\text{s\_peak}}\frac{T_{\text{r}}}{T_{\text{p}}}, \tag{15}$$

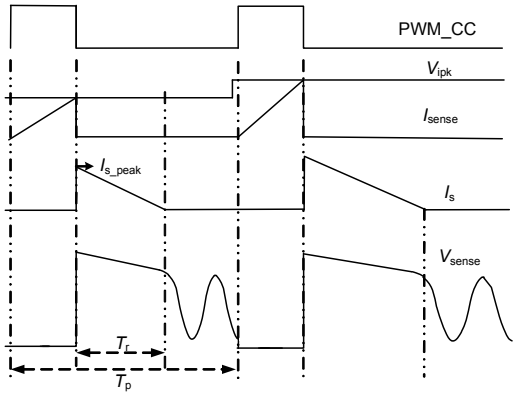

Fig. 10 Operation waveforms in constant current (CC) mode

where I_{s_peak} is the peak current of I_s, T_r is the reset time of the transformer, and T_p is the period of the PWM_CC, which can be found in Fig. 10. However, the I_{s_peak} is translated from the primary-side current:

$$I_{s\_peak} = \frac{N_p}{N_s}\frac{V_{ipk}}{R_{sense}}. \tag{16}$$

Thus, the V_{ipk} can be calculated as

$$V_{ipk} = \frac{2I_{out}R_{sense}N_s}{N_p}\frac{T_p}{T_r}. \tag{17}$$

According to Eq. (17), if T_p, T_r, N_s, N_p, and R_{sense} are all detectable, then I_{out} can be regulated by controlling the V_{ipk}. In this design, we set V_{ipk_ref} to 0.294 V, where

$$V_{ipk\_ref} = \frac{2I_{out}R_{sense}N_s}{N_p}. \tag{18}$$

The real-time waveform analyzer will detect the T_p and T_r of V_{sense} cycle by cycle. Then, the peak voltage can be calculated using Eq. (17).

However, different applications may need different preset currents, and the user can adjust the R_{sense}, N_p, or N_s to obtain a different current. For example, if we set N_p=100, N_s=10, and R_{sense}=0.7 Ω, considering the efficiency is 100%, then the default constant current will be 2.1 A. As the load current reaches 2.1 A, the system will automatically switch to CC mode.

To reduce EMI and switching losses, this design employs quasi-resonant control during CC mode. In quasi-resonant control, the MOSFET Q_1 is turned on at the point where the resonant voltage of V_{sense} is at its lowest point (Fig. 10).

3.5 Automatic mode switching

Fig. 4 illustrates that the converter operates in four modes: SS, CC, PWM CV, and PFM CV. To simplify system operation, an automatic load dependent mode switching is desirable (Fig. 11).

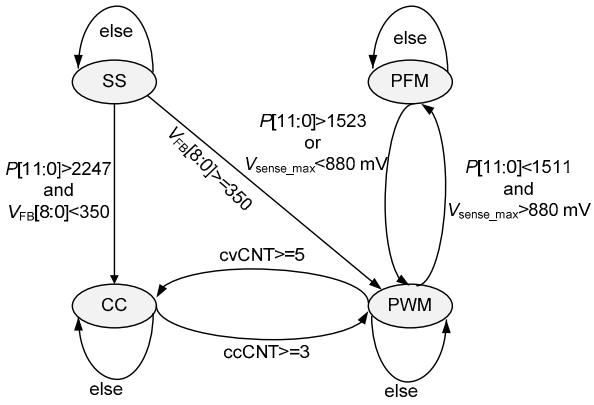

Fig. 11 Automatic mode switching

As shown in Fig. 4, first the converter will operate in SS mode when powered on, and operate in CC mode if the load current reaches the preset current I_{set}; otherwise, it will operate in PWM CV or PFM CV mode.

In SS mode, the converter operates at a fixe frequency of 40 kHz, and the on-time of every switching cycle is limited by

$$T_{on} = \min\left(\frac{M}{4}T_{on\_max},\ T_{on\_c}\right), \tag{19}$$

where T_{on_max} is the preset maximum on-time limitation of the converter, T_{on_c} is the on-time of PWM_CV calculated according to Eq. (12), and M is countered from 1 to 4 with a period of 400 μs.

In SS mode, if the output voltage is charged close to the reference, which means V_{FB} is larger than 350, the mode will switch to PWM CV. If the output of the digital compensator is larger than a threshold, which means the load current is very large, the mode will switch to CC. In this design the threshold is the preset maximum value of $P[n]$, which is set to be 2247.

In CV mode, the output voltage is regulated against different load currents. If the load current is lower than 5% of the maximum current, the converter operates in PFM CV mode. Otherwise, it operates in PWM CV mode. Because $P[n]$ is directly proportional to the load current, a threshold value of $P[n]$ is set, at which the load current is 5% of the maximum current. In this work this threshold is set to be 1511. If the detected value of $P[n]$ is less than this threshold value, then the system will switch to PFM mode. Also, to improve load response, the maximum value of the auxiliary winding voltage $V_{\text{sense\_max}}$ is detected. If $V_{\text{sense\_max}}$ is lower than a threshold voltage, which means the output voltage is very low, then the converter could not switch to PFM mode, and the output voltage will be charged up quickly in PWM mode. A hysteresis is employed when the mode is switched from PFM CV to PWM CV.

In PWM CV mode, the peak voltage of I_{sense} is directly proportional to load current. Meanwhile, the controller calculates a reference voltage V_{ipk} every switching cycle according to Eq. (17). If the peak of I_{sense} is equal to V_{ipk}, the load current is equal to the preset current I_{set}. If the peak of I_{sense} keeps being above V_{ipk} for five switching cycles, the mode will switch to CC. There is a counter cvCNT to detect this event.

In CC mode, the output voltage is charged up with a constant current I_{set}. If the voltage is charged up to the reference voltage, the converter should switch to PWM CV mode. This is necessary in a charger application. As soon as the output voltage has been charged up to the reference voltage, the output of the digital compensator will decrease. If the converter keeps operating in CC mode, the duty of PWM_CV calculated using Eq. (11) will decrease rapidly. At the same time the on-time of PWM_CC will keep increasing. Therefore, the converter will automatically switch from CC mode to CV mode, if the on-time of PWM_CV keeps being less than the on-time of PWM_CC for three switching cycles. There is a counter ccCNT to detect this event.

4 Simulation and experimental results

The digital circuit in Fig. 3 was implemented with Verilog HDL. A flyback converter as shown in Fig. 2 was used to test the controller. The proposed design was simulated in a Cadence environment. Moreover, the controller was implemented with a field-programmable gate array (FPGA). This section will present both simulation and experimental results.

First the controller was simulated in Cadence software. The constant current I_{set} was set to 2.1 A, and the reference output voltage was set to 4.79 V. The load resistor translated between 1.5 and 5.0 Ω. Theoretically, the converter should operate in SS mode first, and switches to CC mode if the load resistor is 1.5 Ω. If the load resistor is 5.0 Ω, the operation mode should be PWM CV. Fig. 12 proves this mode switching between CC and PWM CV.

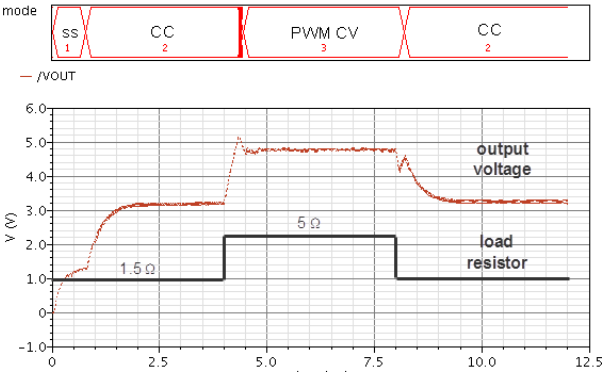

Fig. 12 Mode switching between CC and PWM

Fig. 13 shows the mode switching between PWM and PFM CV. The load resistor translated between 5.0 and 50 Ω.

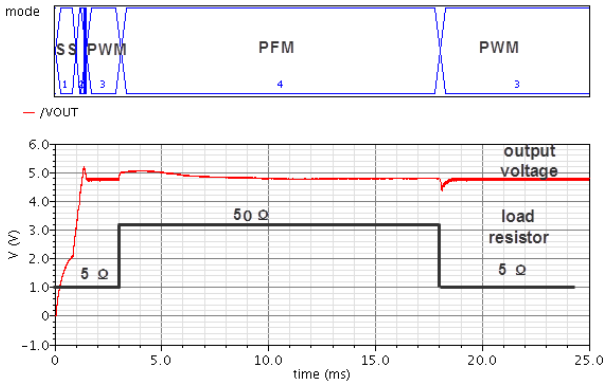

Fig. 13 Mode switching between PFM and PWM

The simulation results showed that the controller operates as well as the theoretical design. Then the digital circuit was synthesized to a NEXYS3

(Digilent, USA) FPGA. Cooperating with DAC900 (TI, USA), ADC08200 (TI, USA), and LMV762 (TI, USA), the digital controller has been implemented as shown in Fig. 14. A flyback converter as shown in Fig. 2 can be used to evaluate the performance of the digital controller, such as primary-side sensing, quasi-resonant control, and CV or CC operation.

Fig. 14 Test board of the proposed controller

The primary-side feedback voltage is as shown in Fig. 15, where 'Gate' means the control signal of Q_1. The feedback voltage V_{fb} is right at the knee voltage of V_{sense}. According to Eq. (4), at the knee point, the sense error voltage is zero. Zhang *et al*. (2005) and Xiao *et al*. (2009), however, sensed the feedback voltage at a fixed sampling time during the reset time of the transformer. When the sampling time was set at T_{sample} (Fig. 15), the sense error voltage was 200 mV. This error voltage is caused by the parasitic resistor and the output diode. Chang *et al*. (2009) tried to eliminate the error voltage caused by the parasitic resistor, but the forward voltage of the output diode still caused an error. Adopting Chang *et al*. (2009)'s technology in our design, the error voltage was 109 mV (Eq. (3)). A pipeline ADC was used by Kang and Maksimovic (2012) to sense the knee point voltage. However, the accuracy is very sensitive to the resonant frequency of the transformer. A high speed pipeline ADC also means a large cost. In our design, however, only a simple voltage scaling DAC is needed. The experimental results proved that the primary-side sensing technology proposed in this study can auto-track the knee point and minimize the sensing error.

Table 1 gives the output voltage and operation mode against different loads. Here the preset current was 0.5 A, and the reference output voltage 5.68 V. Taking advantage of high accuracy primary-side sensing technology, the output voltage was tightly regulated to the reference voltage during PWM and

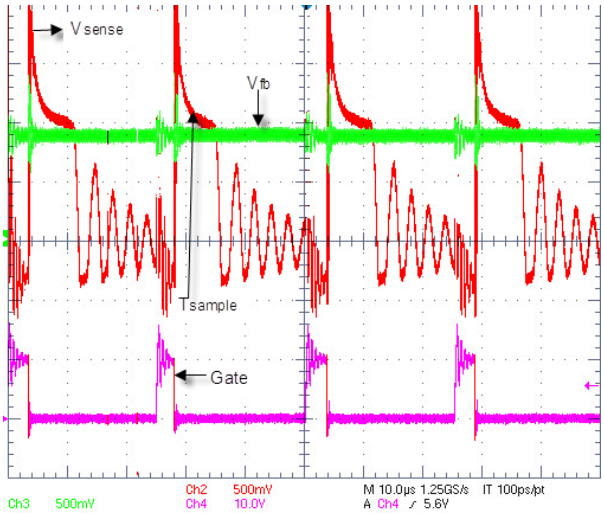

Fig. 15 Primary-side feedback voltage

Table 1 Output voltage and operation mode against different loads

R_L (Ω)	V_o (V)	Load (A)	Mode
100.0	5.68	0.057	PFM
20.0	5.64	0.282	PWM
17.6	5.60	0.318	PWM
14.0	5.60	0.400	PWM
11.0	5.55	0.500	CC
7.9	4.00	0.506	CC
4.4	2.20	0.500	CC

PFM CV modes. However, there is still an error voltage between the actual output voltage V_o and reference voltage V_{ref}. The sensing error can be calculated as

$$V_e = \frac{R_{f2}}{R_{f1}+R_{f2}}\frac{N_{aux}}{N_s}(V_{ref}-V_o). \quad (20)$$

In the tested flyback converter,

$$\frac{R_{f2}}{R_{f1}+R_{f2}}\frac{N_{aux}}{N_s}=0.157. \quad (21)$$

During PFM and PWM CV modes, the maximum sensing error was 12.48 mV, while it was 109 mV using Chang *et al*. (2009)'s design. The error is caused by the quantization of the DAC and the clock in the PSS circuit. More accurate DAC and clock can reduce the error.

Table 1 also shows that the controller operated in different modes against different loads, as described in Section 3.5. In CC mode, the current was well regulated to the preset current.

Fig. 16 evaluates the quasi-resonant control. The power MOSFET Q_1 was turned on at the valley of the resonant where the drain-source voltage of Q_1 was the minimum. The inrush current of Q_1 will be minimized, and thus the switching power loss and EMI can be minimized.

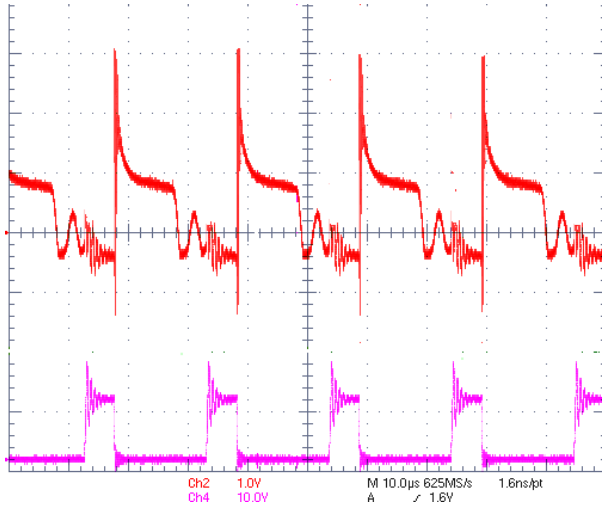

Fig. 16 Quasi-resonant control

5 Conclusions

We propose a high performance flyback converter controller, in which digital control technology is used to build both CV and CC supplies. It can be used in AC-DC chargers for cell phones and LED drivers. The output voltage is fed back through a high accuracy primary-side sensing technology without any isolated feedback circuit. According to the test results, the maximum sensing error is 12.48 mV, about 11% of the normal sensing error. An internal digital compensator regulates the output voltage according to the feedback voltage. In CC mode, the output current is regulated based on the primary-side current without any isolated circuit. Compared to a traditional flyback controller, the proposed controller has such advantages as high accuracy primary-side feedback, simple external components, and simple design of controller IC.

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