Journal of Zhejiang University-SCIENCE C (Computers & Electronics)
ISSN 1869-1951 (Print); ISSN 1869-196X (Online)
www.zju.edu.cn/jzus; www.springerlink.com
E-mail: jzus@zju.edu.cn

Ka-band ultra low voltage miniature sub-harmonic resistive mixer with a new broadside coupled Marchand balun in 0.18-μm CMOS technology*

Ge-liang YANG†, Zhi-gong WANG†‡, Zhi-qun LI, Qin LI, Fa-en LIU, Zhu LI

(*Engineering Research Center of RF-ICs and RF-Systems, Ministry of Education, Southeast University, Nanjing 210096, China*)

†E-mail: yglamen@gmail.com; zgwang@seu.edu.cn

Received Dec. 22, 2012; Revision accepted Mar. 13, 2013; Crosschecked Mar. 23, 2013

Abstract: A Ka-band sub-harmonically pumped resistive mixer (SHPRM) was designed and fabricated using the standard 0.18-μm complementary metal-oxide-semiconductor (CMOS) technology. An area-effective asymmetric broadside coupled spiral Marchand balance-to-unbalance (balun) with magnitude and phase imbalance compensation is used in the mixer to transform local oscillation (LO) signal from single to differential mode. The results showed that the SHPRM achieves the conversion gain of −15–−12.5 dB at fixed f_{IF}=0.5 GHz with 8 dBm LO input power for the radio frequency (RF) bandwidth of 28–35 GHz. The in-band LO-intermediate freqency (IF), RF-IF, and LO-RF isolations are better than 31, 34, and 36 dB, respectively. Besides, the 2LO-IF and 2LO-RF isolations are better than 60 and 45 dB, respectively. The measured input referred P1dB and 3rd-order inter-modulation intercept point (IIP3) are 0.5 and 10.5 dBm, respectively. The measurement is performed under a gate bias voltage as low as 0.1 V and the whole chip only occupies an area of 0.33 mm^2 including pads.

Key words: Complementary metal-oxide-semiconductor (CMOS), Sub-harmonically pumped resistive mixer (SHPRM), Marchand balance-to-unbalance (balun), Millimeter wave (MMW), Monolithic microwave integrated circuit (MMIC)
doi:10.1631/jzus.C1200369 **Document code:** A **CLC number:** TN4

1 Introduction

With the rapid development of wireless communication, the millimeter wave (MMW) technology has achieved a significant progress due to its compensation for the spectrum blockage in industrial, scientific, and medical (ISM) band up to 10 GHz and satisfaction to the increasing requirements for higher data-rate transmission. Traditionally, monolithic MMW integrated circuits (ICs) have been fabricated using III/V compound semiconductor technologies due to their higher electron mobility and less substrate loss than previous complementary metal-oxide-semiconductor (CMOS) technologies (Barker *et al*., 1984; Yeh *et al*., 2005). CMOS process is particularly attractive for its low cost, low power, and enabling of integration with base-band ICs. As the CMOS device continuously scales down to the deep sub-micrometer regime, the cut-off frequency f_T already catches up with and even exceeds that of III/V technologies. Practically, the improved modern CMOS technology has been certified feasible to render the MMW circuitry (Sun *et al*., 2011; Wang *et al*., 2011).

Among the building blocks in MMW front-end, the mixer plays a dominant role in translating the radio frequency (RF) signals to the intermediate freqency (IF) band in a receiver, or vice versa in a transmitter. Various solutions have been demonstrated viable for the mixer design. Active mixers, well-known for the Gilbert structure, can provide higher conversion gain and better noise performance and occupy a smaller chip area, but with the drawback of high DC power consumption. Passive mixers offer

‡ Corresponding author

* Project supported by the National Basic Research Program (973) of China (No. 2010CB327404), the National High-Tech R&D Program (863) of China (No. 2011AA10305), and the National Natural Science Foundation of China (No. 60901012)

better linearity without DC power consumption, but suffer from higher conversion loss. Sub-harmonic passive mixers, with advantages of not only requiring half-frequency local oscillation (LO) sources, but also preventing the self-mixing problem, have attracted much interest over the last ten years. Previously, the anti-parallel diode pair (APDP) topology was supposed to be efficient for the sub-harmonic mixers design (Lin CH *et al*., 2007; Lin CM *et al*., 2009). Both mixers have a wide operation band but they all suffer from bad LO-RF isolations; moreover, the output spectrum will also suffer from undesired distortions because the diodes are intrinsically unideal.

In this work, a sub-harmonic mixer was designed from another point of view. The mixer core is composed of two parallel transistors that are gate-pumped by equal amplitude but anti-phase LO signals. Accordingly, a balance-to-unbalance (balun) is needed to realize the single to differential transformation for such LO signals. For compactness consideration, a novel asymmetric broadside coupled spiral structure with magnitude and phase imbalance compensation is used for the balun design. Consequently, a sub-harmonically pumped resistive mixer (SHPRM) employing the aforementioned Marchand balun is proposed and its building blocks are presented. Finally, the experimental results and discussions are provided.

2 Implementation and verification of the asymmetric broadside coupled spiral Marchand balun

Balun, which splits the single-ended signal into two signals of equal amplitude but 180° out of phase, plays an important role in balanced circuits. Generally, a balun can be realized by active or passive ways. The active baluns pose the fundamental limits for high frequency operations, and additionally, they consume extra DC power. Thus, the passive baluns, which exploit the power coupling of the transmission lines, become suitable candidates. The structures of lateral coupling have been widely investigated (Yu *et al*., 2007; Xu *et al*., 2009) and already been employed for the monolithic circuit design (Wei *et al*., 2008). However, all of these baluns are commonly not small enough for a compact application. To take advantage of the multilayer metallization of the CMOS process, the broadside coupled structure provides more facilities and flexibilities when compactness is taken into consideration. A symmetric broadside coupled Marchand balun has been proposed with the measured magnitude and phase imbalance of less than 0.5 dB and 1° from 8.7 to 17.4 GHz (Chiang *et al*., 2010). However, its insertion loss is as high as 7.4 dB. In contrast to the symmetric arrangement, an asymmetric broadside coupled balun was demonstrated and it featured a relatively low insertion loss of 4.1 dB at the frequency of 37.5 GHz (Chiou *et al*., 2007). Nevertheless, Chiou *et al*. (2007) proclaimed that the meandered structure will take up more than 0.06 mm^2 chip area when the center frequency is shifted down to lower than 20 GHz.

To realize an area-effective balun with wideband, low loss, and high balance characteristics, an asymmetric broadside coupled spiral structure is used for our design. Fig. 1a shows a 3D visualization of the proposed balun. Note that an extra metal line is needed to connect two sections of the balun. As discussed in Xu *et al*. (2009) and Chiang *et al*. (2010), this extra connecting line will degrade the balun's performance in terms of magnitude and phase balance. Fig. 1b schematically describes the proposed balun. The scattering matrices of each part are given by

$$\boldsymbol{S}_{\text{section1}}=\begin{bmatrix} -y^2/z^2 & x/z & -xy/z^2 \\ x/z & 0 & y/z \\ -xy/z^2 & y/z & -x^2/z^2 \end{bmatrix}, \tag{1}$$

$$\boldsymbol{S}_{\text{section2}}=\begin{bmatrix} \dfrac{x^2}{y^2+z^2} & \dfrac{y^3+yz^2-x^2y}{z(y^2+z^2)} \\ \dfrac{y^3+yz^2-x^2y}{z(y^2+z^2)} & -\dfrac{x^2}{y^2+z^2} \end{bmatrix}, \tag{2}$$

$$\boldsymbol{S}_{Z_1}=\begin{bmatrix} 0 & \mathrm{e}^{-\mathrm{j}\theta_1} \\ \mathrm{e}^{-\mathrm{j}\theta_1} & 0 \end{bmatrix}, \tag{3}$$

where $x=\sqrt{1-k^2}$, y=j$k$sinθ, z=$\sqrt{1-k^2}\cos\theta+\mathrm{j}\sin\theta$, and k is the coupling coefficient.

According to Eqs. (1)–(3), the scattering matrix of the balun was derived as

$$\boldsymbol{S}_{\text{balun}}=\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix}, \tag{4}$$

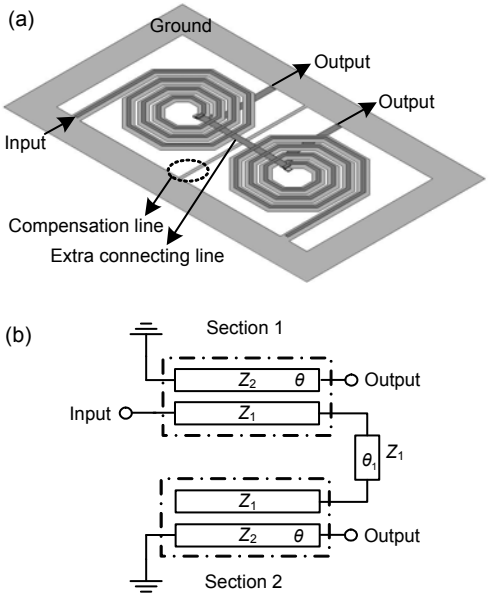


Fig. 1 Proposed broadside coupled Marchand balance-to-unbalance (balun) with an extra connecting line: (a) 3D visualization; (b) schematic diagram

Both coupling sections of the balun have the equal electrical length θ. θ_1 is the electrical length of the connecting line. The characteristic impedances of the primary and secondary spirals are Z_1 and Z_2, respectively

where S_{21} and S_{31} are the key elements useful for describing the performance of the balun and they are given by

$$\begin{cases} S_{21} = \dfrac{yx^3 e^{-2j\theta_1} - xyz^2 - xy^3}{z^2(y^2+z^2)}, \\ S_{31} = -\dfrac{(yx^3 - xyz^2 - xy^3)e^{-j\theta_1}}{z^2(y^2+z^2)}. \end{cases} \tag{5}$$

As illustrated in Eq. (5), there will be $S_{21}=-S_{31}$ when $\theta_1=0$. Otherwise, S_{21} and S_{31} are no longer of equal amplitude and 180° out-of-phase, which leads to a deteriorated balun performance. In this case, the solutions to the problem demand an in-depth analysis.

The scaling factor θ_1 is known as

$$\theta_1 = \beta l = 2\pi f\sqrt{LC}l, \tag{6}$$

where β is the propagation constant, f is the operating frequency, l is the physical length of the line, and L and C are the frequency-dependent self-inductance and the self-capacitance per unit of the line, respectively.

Considering Eq. (5) along with Eq. (6), we can find that the magnitude and phase imbalance can be optimized by decreasing L. It is well-known that the inductance of an inductor would decrease if the grounded metal lines were placed under the spiral coil. Accordingly, in this case, an orthogonal grounded metal line is placed under the extra connecting line as shown in Fig. 1a. From another point of view, the introduced compensation line plays a critical role in separating the balun into two independent parts. Thus, the coupling between two unbalanced ports is constrained to offer the better balun performance. To verify the practicality of the idea, baluns configured with and without the orthogonal grounded line are simulated in Agilent's ADS Momentum. Fig. 2 shows the simulated results in terms of the insertion loss (S_{21}) and the magnitude and phase imbalances. In the intended band of 13–20 GHz, the balun's magnitude and phase imbalances are compensated when the orthogonal grounded line is employed.

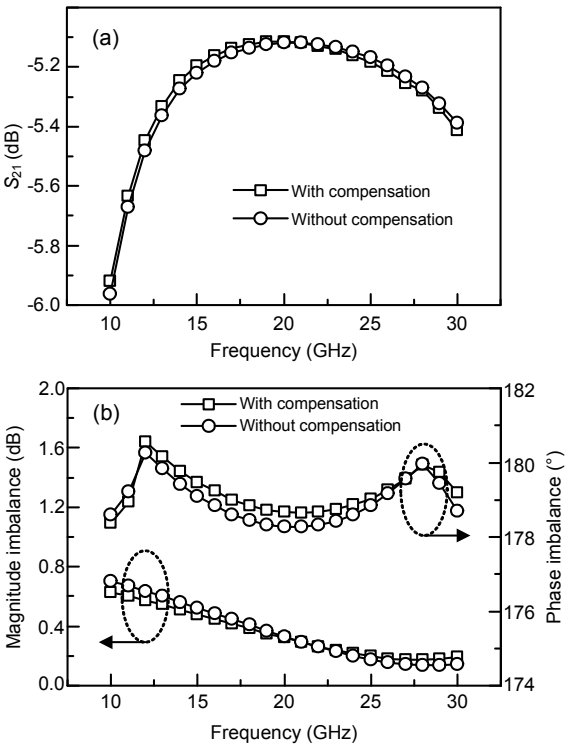
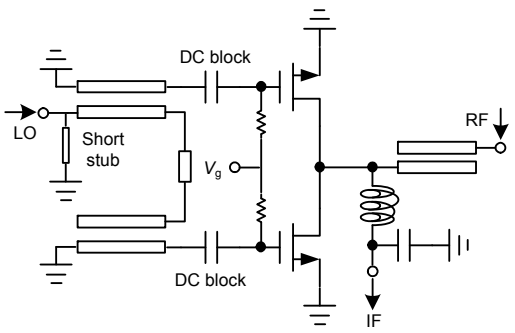


Fig. 2 Simulated results comparison of baluns with and without compensation

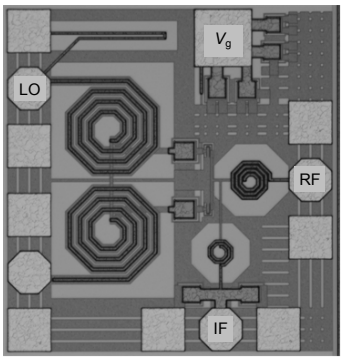
(a) Magnitude of S_{21}. The simulated S_{31} curves are not shown here because they can be derived from their respective magnitude imbalance curves. (b) Magnitude and phase imbalances

In the range of frequency over 20 GHz, the compensating line introduces a slight magnitude imbalance, but it remains offering better phase balance. Since the magnitude imbalance in decibels is defined as $20\lg(|S_{21}/S_{31}|)$ whose value is decided by S_{21} alone, the variation of θ_1 cannot affect the value according to Eq. (5). At elevated frequencies, the stray capacitance brought by the compensating line in conjunction with C dominates the tendency of S_{21}. This is the reason why a slight magnitude imbalance is introduced at frequencies beyond 20 GHz. On the other hand, both phases of S_{21} and S_{31} are θ_1-dependent. Thus, the absolute value of $|\angle(S_{21}/S_{31})|$, which is defined as the phase imbalance, guarantees the effectiveness of the compensation even if high frequencies are concerned.

So far, an asymmetric broadside coupled spiral Marchand balun has been designed using the magnitude and phase imbalance compensating technique. The simulated results show that the balun features an insertion loss of 5.1–5.4 dB from 13 to 30 GHz. Additionally, the magnitude and phase imbalances are less than 0.55 dB and 1.5°, respectively. Finally, it is worth mentioning that the proposed balun only occupies a core area of 164 μm×361 μm.



(a)



(b)

Fig. 3 Schematic diagram (a) and chip photograph (b) of the sub-harmonically pumped resistive mixer (560 μm×590 μm)

V_g: gate bias voltage; IF: intermediate freqency; RF: radio frequency; LO: local oscillation

3 Mixer design and implementation

Fig. 3a shows the schematic diagram of the proposed SHPRM. A short stub acting as an inductor is placed at the input port of the balun to cancel the pad-to-ground parasitic capacitance. At the output ports of the balun, two NMOS transistors connected in parallel are gate-pumped by differential LO signals, which drive the alternatively working transistors. For signal mixing, two MOS drains are connected and exited by an RF signal through a compact directional coupler for input match. The IF signal is extracted from the drains via a low pass filter. The mixer is fabricated using the standard 1P6M 0.18-μm CMOS technology. The chip photograph is shown in Fig. 3b.

To characterize the mixer's main performance, the critical specification of the conversion gain (CG) is given as

$$\mathrm{CG}=R_{\mathrm{L}}R_{\mathrm{RF}}K^2\left[\frac{\alpha V_{\mathrm{LO}}^2}{8}\left(1-3\alpha\frac{V_{\mathrm{LO}}}{\pi}\right)-\frac{V_{\mathrm{LO}}}{3\pi}\right]^2, \quad (7)$$

where R_{L} is the load resistance at the IF port and R_{RF} is the input resistance at the RF port, V_{LO} is the voltage amplitude of the LO signal, and α and K are defined in the Appendix, which describes the derivation in detail.

From Eq. (7), it can be generalized that CG changes with respect to the variation of V_{LO}. An optimum value of CG will be obtained by the scan of V_{LO} which is related to the input LO power. As described in the Appendix, Eq. (7) is derived in the case of $V_{\mathrm{g}}=V_{\mathrm{T}}$, where V_{g} is the gate bias voltage and V_{T} is the threshold voltage. It means that a close relationship implicitly exists between CG and V_{g}. The simulated and measured results shown in Fig. 4 experimentally confirm the analysis and inference above. Significantly, the determined values of the optimum bias voltage and LO input power are 0.1 V and 8 dBm, respectively. Other performance specifications measured under these circumstances will be conducted in the following section.

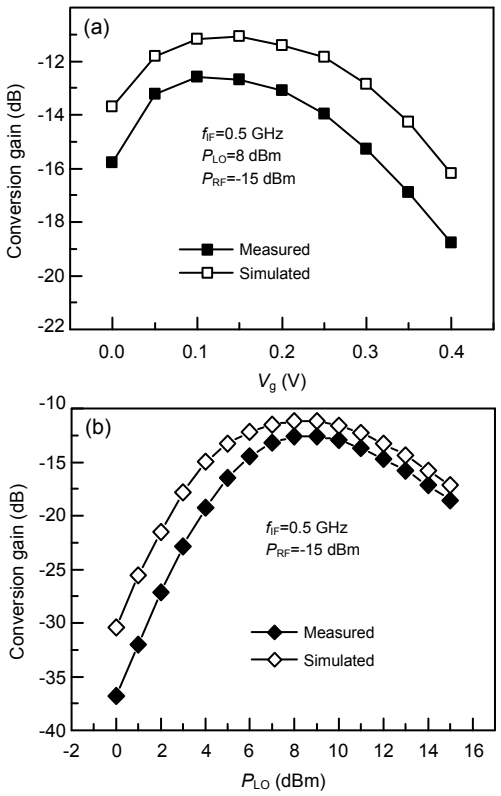


Fig. 4 Simulated and measured results of the conversion gain with respect to the gate bias voltage V_g (a) and the local oscillation power P_{LO} (b)

4 Experimental results and discussion

The input return losses of the LO and RF ports were measured using the Agilent E8363B vector network analyzer (VNA) and a cascade probe station with 40 GHz probes and coaxial cables. The probes and cables were calibrated using an open-through-short-load method. The IF port was terminated by a 50 Ω resistor during the measurement. The measured results are shown in Fig. 5.

One-tune measurements, including conversion gain and port-to-port isolations, were carried out using a spectrum analyzer. LO and RF signals were generated by two signal generators. The cable losses vs. frequencies were also measured and then taken from the final data sheets.

Fig. 6 shows the conversion gain measured at a fixed IF of 0.5 GHz under an LO power of 8 dBm and RF power of −15 dBm with the RF varying from 26.5 to 39.5 GHz. It fluctuates between −15.5–−12.5 dB when the RF range from 28 to 35 GHz. The maximum conversion gain of −12.5 dB can be observed at 31.5 GHz. The simulated curve is also incorporated for comparison and it corresponds well with the measured one.

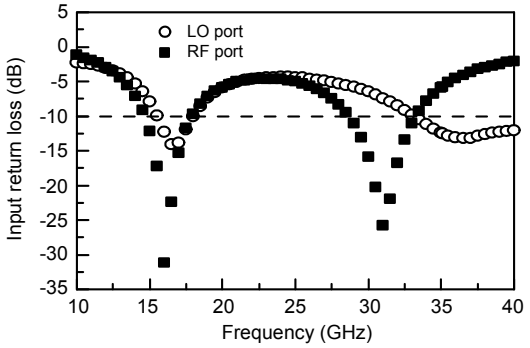


Fig. 5 Measured input return losses of the local oscillation (LO) and the radio frequency (RF) ports

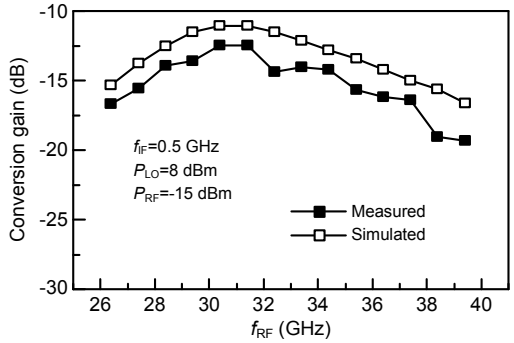


Fig. 6 Measured and simulated results of the conversion gain vs. radio frequency (f_{RF})

Fig. 7 shows the conversion gain measured under an 8 dBm LO power and −15 dBm RF power. The RF gradually increases from 31.1 to 32 GHz by a step size of 0.1 GHz while the LO frequency is fixed at 15.5 GHz. The obtained conversion gain is higher than −15 dB for IF spanning from 0.1 to 1.0 GHz.

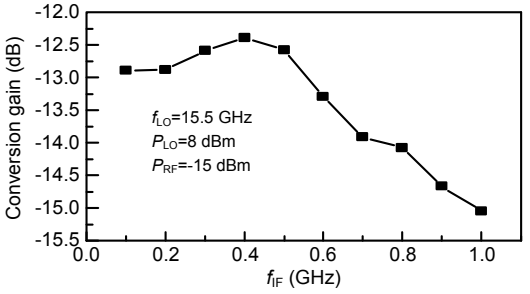


Fig. 7 Measured conversion gain vs. intermediate freqency (f_{IF})

The port-to-port isolations of LO-IF, LO-RF, RF-IF, 2LO-IF, and 2LO-RF are measured at a fixed IF of 0.5 GHz. The results in Fig. 8 indicate that the mixer performs good in-band port-to-port isolations.

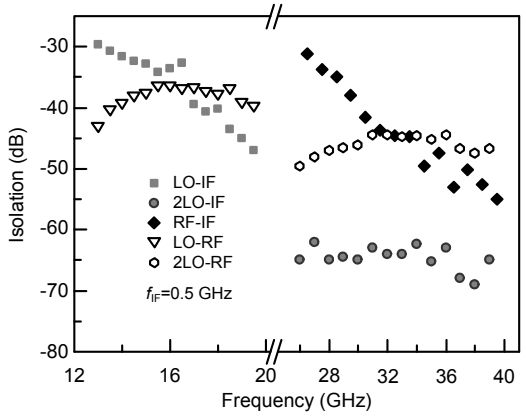


Fig. 8 Measured port-to-port isolations at a fixed f_{IF}=0.5 GHz

The 3rd-order inter-modulation intercept point (IIP3) performance is generally determined by two-tone measurements. Two tones separately generated by two signal sources with a frequency shift of 500 kHz were applied on the RF port through a signal synthesizer. The synthesized signals then mixed with the LO signal and a modulated spectrum extracted from the IF port would be displayed on the spectrum analyzer. The measured input referred P1dB and extrapolated IIP3 shown in Fig. 9 are 0.5 dBm and 10.5 dBm, respectively.

The performances of the proposed SHPRM and some other recently published papers are summarized in Table 1 for comparison. As far as CMOS process is concerned, it is noted that the circuit proposed by Bao *et al*. (2006) shows the widest bandwidth, but inferior performances in terms of isolation and IIP3. Moreover, it requires the largest LO power and occupies the largest chip area. Compared to this work, the mixers designed by Wei *et al*. (2008) and Chiou and Lin (2011) perform better conversion gains and IIP3s with relatively low LO power levels. This is attributed to the advanced 1P8M 0.13-μm CMOS technology they used. The thicker top metal provided by the 0.13-μm CMOS process results in the lower insertion loss of balun. Therefore, the potential LO power is saved. In addition, the advanced process provides transistors with shorter channel length L. According to Eq. (7), it is implicit that CG is inversely proportional to L^2 because $K=\mu_0 C_{ox} W/L$, which is given in the Appendix. Thus, CG would be theoretically at least 2.8 dB improved if our circuit was re-fabricated using the 1P8M 0.13-μm CMOS technology. In this case, CG is comparable to the proposed ones. The disadvantages of the mixers proposed by Wei *et al*. (2008) and Chiou and Lin (2011) are higher absolute gate bias voltage requirements and larger chip area occupation. Particularly, the demand for the negative voltage in Chiou and Lin (2011) reduces its flexibility in RF frond-end integration.

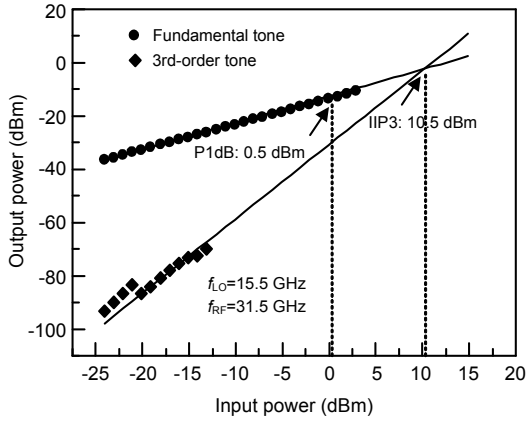


Fig. 9 Measured P1dB and IIP3 at a fixed f_{IF}=0.5 GHz

Table 1 Comparison of the performances for currently published SHPRMs

Reference	Process	RF (GHz)	Conv. gain (dB)	LO power (dBm)	Isolation (dB)			IIP3 (dBm)	Gate bias (V)	Chip area (mm^2)
					LO-RF	LO-IF	RF-IF			
Hwang *et al.* (2004)	0.15-μm pHEMT	85–92	−10–−4.7	10	15–25	20–30			−1	2
Bao *et al.* (2006)*	90-nm CMOS	9–31	−11–−8	9.7	17	22.5	37.7	3	0.12	1
Wei *et al.* (2008)	0.13-μm CMOS	18–26	−12–−11	4–8	30	33	30	14–20	0.3	0.41
Chiou and Lin (2011)	0.13-μm CMOS	28–50	−11–−9.6	7	37	31	36	16	±0.4	0.61
Sun *et al.* (2011)	0.15-μm pHEMT	27.5–28.5	−11	13	35	30	23			2
This work	0.18-μm CMOS	28–35	−15–−12.5	8	36.3–40	31–40	34–50	10.5	0.1	0.33

* 1/2-LO-source pumped SHPRM

5 Conclusions

This paper propose a sub-harmonically gate-pumped resistive mixer with a novel magnitude and phase imbalance compensated Marchand balun. From the measured results, the mixer features that the conversion gain is −15–−12.5 dB and that the isolations between ports are all better than 31 dB with an LO power level of 8 dBm for the RF ranging from 28 to 35 GHz. The measured input referred P1dB and IIP3 are 0.5 and 10.5 dBm, respectively. It is worth mentioning that the circuit is measured under a gate bias voltage as low as 0.1 V and it only occupies a chip area of 0.33 mm^2 including pads.

References

Bao, M., Jacobsson, H., Aspemyr, L., Carchon, G., Sun, X., 2006. A 9-31-GHz subharmonic passive mixer in 90-nm CMOS technology. *IEEE J. Sol.-State Circ.*, **41**(10): 2257-2264. [doi:10.1109/JSSC.2006.881551]

Barker, G.K., Badawi, M.H., Mun, J., 1984. 60GHz monolithic GaAs front-end circuit for reciver applications. *Electron. Lett.*, **20**(8):334-335. [doi:10.1049/el:19840226]

Chiang, P.Y., Su, C.W., Luo, S.Y., Hu, R., Jou, C.F., 2010. Wide-IF-band CMOS mixer design. *IEEE Trans. Microw. Theory Techn.*, **58**(4):831-840. [doi:10.1109/TMTT.2010.2041575]

Chiou, H.K., Lin, J.Y., 2011. Symmetric offset stack balun in standard 0.13-μm CMOS technology for three broadband and low-loss balanced passive mixer designs. *IEEE Trans. Microw. Theory Technol.*, **59**(6):1529-1538. [doi:10.1109/TMTT.2011.2140123]

Chiou, H.K., Yang, T.Y., Hsu, Y.C., Lin, S.G., Juang, Y.Z., 2007. 15–60 GHz asymmetric broadside coupled balun in 0.18 μm CMOS technology. *Electron. Lett.*, **43**(19): 1028-1030. [doi:10.1049/EL:20071200]

Hwang, Y.J., Wang, H., Chu, T.H., 2004. A W-band subharmonically pumped monolithic GaAs-based HEMT gate mixer. *IEEE Microw. Wirel. Comp. Lett.*, **14**(7):313-315. [doi:10.1109/LMWC.2004.829256]

Lin, C.H., Lai, Y.A., Chiu, J.C., Wang, Y.H., 2007. A 23–37 GHz miniature MMIC subharmonic mixer. *IEEE Microw. Wirel. Comp. Lett.*, **17**(9):679-681. [doi:10.1109/LMWC.2007.903460]

Lin, C.M., Lin, H.K., Lai, Y.A., Chang, C.P., Wang, Y.H., 2009. A 10–40 GHz broadband subharmonic monolithic mixer in 0.18-μm CMOS technology. *IEEE Microw. Wirel. Comp. Lett.*, **19**(2):95-97. [doi:10.1109/LMWC.2008.2011330]

Sun, M., Zhang, Y.P., Liu, D.X., Chua, K.M., Wai, L.L., 2011. A ball grid array package with a microstrip grid array antenna for a single-chip 60-GHz receiver. *IEEE Trans. Antennas Propag.*, **59**(6):2134-2140. [doi:10.1109/TAP.2011.2143669]

Wang, N.Y., Wu, H., Liu, J.Y.C., Chang, M.C.F., 2011. 65-nm CMOS receiver with 4.2 dB NF and 66 dB gain for 60 GHz applications. *Electron. Lett.*, **47**(1):15-17. [doi:10.1049/EL.2010.3049]

Wei, H.J., Meng, C., Wu, P.Y., Tsung, K.C., 2008. K-band CMOS sub-harmonic resistive mixer with a miniature Marchand balun on lossy silicon substrate. *IEEE Microw. Wirel. Comp. Lett.*, **18**(1):40-42. [doi:10.1109/LMWC.2007.911991]

Xu, L.J., Wang, Z.G., Li, Q., 2009. Design and analysis of millimeter-wave Marchand balun with interconnected transmission line. *J. Infr. Millim. Terahertz Waves*, **30**(7): 738-745. [doi:10.1007/S10762-009-9504-8]

Yeh, P.C., Liu, W.C., Chiou, H.K., 2005. Compact 28-GHz subharmonically pumped resistive mixer MMIC using a lumped-element highpass/band-pass balun. *IEEE Microw. Wirel. Comp. Lett.*, **15**(2):62-64. [doi:10.1109/LMWC.2004.842814]

Yu, H.Y., Choi, S.S., Kim, S.H., Kim, Y.H., 2007. K-band balun with slot pattern ground for wide operation using 0.18 μm CMOS technology. *Electron. Lett.*, **43**(5):293. [doi:10.1049/EL:20070092]

Appendix: Derivation of Eq. (7)

The conversion gain of a sub-harmonic resistive mixer is mathematically derived under the LO gate-pumped mode. To simplify the deriving process, the second-order effects are neglected and the parasitic effects are not taken into account. Thus, the final expression for the conversion gain is not accurate enough for calculation. However, it provides a rule of thumb to analyze what the key factors are to determine the conversion gain.

When the RF and LO signals are respectively applied to the drain and gate, the drain-source voltage and gate-source voltage can be expressed as

$$V_{\mathrm{DS}} = V_{\mathrm{RF}} \sin(\omega_{\mathrm{RF}} t), \tag{A1}$$

$$V_{\mathrm{GS}} = V_{\mathrm{g}} + f(\omega_{\mathrm{LO}} t), \tag{A2}$$

where $f(\omega_{\mathrm{LO}}t)$ denotes a Fourier series representing the LO voltage of a positive half-cycle period (Hwang *et al.*, 2004):

$$f(\omega_{\mathrm{LO}} t) = V_{\mathrm{LO}} \left[\frac{1}{\pi} + \frac{1}{2} \sin(\omega_{\mathrm{LO}} t) - \frac{2}{\pi} \left(\frac{\cos(2\omega_{\mathrm{LO}} t)}{1 \times 3} + \frac{\cos(4\omega_{\mathrm{LO}} t)}{3 \times 5} + \frac{\cos(6\omega_{\mathrm{LO}} t)}{5 \times 7} + \cdots \right) \right]. \tag{A3}$$

The applied RF signal at the drain is not large enough to drive the transistor into the saturation region. Simultaneously considering the mobility degradation and the triode operating region of the transistor, we obtain the drain current I_D which is expressed as

$$\begin{aligned} I_D &= K\frac{\left(V_{GS}-V_T-\frac{1}{2}V_{DS}\right)V_{DS}}{1+\alpha(V_{GS}-V_T)} \\ &\approx K\left((V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right) \\ &\quad\times\left(1-\alpha(V_{GS}-V_T)+\alpha^2(V_{GS}-V_T)^2-\cdots\right), \end{aligned} \tag{A4}$$

where $K=\mu_0 C_{ox}W/L$, α approximately models the mobility degradation, and $V_{GS}-V_T$ can be written as

$$V_{GS}-V_T=f(\omega_{LO}t)+V_g-V_T. \tag{A5}$$

It should be pointed out that Eq. (A3) is obtained under the condition of $V_g=V_T$. Therefore, Eq. (A5) is rewritten as

$$V_{GS}-V_T=f(\omega_{LO}t). \tag{A6}$$

From Eqs. (A3)–(A6), it can be found that $(V_{GS}-V_T)V_{DS}$, $-\alpha(V_{GS}-V_T)^2V_{DS}$, and $\alpha^2(V_{GS}-V_T)^3V_{DS}$ contain the IF angular frequency of $(\omega_{RF}-2\omega_{LO})$, which is extracted as

$$\begin{aligned} I_D(\omega_{IF}) &= I_D(\omega_{RF}-\omega_{LO}) \\ &= \frac{K\alpha V_{LO}^2 V_{RF}}{8}\left(1-3\alpha\frac{V_{LO}}{\pi}\right)-\frac{KV_{LO}}{3\pi}V_{RF}. \end{aligned} \tag{A7}$$

The corresponding IF, LO, and RF signal power levels are then given by

$$P_{IF}=\frac{1}{2}I_D^2(\omega_{IF})R_L, \tag{A8}$$

$$P_{LO}=\frac{1}{2}V_{LO}^2/R_{LO}, \tag{A9}$$

$$P_{RF}=\frac{1}{2}V_{RF}^2/R_{RF}. \tag{A10}$$

Finally, the conversion gain is derived from Eqs. (A7) to (A10):

$$\mathrm{CG}=R_L R_{RF}K^2\left[\frac{\alpha V_{LO}^2}{8}\left(1-3\alpha\frac{V_{LO}}{\pi}\right)-\frac{V_{LO}}{3\pi}\right]^2.$$