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Electrical characterization of integrated passive devices using thin film technology for 3D integration*

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Abstract: With the development of 3D integration technology, microsystems with vertical interconnects are attracting attention from researchers and industry applications. Basic elements of integrated passive devices (IPDs), including inductors, capacitors, and resistors, could dramatically save the footprint of the system, optimize the form factor, and improve the performance of radio frequency (RF) systems. In this paper, IPDs using thin film built-up technology are introduced, and the design and characterization of coplanar waveguides (CPWs), inductors, and capacitors are presented.

Key words: Integrated passive device (IPD), Benzocyclobutene (BCB), Thin flim, 3D Integration
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1 Introduction

Passive devices have been widely used in radio frequency (RF) systems for matching circuit networks, filtering, power delivery network (PDN) decoupling, and so on. As there are always trade-offs in discrete passive devices between high quality (*Q*) factor and the reduction of device footprint and cost, integrated passive devices (IPDs) have been massively studied to replace discrete passive devices to meet the ever increasing higher performance and lower form factor requirements of electronics systems, especially in handheld consuming devices. Mi *et al.* (2008) reported IPDs on a low temperature co-fired ceramic (LTCC) substrate for RF-module applications. Using developed multistage plating technology, aerial spiral inductors and capacitors are fabricated to increase the *Q* factor and reduce parasitic capacitance. However, the process tolerance and poor scaling ability of the LTCC technology limit its further integration. Siew *et al.* (2011) showed their silicon-based IPDs with multilayer thin film technology. Polyimide (PI) was used as the inter-metal dielectric material with a plated copper redistribution layer (RDL) as the conductive material. Inductors of 1–23 nH with self-resonant frequency of 1–6 GHz and *Q* factor of 10–45 were developed, as well as capacitors of 10 pF/mm^2. As copper can easily drift into PI, reliability is a major concern in this approach.

Through-silicon-via (TSV) based 3D integration technology has recently been attracting interest with short vertical interconnect, high density, and high performance (Beyne, 2008; Lu, 2009; Ramm *et al.*, 2010). Combining TSV and IPD in 3D integration will further extend and diversify the device/system functions (Zinck, 2010) (Fig. 1). Multilayer thin film technology is usually used to fabricate the RDL to

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reroute TSV signals. It is just compatible with IPD fabrication, so that RDLs and IPDs can be formed simultaneously on either the front or backside of the silicon wafer (Liu *et al.*, 2012; Yook *et al.*, 2012; Zhan *et al.*, 2012).

Many polymer materials, such as PI, SU8, parylene, benzocyclobutene (BCB), have recently been widely used as key elements in wafer-level packaging (WLP) and 3D integration (Töpper *et al.*, 2010; Baron *et al.*, 2012). These polymers can be used as adhesive tape, temporary bonding adhesive, molding compound, wafer level underfill, dielectric passivation resist, and so on, either to simplify the fabrication process and reduce cost, or to improve electrical or thermo-mechanical performance of the device or system.

Compared with the other abovementioned polymers, BCB has lower moisture absorption, lower shrinkage, lower deposition temperature, lower copper drift issue, and higher planarization level, as well as lower dielectric constant (ε_r=2.65), lower dielectric loss (loss tangent, $\tan\delta=8\times10^{-4}$), and greater thermal stability, which makes it a great candidate for WLP and 3D integration applications.

In this paper, we present the thin film process for IPD fabrication using photosensitive BCB as the inter-metal dielectric on the silicon substrate. Copper is electroplated on BCB to form the IPD structures. The process is developed to suit 3D integration using TSV and stacking. Characterization of passive structures including coplanar waveguides (CPWs), inductors, and capacitors will also be discussed.

2 Fabrication process

In our 3D integration scheme, the thin film process is implemented to form an RDL and IPDs after TSV fabrication. The main steps of the thin film process are shown in Fig. 2 (Cui *et al.*, 2011). To get a comprehensive understanding of the IPD fabrication in our 3D integration, TSV is also illustrated in the process.

The process starts with a 100-mm silicon wafer with a thickness of about 500 μm. TSVs are etched by deep reactive-ion etching (DRIE), isolated with SiO_2, filled with electroplated copper (Sun *et al.*, 2010), and grinded to remove residual metal patterns and TSV overburdens on the surface. An optional metal sputtering and patterning can be implemented to form the first RDL layer on SiO_2.

Then, there starts the thin film build-up process. First, an adhesion promoter AP3000 (Dow Chemical Co., USA) is deposited on the wafer surface to improve adhesion between the BCB layer and the substrate surface. Then, CYCLOTENE 4024-40 BCB is directly deposited on the silicon substrate by spin coating (Fig. 2a). The wafer is then pre-baked on a hot plate at 80 °C for 90 s, and exposed to deep ultraviolet (UV) light with exposure dose in the range of 180–230 mJ/cm^2. After UV exposure, the wafer is immersed in the DS3000 developer (Dow Chemical Co., USA) at 34 °C for 5 min, and hard cured at 210 °C in an annealing oven for 40 min with N_2 protection (Fig. 2b). In this cure condition, about 80% of the BCB is cured, which helps to improve adhesion

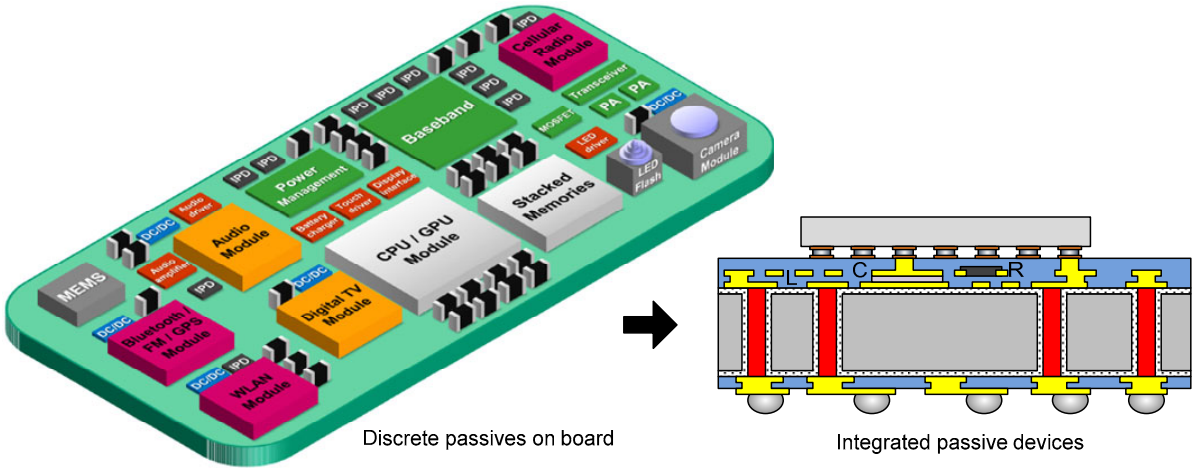

Fig. 1 From discrete passives on board to IPDs in 3D integration

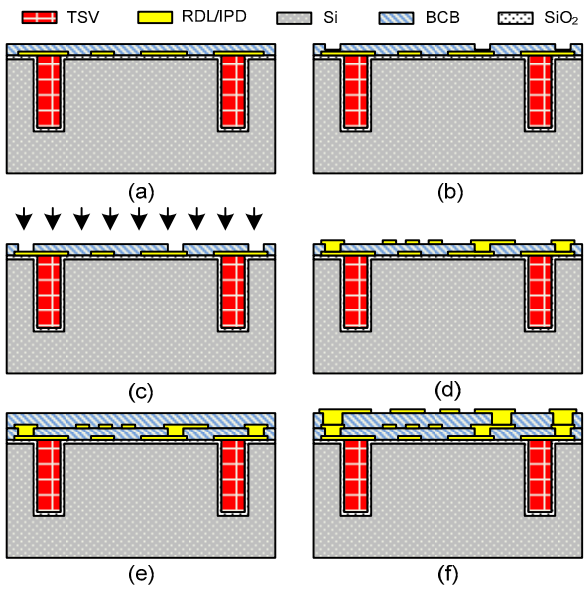

Fig. 2 Benzocyclobutene (BCB) thin film process
(a) 1st BCB spin-coating; (b) 1st BCB lithography; (c) Residual BCB removal; (d) 1st Cu electroplating; (e) 2nd BCB spin-coating; (f) 2nd Cu electroplating

strength between adjacent BCB layers. Successive multiple coating-curing approaches can be used to increase the BCB thickness to meet specific applications. A hard cure is always applied to the top BCB layer at 250 °C for 60 min to further strengthen its stability and reliability. A thin residual BCB layer of about 100 nm thickness may be left on the substrate after the lithography process, so oxygen plasma treatment is followed in Fig. 2c, with bias power of 130 W, chamber pressure of 2.0 Pa, O_2 flow of 80 standard-state cubic centimeters per minute (sccm), and CF_4 20 sccm for 50 s. SF_6 flow of 10 sccm is also necessary to remove the Si inside the polymer chains of BCB and avoid oxidation of the BCB surface. A thin Ti/Cu seed layer (20 nm/400 nm) is sputtered on the BCB. Then a photoresist mask for electroplating is patterned and Cu electroplating is carried out. After removing the residual Ti/Cu seed layer on the wafer surface, the first metal layer is fabricated (Fig. 2d). By adjusting the current density and electroplating time, a Cu layer of different thicknesses, 1–5 μm for instance, can be obtained.

Repeating the BCB coating (Fig. 2e) and Cu electroplating steps (Fig. 2f), multi-layered metal structures can be fabricated. All the steps are carried out below 250 °C, which suits the 3D integration process.

Fig. 3 shows some test structures of the BCB-based thin film process, including a Cu line (Fig. 3a), comb structure (Fig. 3b), and daisy chain (Fig. 3c) to verify and characterize the basic electrical properties of this thin film process. TSV-RDL is also illustrated (Fig. 3d) to show the process compatibility of TSV and thin film IPDs. Fig. 3e is the cross section of a two-layered metal structure. The first and second BCB layers in the fabrication sequence are noted as BCB-1 and BCB-2 with thicknesses of 4.8 and 5.9 μm, respectively. The first and second Cu lines noted as Cu-1 and Cu-2 are 3.0 and 3.5 μm thick, respectively. Measured DC resistance of the Cu interconnect with line thickness/width of 2.5 μm/20 μm is 6.5 to 7.4 Ω/cm, that is, a sheet resistance of 13 to 14.8 mΩ/sq. For the Cu line of 3 μm thickness and 30 μm width, DC resistance is 2.9–3.7 Ω/cm, which equals a sheet resistance of 8.7–11.1 mΩ/sq. All the factors including lithography resolution, BCB shrinkage in the curing step, and surface roughness of the electroplated Cu lines may contribute to fluctuations of metal line resistance and its deviation from ideal copper conductivity.

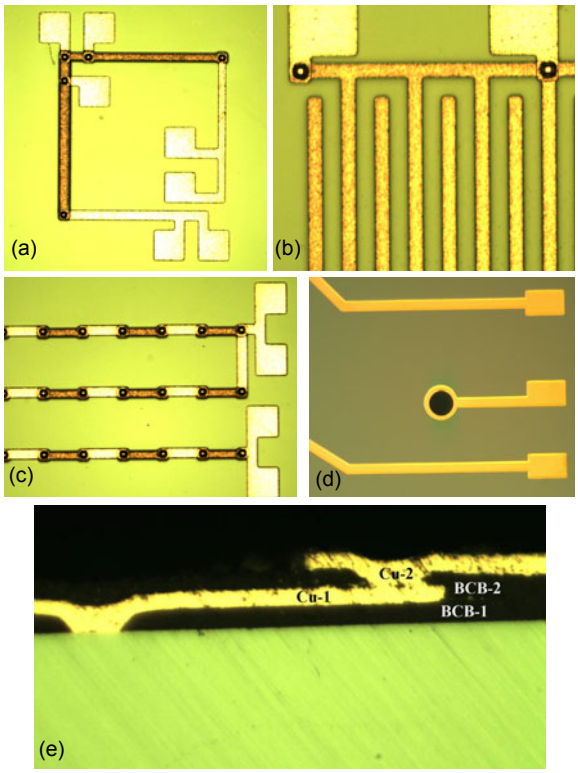

Fig. 3 Benzocyclobutene (BCB) thin film structures
(a) Cu line; (b) Comb structure; (c) Daisy chain; (d) TSV-RDL; (e) Two-layered metal line cross section

Successive steps include chemical mechanical planarization (CMP) of the wafer surface, micro-bumps forming, wafer backside thinning, and so on. BCB ensures a fine planarization of wafer surface after the thin film process, which helps to improve both performance and reliability of devices.

3 Integrated passive device (IPD) design and characterization

The designed and fabricated passive devices by the former described thin film built-up process include a one/two-layered CPW, a planar rectangle spiral inductor, and a parallel-plate capacitor. The dimension schematic of the thin film devices is illustrated in Fig. 4. The thicknesses of the bottom and top Cu lines are noted t_1/t_2, and h_1/h_2 for thicknesses of the bottom and top BCB layers. The silicon substrate is about 500 μm thick, with a quite low resistivity of 2–4 Ω·cm.

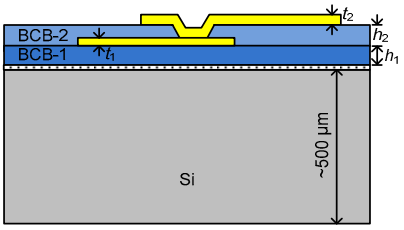

Fig. 4 Two-layered thin film structure schematic

On-wafer *S*-parameter measurements were carried out using the Agilent vector network analyzer (VNA) and microwave probe station from 0.01–20 GHz at room temperature.

3.1 Coplanar waveguide (CPW)

CPWs of one/two-layered metal with different line widths and spaces have been fabricated (Fig. 5) to characterize the high frequency signal loss through Cu RDLs. Table 1 lists the dimensions of the fabricated CPWs, where W_1/W_2 stands for signal line widths of the bottom and top Cu lines, and S_1/S_2 are the gap widths between the signal line and ground.

Fig. 6a compares the insertion loss of a single-layered CPW with different BCB thicknesses between the silicon substrate and CPWs (4.8-μm thick BCB for CPW1 and CPW2, and 10.7-μm thick BCB for CPW3 and CPW4). Attenuation of 0.8 dB/mm at 20 GHz can be achieved for a single-layered CPW. It is clear that the insertion loss of CPW lines decreases with increase of the signal line width from the comparisons of insertion loss of CPW1 and CPW2, and CPW3 and CPW4. On the other hand, it increases as the BCB layer becomes thicker.

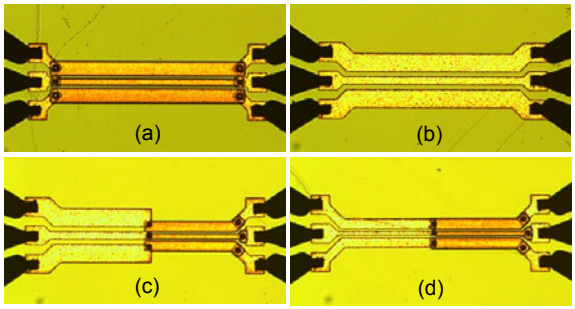

Fig. 5 Fabricated coplanar waveguides (CPWs)
(a) CPW with bottom metal layer; (b) CPW with top metal layer; (c) CPW with two metal layers and different line widths; (d) CPW with two metal layers and the same line width

Table 1 Dimensions of coplanar waveguides (CPWs)

CPW	W_1/W_2	S_1/S_2	t_1/t_2	h_1/h_2
CPW1	15/–	12.5/–	2.5/–	4.8/5.9
CPW2	30/–	21/–	2.5/–	4.8/5.9
CPW3	–/15	–/11.5	–/3	4.8/5.9
CPW4	–/30	–/21	–/3	4.8/5.9
CPW5	20/20	15/15	2.5/3	4.8/5.9
CPW6	20/40	15/27	2.5/3	4.8/5.9
CPW7	30/30	21/21	2.5/3	4.8/5.9
CPW8	30/60	21/39	2.5/3	4.8/5.9

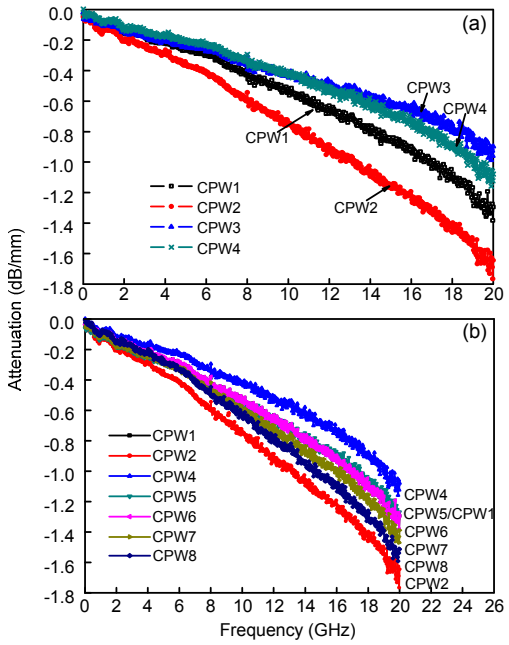

Fig. 6 Attenuation of single-layered CPW (a) and two-layered CPW (b)

Fig. 6b shows the insertion loss of two-layered CPWs compared with single-layered CPWs, noted as CPW5 to CPW8 in Table 1. The best result we obtain is 1.2 dB/mm at 20 GHz of CPW5. It can also be seen that insertion loss decreases with signal line width and increases with BCB thickness. Single-layered CPW with thicker BCB dielectric and narrower signal line width shows the best transmission performance among all the CPW patterns. A conclusion can be drawn that substrate coupling dominates the signal transmission performance (Leung *et al.*, 2004). Thicker BCB and narrower signal line help to decrease the electric field penetration into the substrate, and alleviate the coupling between the interconnect and the silicon substrate. Using high resistivity silicon and properly increasing BCB thickness are two direct ways to optimize the transmission performance of CPWs.

3D full wave simulations of single-layered CPWs have been carried out and the electric field distributions are captured to verify the impact of line width and BCB thickness on CPW transmission performance (Figs. 7 and 8).

As shown in Fig. 9, a distributed resistance, inductance, capacitance, and conductance (RLCG) parameter model for transmission line is applied to deliver a simple electrical circuit model of the fabricated single-layered CPW. RLCG parameters are derived from the measured *S*-parameters of the CPW structures (Eisenstadt and Eo, 1992; Frickey, 1994; Kim and Eo, 2008).

Fig. 10 shows the extracted RLCG parameters varying with frequency. Distributed resistance *R* in Fig. 10a is a few ohms per millimeter length, and increases as frequency goes up, which is mainly caused by skin effect. Distributed inductance *L* tends to be smoother, 2.5 to 3.0 nH/mm for the fabricated CPWs (Fig. 10b). Distributed capacitance *C* (Fig. 10c) and conductance *G* (Fig. 10d) represent the substrate loss of CPWs. A thinner BCB layer between silicon substrate and Cu interconnect lines results in greater CG parasitics.

3.2 Inductor

The planar spiral inductor also suits this thin film built-up process and can be easily integrated (Fig. 11). Two spiral inductors with different line widths and minimum inner radius are designed and fabricated in this paper to briefly show the process compatibility. Dimensions of the designed inductor are listed in Table 2 with two kinds of inductors noted as L1 and L2. Both inductors have 6.5 turns. Simulated

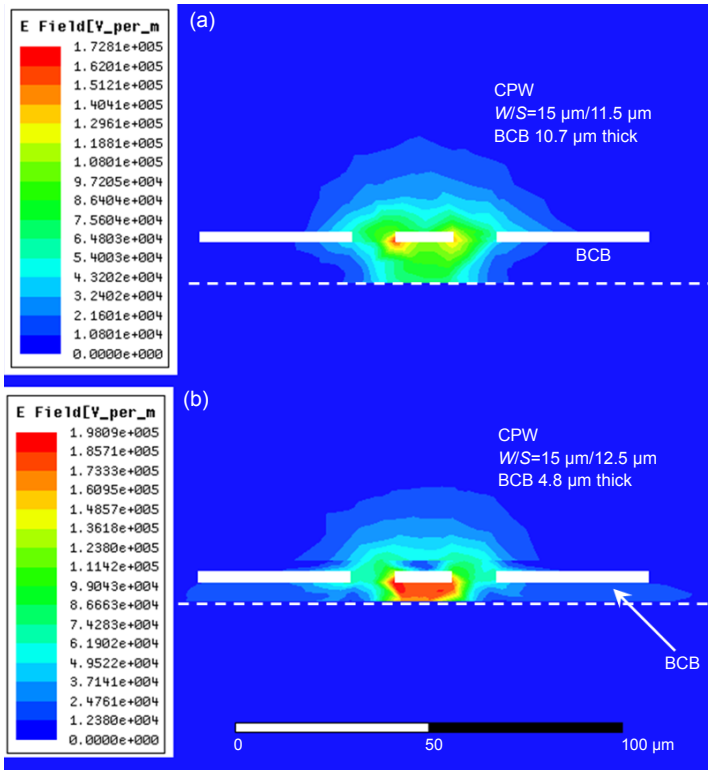

Fig. 7 Electric field distributions of single layer CPWs with different BCB thicknesses
(a) CPW3, BCB 10.7 μm thick;
(b) CPW1, BCB 4.8 μm thick

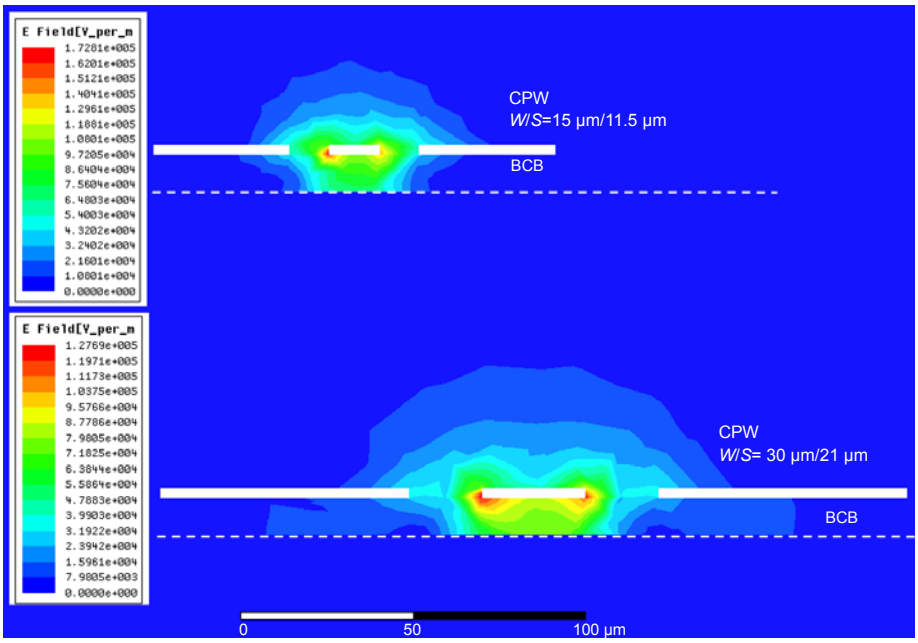

Fig. 8 Electric field distributions of single-layered CPWs with different signal line widths and spaces
(a) CPW3, line width/space=15 μm/11.5 μm; (b) CPW4, line width/space=30 μm/21 μm

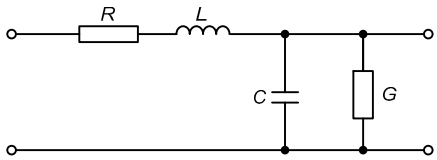

Fig. 9 Distributed resistance, inductance, capacitance, and conductance (RLCG) model of transmission line

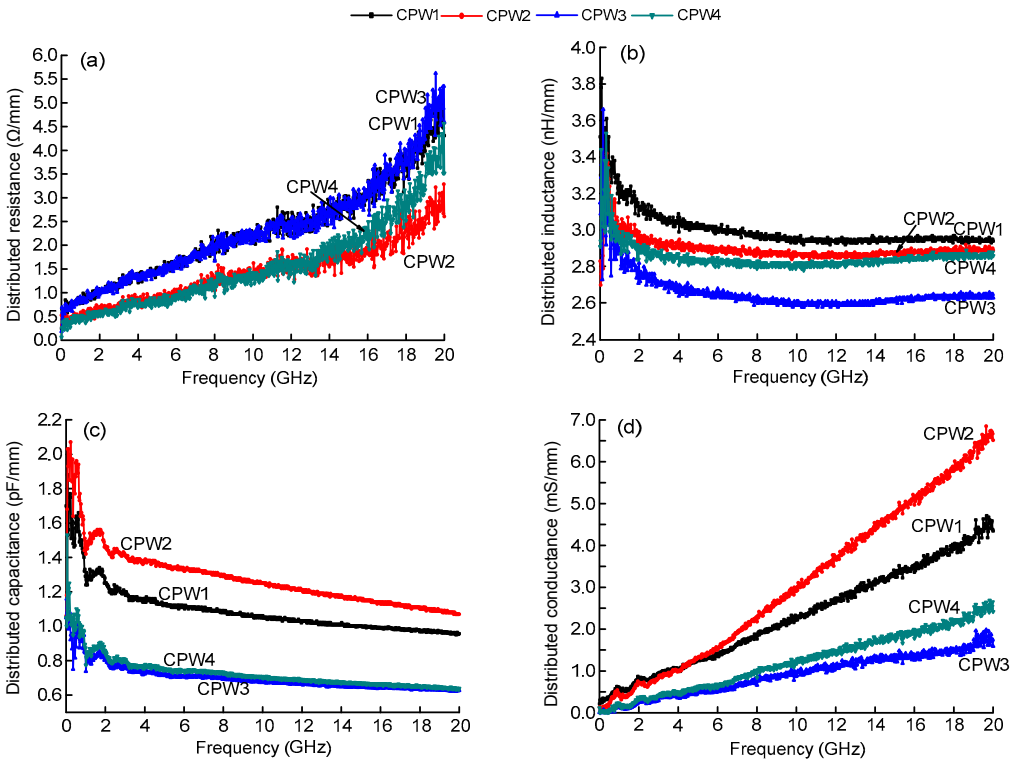

Fig. 10 Distributed RLCG parameters of single-layered CPW
(a) Resistance R; (b) Inductance L; (c) Capacitance C; (d) Conductance G

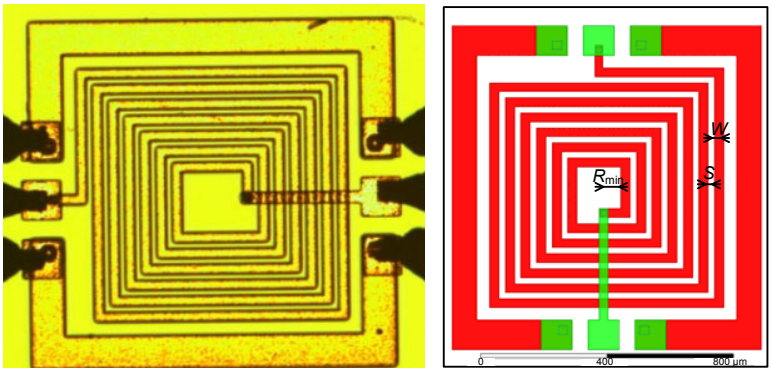

Fig. 11 Fabricated spiral inductor and inductor pattern
R_{min}: minimum metal radius;
S: metal line space;
W: metal line width

Table 2 Dimensions and measured results of inductors

Inductor	Line width (μm)	Line space (μm)	Minimum radius (μm)	Simulated L (nH)	Measured L (nH)	SRF (GHz)
L1	30	20	70	20.65	20.3	3.46
L2	20	20	80	19.97	19.5	3.80

SRF: self-resonant frequency

inductances by ANSYS Q3D are also illustrated in Table 2, with a magnitude of about 20 nH. The inductors are also measured by a vector network analyzer, and the inductance values are derived from scattering parameters and transformed Y parameters (Eisenstadt and Eo, 1992). The measured S_{21} parameter, Q factor, and inductance calculated from S parameters are illustrated in Fig. 12. The maximum Q factor is about 7 for both inductors. Calculated inductances of both are also shown in Fig. 12 and listed in Table 2, with less than 2.5% deviation from simulated results. Self resonant frequency (SRF) is defined when S_{21} obtains its minimum magnitude (Ashby *et al.*, 1996; Arcioni *et al.*, 1998), and is 3.46 and 3.8 GHz for the two inductors, L1 and L2, respectively. These inductors can be used in 2.4 GHz RF applications, and more design effort is needed to optimize the Q factor of inductors and think about higher frequency applications.

3.3 Capacitor

A metal-insulator-metal (MIM) capacitor is fabricated using BCB as the inter-metal dielectric and electroplated copper as the parallel plate (Fig. 13). Table 3 lists the dimensions of the fabricated capacitors noted as C1 and C2. In this paper, different sizes of capacitors are designed, and their capacitances are also calculated from measured S parameters, with a capacitance density of about 6 pF/mm^2 (Table 3; Fig. 14). 3D electromagnetic modeling is

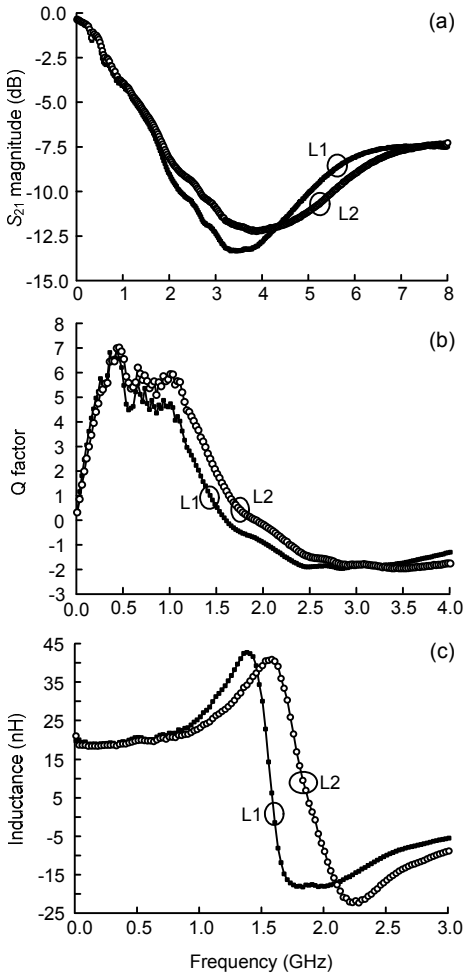

Fig. 12 Measured S_{21} parameter of inductors (a), derived Q factor (b), and inductance (c)

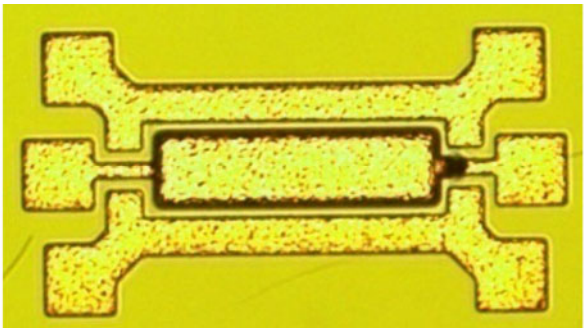

Fig. 13 Fabricated metal-insulator-metal (MIM) capacitor

Table 3 Dimensions and measured results of capacitors

Capacitor	Area (μm×μm)	BCB thickness (μm)	Simulated *C* (fF)	Measured *C* (fF)
C1	80×700	3.4	412.7	328.7
C2	80×300	3.4	175.7	158.3

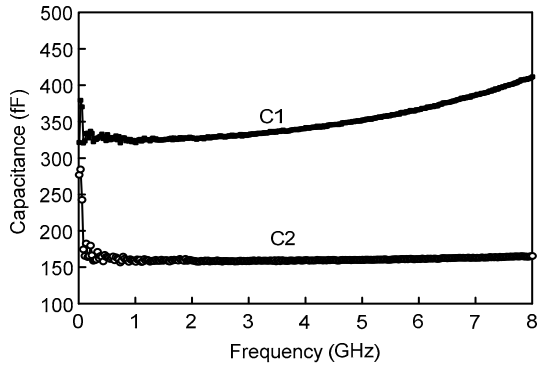

Fig. 14 Derived capacitance of the fabricated capacitor

carried out to evaluate the designed capacitor. There is a greater deviation from design models compared with inductors, up to 20%. As the MIM capacitor is very sensitive to the thickness of inter-metal dielectric, process variation control is essential, and an appropriate high-κ dielectric is also necessary.

4 Conclusions

In this paper, a BCB-based thin film process developed for IPDs fabrication is presented. The entire process can be carried out below 250 °C, which makes it flexible in 3D integration and WLP applications. Two-layered passive devices, including CPW, inductor, and capacitor are designed, fabricated, and measured. CPW obtains a minimum attenuation of 0.8 dB/mm at 20 GHz. The measured parameters of the inductors are an inductance of 20 nH, *Q* factor of 7, and self-resonant frequency of approximately 3.5 GHz. Capacitors of several hundred femto Faradays (fF) are also achieved in this research. The process for combining IPDs with TSV is undergoing and characterization of TSV-IPD structures will be done in the future.

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