Journal of Zhejiang University-SCIENCE C (Computers & Electronics)
ISSN 1869-1951 (Print); ISSN 1869-196X (Online)
www.zju.edu.cn/jzus; www.springerlink.com
E-mail: jzus@zju.edu.cn

Folded down-conversion mixer for a 60 GHz receiver architecture in 65-nm CMOS technology*

Najam Muhammad AMIN†, Zhi-gong WANG†‡, Zhi-qun LI

(*Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China*)

†E-mail: najam.m.amin@seu.edu.cn; zgwang@seu.edu.cn

Received Mar. 13, 2014; Revision accepted June 24, 2014; Crosschecked Nov. 9, 2014

Abstract: We present the design of a folded down-conversion mixer which is incorporated at the final down-conversion stage of a 60 GHz receiver. The mixer employs an ac-coupled current reuse transconductance stage. It performs well under low supply voltages, and is less sensitive to temperature variations and process spread. The mixer operates at an input radio frequency (RF) band ranging from 10.25 to 13.75 GHz, with a fixed local oscillator (LO) frequency of 12 GHz, which down-converts the RF band to an intermediate frequency (IF) band ranging from dc to 1.75 GHz. The mixer is designed in a 65 nm low power (LP) CMOS process with an active chip area of only 0.0179 mm^2. At a nominal supply voltage of 1.2 V and an IF of 10 MHz, a maximum voltage conversion gain (VCG) of 9.8 dB, a double sideband noise figure (DSB-NF) of 11.6 dB, and a linearity in terms of input 1 dB compression point ($P_{\text{in,1dB}}$) of −13 dBm are measured. The mixer draws a current of 5 mA from a 1.2 V supply dissipating a power of only 6 mW.

Key words: Folded mixer, Current reuse, Low power, Inductorless design, Direct conversion
doi:10.1631/jzus.C1400087 **Document code:** A **CLC number:** TN4

1 Introduction

The 7 GHz unlicensed band at 60 GHz has resulted in active research in CMOS integrated circuits (ICs) for high data-rate wireless communication systems. In 60 GHz transceiver designs, the receiver front-end is a critical block that amplifies a small RF signal from the antenna and converts it down to baseband under a specified signal-to-noise ratio (Cai *et al.*, 2013). The simplest realization of a 60 GHz receiver is by employing a direct conversion architecture (Afshar *et al.*, 2008; Marcu *et al.*, 2009; Tomkins *et al.*, 2009; Vecchi *et al.*, 2011), which has the advantage of low power consumption (compared to its heterodyne counterpart) due to fewer building blocks. Nevertheless, this simple architecture faces many challenges in terms of local oscillator (LO) I/Q generation, LO frequency division, and LO distribution, as has been discussed by Razavi (2009). Moreover, quadrature phase generation at 60 GHz has an effect of considerable degradation in phase noise according to Razavi (2009). The phase noise generated by a low frequency voltage-controlled oscillator (VCO) is magnified due to frequency multiplication in order to achieve a reference frequency close to the desired carrier frequency, which for the case of multicarrier transmission scheme such as orthogonal frequency division multiplexing (OFDM) is quite critical due to spectrum broadening.

The aforementioned LO related problems can be greatly simplified by employing dual-conversion or heterodyne receiver architecture (Fig. 1). After the weak input signal reception by the receive antenna and subsequent amplification along with noise

‡ Corresponding author

* Project supported by the National High-Tech R&D Program (863) of China (No. 2011AA010200)

ORCID: Najam Muhammad AMIN, http://orcid.org/0000-0002-9419-0380; Zhi-gong WANG, http://orcid.org/0000-0002-9203-4683

injection by the low noise amplifier (LNA), the input RF band ranging from 58.25 to 61.75 GHz is initially down-converted by mixer 1 in the receiver chain to an intermediate frequency (IF) band ranging from 10.25 to 13.75 GHz. A bandwidth of only 3.5 GHz out of the available 7 GHz has been considered, as the design of a 60 GHz wireless communication system covering the entire allocated bandwidth requires much higher power consumption compared to a wireless system which uses only a fraction of this allocated bandwidth. An example of portable devices with battery power limitation is worth mentioning, where the major concern is energy efficiency rather than higher bandwidth.

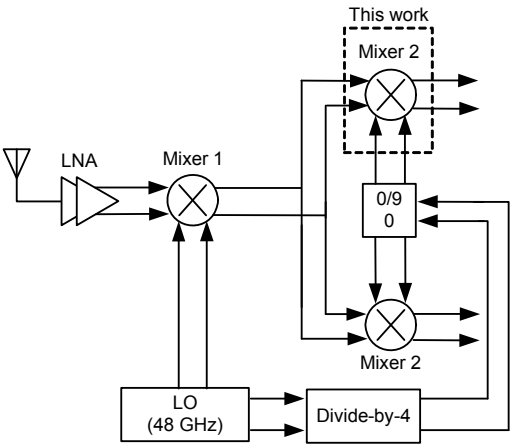

Fig. 1 The 60 GHz receiver architecture with emphasis on this work

The LO signal generation occurs at 48 GHz, without requiring quadrature phases along with subsequent division at the same frequency (to achieve the LO frequency for the final mixer, i.e., mixer 2, in the receiver chain), permitting a broadband design. Moreover, the distribution of differential LO signals at 48 GHz is much simpler than that of quadrature 60 GHz components. The down-converted IF band from mixer 1 (10.25–13.75 GHz) is finally down-converted directly to baseband ranging from dc to 1.75 GHz by an LO frequency of 48/4=12 GHz. The focus of this work is the design of the final down-conversion mixer (mixer 2) and it is the first design in a series of other design blocks for the 60 GHz receiver to follow (Fig. 1).

2 Mixer design and implementation

2.1 Folded mixer design

The design of the proposed folded mixer along with component values and transistor dimensions can be seen from Fig. 2. The output small-signal current of the transconductance stage (M1−M4) contains low frequency second-order intermodulation products in its spectrum, which can leak to the output IF stage (R_L) without being up-converted due to mismatches in switch transistors (M5−M8). To prevent this leakage, capacitive coupling is employed.

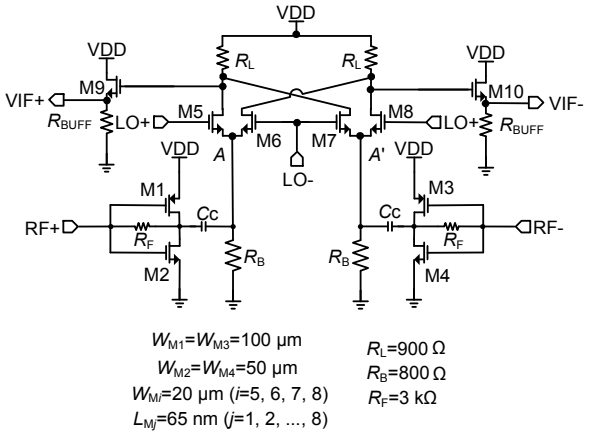

Fig. 2 Schematic of the proposed folded mixer design along with component values

The transconductance stage comprises a self-bias current reuse topology which is less sensitive to supply voltage, temperature, and process variations. By employing a feedback resistor to an inverter, bandwidth extension can be achieved along with self-biasing. The voltage gain (Wang and Wan, 2011) and noise factor (Hampel *et al.*, 2010) of the transconductance stage can be given as

$$A_V = (g_{m,NMOS} + g_{m,PMOS})(R_F // r_{ds,NMOS} // r_{ds,PMOS} // Z_L), \quad (1)$$

$$F = 1 + \frac{1}{R_s R_F}\left(\frac{1}{g_m} + R_s\right)^2 + \ldots + \frac{1}{R_s}\left(1 + \frac{R_s}{R_F}\right)^2\left(\frac{\gamma}{\alpha g_m} + \frac{\delta\alpha}{5g_m}\right), \quad (2)$$

where $g_{m,NMOS}$, $g_{m,PMOS}$ are the transconductances and $r_{ds,NMOS}$, $r_{ds,PMOS}$ are the output channel resistances of NMOS and PMOS transistors, respectively, whereas

Z_L denotes the transconductor's output load impedance in Eq. (1). In Eq. (2), R_s denotes the source resistance, γ, δ, and α represent the bias-dependent technology parameters, where $\alpha=g_m/g_{ds0}$ with $g_{dso}=g_{ds}$ for $V_{ds}=0$ (Hampel *et al.*, 2010). A high voltage gain can be achieved due to the improved transconductance of the stacked NMOS-PMOS transistor pair as is evident from Eq. (1). This voltage gain can further be increased by employing a high value of feedback resistance R_F. The high feedback resistance not only improves the voltage gain but also has an effect of noise figure reduction according to Eq. (2). This noise figure reduction, however, comes at the expense of deterioration in input matching.

To have an input match with a source resistance of 50 Ω, the value of R_F does not need to be high enough. The input impedance of an unloaded self-bias current reuse transconductance stage can easily be derived as (derivation can be seen in Appendix A)

$$Z_{IN}=\frac{R_F+R_{OUT}}{1+g_m R_{OUT}}, \tag{3}$$

where R_{OUT} is a parallel combination of $r_{ds,NMOS}$ and $r_{ds,PMOS}$, respectively. Eq. (3) can be rearranged for R_F, which leads to the following expression:

$$R_F=Z_{IN}(1+g_m R_{OUT})-R_{OUT}. \tag{4}$$

Assuming that a match of better than $S_{11}=-10$ dB is a feasible design criterion and solving the well-known equation of the input reflection coefficient given by

$$\Gamma=\frac{Z_{IN}-Z_o}{Z_{IN}+Z_o}, \tag{5}$$

in consideration of a 50 Ω reference impedance Z_0, the minimum and maximum values of Z_{IN} are approximately 25 and 100 Ω, respectively (Hampel *et al.*, 2010). Substituting the values of $g_m=g_{m,NMOS}+g_{m,PMOS}=48.31$ mS, $R_L=105.4$ Ω (obtained from the aspect ratios of inverter transistors) and the minimum and maximum values of Z_{IN} in Eq. (4), results in a corresponding range of R_F such that 46.89 Ω≤R_F≤503.78 Ω.

For the case of a folded mixer, if the value of R_F is chosen within the aforementioned range (when input matching is considered), a considerable leakage of LO to the RF port can severely deteriorate the overall performance of the mixer, also giving rise to DC offset which is highly undesirable for the design of a direct conversion mixer. Fig. 3 gives an illustration of the simulated noise figure and isolation characteristics of the self-bias current reuse topology, when employed to a folded mixer, with respect to variation in R_F.

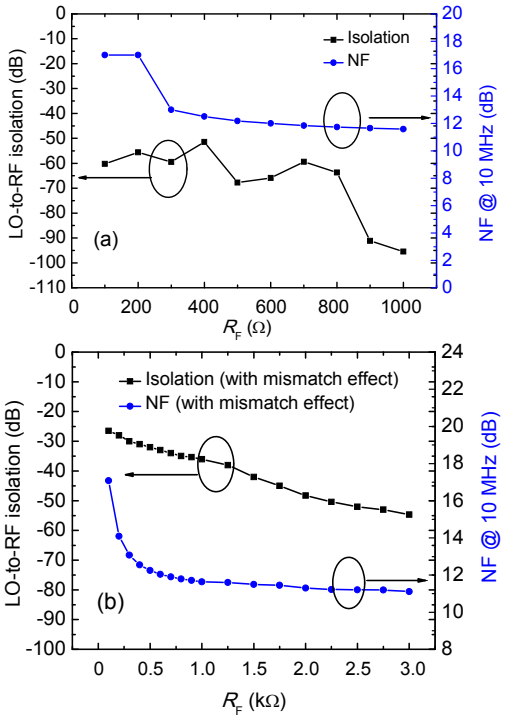

Fig. 3 Isolation and NF (at IF=10 MHz) variation with respect to R_F (a) and effect of mismatches on isolation and NF (b)

For a folded mixer operating under ideal conditions (no mismatches), a good LO to RF isolation can be seen from Fig. 3a even at R_F values as low as 100 Ω. The noise figure is approximately 18 dB for such a small value of R_F but settles down to an approximate value of 12 dB above 400 Ω without any further improvement by an increase in R_F. However, when the mismatch effects are considered (Fig. 3b), isolation between LO and RF ports worsens, and an improvement can be seen only for an increase in the value of R_F unlike the case for noise figure, which does not vary much above 500 Ω. The proposed mixer is designed so that it can be later integrated into a 60 GHz receiver architecture (Fig. 1), where input

matching is not a main concern. Instead, voltage conversion gain is preferred over power gain. Therefore, in this work input matching has been compromised for better isolation, low noise figure, and high voltage gain characteristics; hence, R_F is chosen to be high enough (R_F=3 kΩ). As can be seen from Fig. 3b, for LO-to-RF isolation ≥40 dB along with an NF of 11 dB, values of 1.5 kΩ≤R_F≤3 kΩ can qualify for a good transcondutance design.

The switch core of the mixer can be implemented by employing either PMOS or NMOS transistors. For a capacitively coupled transconductance stage and an implementation of switching stage using PMOS transistors, inductors need to be inserted between supply rails and switch transistors source terminals. These inductors not only relax the voltage headroom problem, not consuming any of the voltage themselves, but also resonate out the parasitic capacitance present at the source terminals.

For narrowband applications, these inductors can also be replaced by LC-tank circuits, as is the case in Chiou *et al.* (2012), where the resonant frequency of the tank circuit is close to LO and RF frequencies. Unfortunately, for a double-balanced mixer two such inductors or LC-tank circuits not only consume a lot of die area, thereby increasing the cost of fabrication, but also make the layout design problematic, due to long interconnecting lines giving rise to losses, thereby necessitating full-wave electromagnetic (EM) simulations. Although the PMOS switch core has the advantages of lower flicker noise and higher linearity under low LO power, at low bias current over its NMOS counterpart, it has lower conversion gain compared to the NMOS switch core. Moreover, the transition frequency f_T of PMOS transistors is much lower than that of NMOS transistors ($f_{T,NMOS}$= 150 GHz>$f_{T,PMOS}$=90 GHz in a TSMC 65 nm CMOS technology). Effort has been made in this work to realize an inductorless folded mixer. Therefore, NMOS transistors were the preferred choice for the switch core.

2.2 Conversion gain and linearity

The voltage conversion gain of the mixer, assuming a square wave LO signal and a high value of feedback resistance, can be given as (Vidojkovic *et al.*, 2005)

$$\mathrm{CG}=20\log\left(\frac{2}{\pi}(g_{\mathrm{m,\,NMOS}}+g_{\mathrm{m,\,PMOS}})R_{\mathrm{L}}\right), \tag{6}$$

where R_L is the load resistance. By decoupling the dc paths in a folded mixer (Fig. 2), the transconductance stage can be biased with a high dc current, which has the advantage of an increase in conversion gain. The feedback resistor R_F assures that both inverter transistors are in saturation by connecting their respective drain and gate terminals together. Not only is an increase in conversion gain possible by employing a folded type topology, but an increase in linearity is possible. The linearity in terms of the third-order input intercept point (IIP3) can be given as (Hampel *et al.*, 2010)

$$\mathrm{IIP3}=4\sqrt{\frac{2}{3}\frac{I_{\mathrm{ds},R_F}}{K_{R_F}}}, \tag{7}$$

where $K_{R_F}=2\mu C_{OX}W/L$ is the process parameter with electron or hole mobility μ, the gate oxide capacitance C_{OX}, and W and L are the width and length of the transistors respectively along with I_{ds,R_F} representing the bias current for the input transconductance stage. Clearly, from Eq. (7) an increase in bias current effectively increases the linearity of the mixer. Nonlinearity in the mixer is caused due to the switch transistors operating in the linear region. Therefore, the switch transistors should be biased in deep saturation such that $V_{ds}>>V_{ds,sat}$ and V_{gs} should be chosen slightly higher than V_{th} (for abrupt switching between saturation and cut-off regions) along with low voltage level and voltage swing at the source terminals of switch transistors.

2.3 Noise figure

The direct and indirect flicker noise contributions of switch transistors can be given as (Darabi and Abidi, 2000)

$$i_{\mathrm{n,dir}}=4I_{\mathrm{ds},\,R_F}V_{\mathrm{n}}/(ST), \tag{8}$$

where T is the LO period, S is the slope of the LO voltage at the switching time, and V_n is the slowly varying low frequency noise present at the gates of the switching pair, which modulates the time at which the switching pair starts to perform switching. It is expressed as

$$V_{\mathrm{n}}=\sqrt{2K_f/(WLC_{\mathrm{OX}}f)}\,, \tag{9}$$

where K_f is a process parameter and f is the frequency.

$$i_{\mathrm{n,indir}}=\frac{2C_{\mathrm{p}}}{T}V_{\mathrm{n}}\frac{(C_{\mathrm{p}}\omega_{\mathrm{LO}})^2}{(g_{\mathrm{m,SWITCH}})^2+(C_{\mathrm{p}}\omega_{\mathrm{LO}})^2}, \tag{10}$$

where C_{p} is the parasitic capacitance at the source terminal of the switch transistors and $g_{\mathrm{m,SWITCH}}$ is the switch transconductance (Amin *et al.*, 2012). To lower the direct flicker noise contribution, low bias current should flow through the switch transistors (M5–M8), as is evident from Eq. (8). This can be achieved with the help of a folded mixer topology along with high values of load (R_{L}) and source terminal (R_{B}) resistances. Having a high value load resistance not only limits the current through switch transistors, but also helps boost the conversion gain.

The direct flicker noise can also be lowered by employing wide switch transistors, as is evident from Eq. (9). However, by increasing the width of switch transistors to a large extent, C_{p} increases as well, which causes an increase in the indirect flicker noise, as can be seen from Eq. (10). Not only does the indirect flicker noise start increasing after reaching a maximum value of switch width, but the conversion gain starts to drop due to the small-signal RF current being shunted to ground by C_{p}. Therefore, to avoid the use of large area occupying inductors, a compromise has to be made between the direct, indirect flicker noise contributions and conversion gain. Finally, polysilicon resistors have been used to implement the load stage along with an output buffer matched to 50 Ω.

2.3 DC offset

Static dc offset caused by device mismatches, LO-to-RF leakage, and second-order intermodulation products is one of the major concerns when designing a direct-conversion mixer. When realizing a balanced mixer, mismatches in switch transistors and load resistances play a vital role in causing dc offset. This dc offset is further dependent on the amount of bias current flowing through the switching and load stages. From Fig. 4, dc offset voltage with respect to LO device mismatch for the switching stage of a folded mixer biased at two different current densities can be seen, along with an approximately zero bias current. The higher the current density (J) of switch transistors, the larger the value of dc offset due to device mismatches.

A simulation similar to Choi *et al.* (2007) was performed to evaluate the amount of dc offset due to mismatches for the proposed mixer. Therefore, by biasing the switch transistors at very low dc current density (approximately zero), the effect of device mismatches can be countered without compromising mixer performance, as a folded mixer performs well even when an approximately zero current flows through the switch transistors. A dc offset value of only 6 mV occurs for a device mismatch as high as 20%.

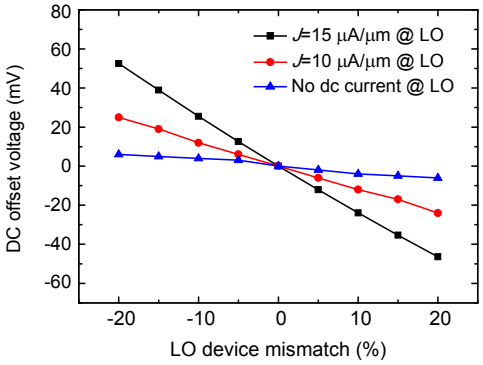

Fig. 4 Simulated dc offset with respect to device mismatch

2.4 Transmission lines

The transmission lines play a vital role in resonating with the intrinsic parasitic capacitance of transistors. The longer transmission lines connected to the input gate and output drain terminals of the transistors resonate out part of the parasitic capacitance, hence enhancing the voltage gain to some ex extent. For the proposed mixer, voltage gain enhancement along with a wider gain curve was observed from simulation results when full-wave electromagnetic (EM) modeled lines for input RF, LO, and interconnects between transconductor's output and switch transistors source terminals were employed, compared to simulation results with parasitic extraction without extracted interconnect inductance.

An inductive quality factor $Q_{\mathrm{L}}=2\omega_0 W_{\mathrm{M}}/P_{\mathrm{R}}$ was defined by Doan *et al.* (2005) for transmission lines resonating with parasitic capacitance (where ω_0 is the resonance frequency, P_{R} is the average power

dissipated in the resistance, and W_M is the average magnetic energy stored), which normally store more magnetic energy than electric energy (W_E). For such inductive lines (W_M>>W_E), the loss of the line is almost completely determined by Q_L according to Doan *et al.* (2005). To implement transmission lines for the mixer with high Q_L, two configurations have been considered (Fig. 5). The first configuration (Fig. 5a) is that of a microstrip line, with the topmost metal (M9) used as the signal line and bottom metal (M1) used as the ground plane. The second configuration is the one shown in Fig. 5b, which is quite similar to a microstrip line with the exception that the substrate is not entirely shielded with the M1 ground plane and a separation S exists between the signal line (M9) and ground plane (M1).

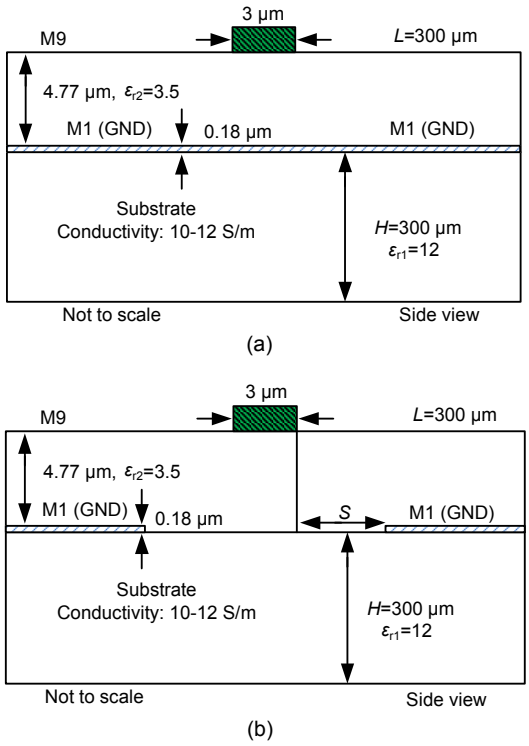

Fig. 5 Two potential transmission line candidates with W=3 μm and L=300 μm: (a) microstrip line; (b) microstrip line without completely shielded substrate

For a microstrip line, close proximity exists between the signal line and ground plane (4.77 μm); thus, the distributed inductance is small, resulting in lowering of Q_L. To mitigate this problem to some extent (at the expense of some electric field penetration into the substrate), the ground plane is separated from signal line with separation S (Fig. 5b), which has an effect of an increase in the value of distributed inductance resulting in an improvement in Q_L.

The increase of the separation S leads to increase of Q_L as the ground is moved away from the signal line, but at the same time electric field penetration into the lossy substrate increases, thereby necessitating an optimization for the value of S. The EM simulation (performed in ADS Momentum) results given in Fig. 6a show that the inductive quality factor (Q_L) increases from approximately three for a microstrip line (MSL) to approximately five for the ground separated line, having a separation value of S=20 μm. For S lower than 20 μm, the value of Q_L is low, whereas for S higher than 20 μm, no significant improvement in Q_L can be seen. The distributed inductance with respect to the input frequency range for different values of S can be seen from Fig. 6b. Clearly, above S=20 μm, no significant improvement in inductance can be seen. Therefore, a separation of S=20 μm was found to be the optimum value for ground separated interconnects.

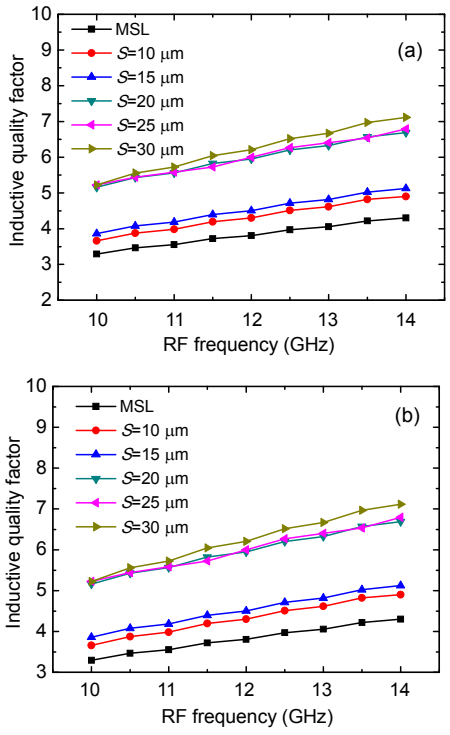

Fig. 6 Inductive quality factor vs. input frequency range with varying S (a) and distributed inductance vs. input frequency range with varying S (b)

3 Measurement results

The chip micrograph of the proposed folded mixer can be seen from Fig. 7. The chip has been fabricated in TSMC's 65 nm 1P9M LP-CMOS process. It covers an area of 564 μm×486 μm, including the pads with an active area of only 0.0179 mm^2.

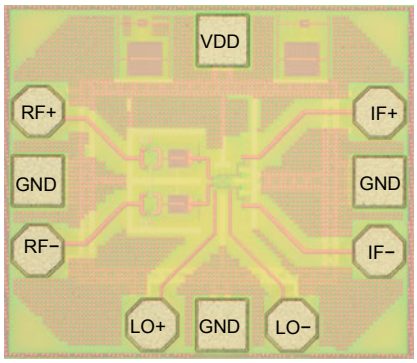

Fig. 7 Chip micrograph of the proposed folded mixer

Measurements have been carried out with RF, LO inputs, and IF outputs probed on-wafer with differential signal−ground−signal (SGS) probes with a pitch of 100 μm. An Agilent E4448A spectrum analyzer and an Agilent N8975A noise analyzer have been used for measurement purposes. KRYTAR hybrids, with operational bandwidths from 1 to 12 GHz and 6 to 26 GHz, were used at the LO and RF inputs, whereas two different baluns with the operating frequency ranging from 10 MHz to 500 MHz and 500 MHz to 7 GHz designed by our institute were used at the IF output.

The measurements have been carried out at a nominal supply voltage of 1.2 V, along with a reduced supply voltage of 1 V for the voltage conversion gain (Fig. 8). An average conversion gain of approximately 9 dB within the desired IF bandwidth with a conversion gain of 8 dB at 1.75 GHz for VDD=1.2 V, along with a conversion gain of 5±0.5 dB for VDD= 1 V can be seen from this figure.

For a supply voltage of 1.2 V, comparison of simulation results and the measured results (Fig. 8) shows that the measured curve deviates from the simulated curve by 2 dB at the far end of the IF bandwidth (f_{IF}=1.75 to 2 GHz). This deviation is mainly due to additional interconnects parasitics, which could not have been accurately modeled during the design procedure. Also, one of the main reasons of bandwidth reduction is the parasitic capacitances present at the input RF terminals and switch transistors source terminals (A, A') (Fig. 2). By employing appropriate valued inductors at these terminals, the bandwidth can be extended further. The mixer consumed a current of 5 mA from a 1.2 V supply voltage, leading to a power dissipation of 6 mW, and a current consumption of only 2 mA for a 1 V supply voltage, leading to a power dissipation of only 2 mW. An LO power of 1 dBm was used for measurements.

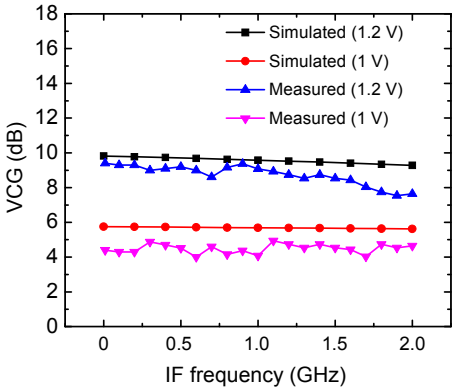

Fig. 8 Measured and simulated voltage conversion gains for VDD=1.2 V and 1 V

The voltage conversion gain variation with respect to LO power for an IF of 10 MHz can be seen from Fig. 9. With an increasing LO power, the switch transistors partially operate in the linear region, leading to a decrease in the conversion gain. The measured $P_{in,1dB}$ of −13 dBm at f_{IF}=10 MHz can be seen from Fig. 10. The isolation between different ports of the mixer can be seen from Fig. 11.

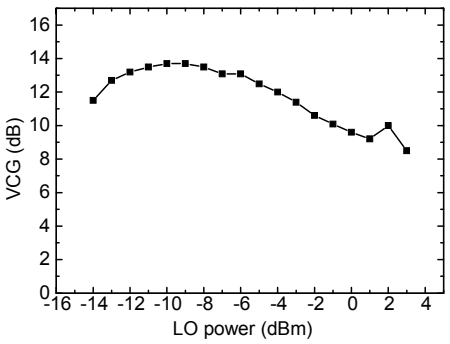

Fig. 9 Conversion gain variation with respect to LO power at an IF=10 MHz

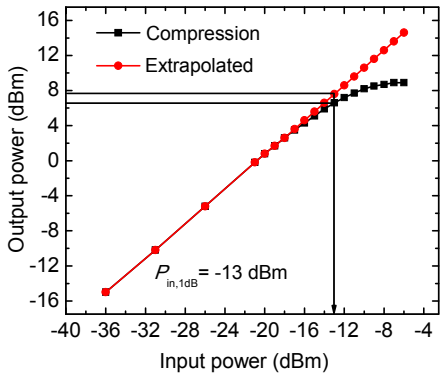

Fig. 10 $P_{in,1dB}$ at an IF of 10 MHz (f_{RF}=12.01 GHz, f_{LO}= 12 GHz)

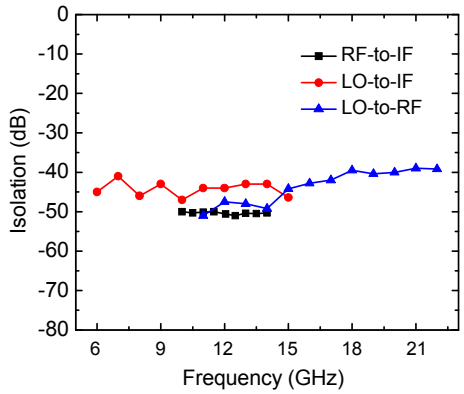

Fig. 11 Isolation characteristics of the proposed mixer (baluns with different frequency ranges were employed to measure isolation)

Depending upon the available baluns with their respective frequency ranges, appropriate baluns were used at different ports. Additional losses due to external transmission lines and components such as dc-blocking capacitors and baluns were later removed from the measured isolation, to determine the actual isolation of the mixer. An isolation of ≥40 dB between mixer ports can be seen.

The screenshot of the spectrum analyzer for a down-converted IF signal at 10 MHz can be seen from Fig. 12. An output buffer matched to 50 Ω accounts for a 10 dB loss along with an insertion loss of 13.5 dB due to external SMA connectors, dc-blocking capacitors, and balun circuitry.

The measured double-sideband (DSB) NF performance of the proposed mixer is shown in Fig. 13a. Due to the limitations of measurement equipment (the lowest operating frequency of the noise analyzer equals 10 MHz), the simulated flicker noise corner frequency is presented along with the measured noise figure in a log-frequency axis (Fig. 13b). The measured and extrapolated noise figure curves in this figure approximate $f_{flicker}$<100 MHz. However, this flicker noise corner frequency is just a vague approximation of the actual flicker noise frequency which is far less than 100 MHz.

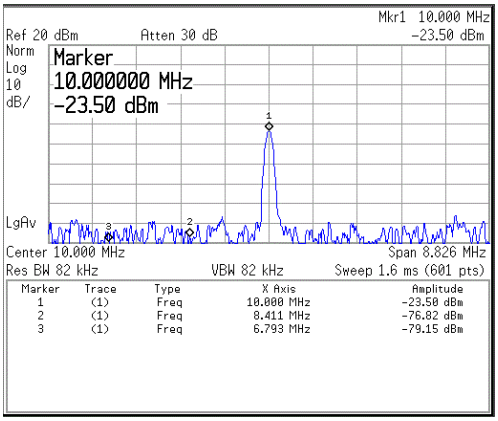

Fig. 12 Snapshot of the spectrum analyzer for an IF of 10 MHz

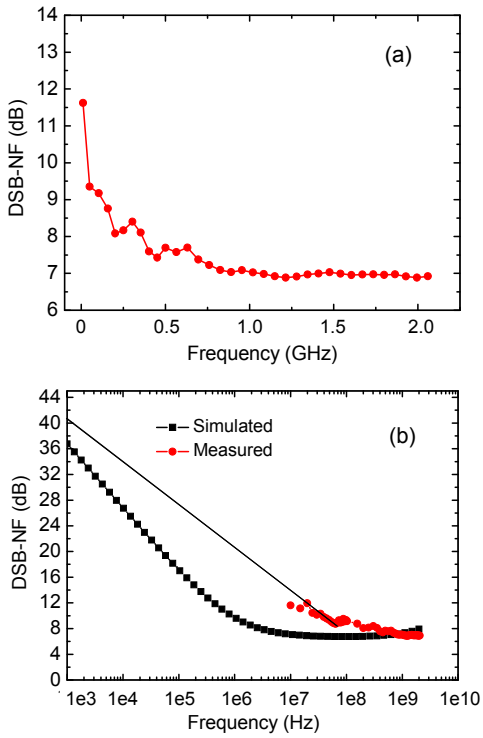

Fig. 13 Double sideband noise figure (DSB-NF): (a) linear IF axis; (b) simulated NF along with measured and extrapolated NF curves in a log-frequency axis

4 Conclusions

The conventional Gilbert mixer is unsuitable for low supply voltages due to its stacked architecture. To resolve the problem of voltage headroom and achieve an optimum performance from the mixer in terms of high conversion gain and low noise figure, folded mixer topology must be employed. A folded mixer design for a 60 GHz receiver in a 65 nm LP-CMOS process has been presented in this work.

The folded mixer employing an ac-coupled self-bias current reuse topology for its transconductance stage shows good performance in terms of conversion gain, noise figure, and linearity. A performance related comparison between this work and other published works can be seen from Table B1 in Appendix B. The performance of a mixer can be evaluated in terms of its figure of merit (FOM) in dB. The higher its value, the better the performance of a mixer. As can be seen from Table B1, a good FOM has been achieved for the proposed mixer compared to other works.

References

Afshar, B., Wang, Y., Niknejad, A.M., 2008. A robust 24 mW 60 GHz receiver in 90 nm standard CMOS. IEEE Int. Conf. on Solid-State Circuits, p.182-605. [doi:10.1109/ISSCC.2008.4523117]

Amin, N.M., Wang, Z., Kuan, B., *et al*., 2012. 1.2 V folded down-conversion wideband mixer in 65 nm CMOS. IEEE Int. Conf. on Electron Devices and Solid-State Circuits, p.1-4. [doi:10.1109/EDSSC.2012.6482774]

Cai, D., Yang, S., Hao, Y., *et al*., 2013. Design of ultralow-power 60 GHz direct-conversion receivers in 65 nm CMOS. *IEEE Trans. Microw. Theory Techn.*, **61**(9):3360-3372. [doi:10.1109/TMTT.2013.2268738]

Chiou, H.K., Lin, K.C., Chen W.H., *et al*., 2012. A 1 V 5 GHz self-bias folded-switch mixer in 90 nm CMOS for WLAN receiver. *IEEE Trans. Circ. Syst. I*, **59**(6):1215-1227. [doi:10.1109/TCSI.2011.2173399]

Choi, K., Shin, D.H., Yue, C.P., 2007. A 1.2 V, 5.8 mW, ultra-wideband folded mixer in 0.13 μm CMOS. IEEE Int. Symp. on Radio Frequency Integrated Circuits, p.489-492. [doi:10.1109/RFIC.2007.380930]

Darabi, H., Abidi, A.A., 2000. Noise in RF-CMOS mixers: a simple physical model. *IEEE J. Solid-State Circ.*, **35**(1):15-25. [doi:10.1109/4.818916]

Doan, C.H., Emami, S., Niknejad, A.M., *et al*., 2005. Millimeter-wave CMOS design. *IEEE J. Solid-State Circ.*, **40**(1):144-155. [doi:10.1109/JSSC.2004.837251]

Furuta, Y., Heima, T., Sato, H., *et al*., 2007. A low flicker-noise direct conversion mixer in 0.13 μm CMOS with dual-mode DC offset cancellation circuits. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, p.265-268. [doi:10.1109/SMIC.2007.322809]

Hampel, S.K., Schmitz, O., Tiebout, M., *et al*., 2010. Inductorless low-voltage and low-power wideband mixer for multistandard receivers. *IEEE Trans. Microw. Theory Techn.*, **58**(5):1384-1390. [doi:10.1109/TMTT.2010.2042894]

Hermann, C., Tiebout, M., Klar, H., 2005. A 0.6 V, 1.6 mW transformer based 2.5 GHz down-conversion mixer with +5.4 dB gain and −2.8 dBm IIP3 in 0.13 μm CMOS. *IEEE Trans. Microw. Theory Techn.*, **53**(2):488-495. [doi:10.1109/TMTT.2004.840762]

Klumperink, E.A.M., Louwsma, S.M., Wienk, G.J.M., *et al*., 2004. A CMOS switched transconductor mixer. *IEEE J. Solid-State Circ.*, **39**(8):1231-1240. [doi:10.1109/JSSC.2004.831797]

Marcu, C., Chowdhury, D., Thakkar, C., *et al*., 2009. A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry. *IEEE J. Solid-State Circ.*, **44**(12):3434-3447. [doi:10.1109/JSSC.2009.2032584]

Poobuapheun, N., Chen, W.H., Boos, Z., *et al*., 2007. A 1.5 V 0.7–2.5 GHz CMOS quadrature demodulator for multi-band direct-conversion receivers. *IEEE J. Solid-State Circ.*, **42**(8):1669-1677. [doi:10.1109/JSSC.2007.900294]

Razavi, B., 1988. RF Microelectronics. Prentice Hall, New Jersey, USA, p.17-22.

Razavi, B., 2009. Design of millimeter-wave CMOS radios: a tutorial. *IEEE Trans. Circ. Syst. I*, **56**(1):4-16. [doi:10.1109/TCSI.2008.931648]

Safarian, A.Q., Yazdi, A., Heydari, P., 2005. Design and analysis of an ultrawide-band distributed CMOS mixer. *IEEE Trans. VLSI Syst.*, **13**(5):618-629. [doi:10.1109/TVLSI.2005.844288]

Tomkins, A., Aroca, R.A., Yamamoto, T., *et al*., 2009. A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link. *IEEE J. Solid-State Circ.*, **44**(8):2085-2099. [doi:10.1109/JSSC.2009.2022918]

Vecchi, F., Bozzola, S., Temporiti, E., *et al*., 2011. A wideband receiver for multi-Gbit/s communications in 65 nm CMOS. *IEEE J. Solid-State Circ.*, **46**(3):551-561. [doi:10.1109/JSSC.2010.2100251]

Vidojkovic, V., van der Tang, J., Leeuwenburgh, A., *et al*., 2005. A low voltage folded-switching mixer in 0.18 μm CMOS. *IEEE J. Solid-State Circ.*, **40**(6):1259-1264. [doi:10.1109/JSSC.2005.848034]

Wang, C., Wan, Q., 2011. A 0.18 μm CMOS low noise amplifier using a current reuse technique for 3.1–10.6 GHz UWB receivers. *J. Semicond.*, **32**(8):085002. [doi:10.1088/1674-4926/32/8/085002]

Appendix A

The small-signal equivalent circuit of a self-bias current reuse transconductance stage (Fig. 2), without any output loading from the subsequent stage, can be seen from Fig. A1.

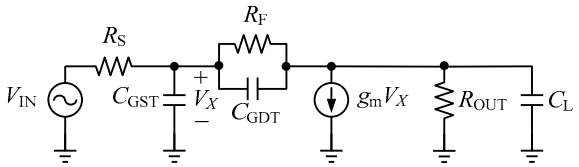

Fig. A1 Small signal equivalent circuit of a self-bias transconductor

In this figure, $C_{GST}=C_{GS,\,NMOS}+C_{GS,PMOS}$, $C_{GDT}=C_{GD,NMOS}+C_{GD,PMOS}$, $C_L=C_{DB,NMOS}+C_{DB,PMOS}$, $R_{OUT}=r_{ds,NMOS}//r_{ds,PMOS}$ and $Z_1=R_F//(1/(sC_{GDT}))$. To derive the input impedance, C_{GST} has been ignored for simplicity. Therefore, the voltage V_X at node X can be given as

$$V_X = I_X Z_1 + (I_X - g_m V_X)\frac{R_{OUT}}{R_{OUT}sC_L + 1}. \quad \text{(A1)}$$

Rearranging Eq. (A1) gives the following expression for input impedance:

$$\frac{V_X}{I_X} = \frac{(R_{OUT}sC_L + 1)Z_1 + R_{OUT}}{R_{OUT}sC_L + 1 + g_m R_{OUT}}. \quad \text{(A2)}$$

At frequencies where $|R_{OUT}sC_L|<<1$ and $|R_{OUT}sC_L|<<1+g_mR_{OUT}$, Eq. (A2) reduces to

$$\frac{V_X}{I_X} = \frac{Z_1 + R_{OUT}}{1 + g_m R_{OUT}}. \quad \text{(A3)}$$

Substituting Z_1 in Eq. (A3) gives

$$\frac{V_X}{I_X} = \frac{R_F + R_{OUT}(R_F sC_{GDT} + 1)}{(R_F sC_{GDT} + 1)(1 + g_m R_{OUT})}. \quad \text{(A4)}$$

The actual input impedance consists of a parallel combination of Eq. (A4) and $1/(sC_{GST})$. At higher frequencies, both Eqs. (A2) and (A4) contain real and imaginary parts. For simplicity, we again assume that at frequencies where $|R_F sC_{GDT}|<<1$, Eq. (A4) can be reduced to

$$\frac{V_X}{I_X} = Z_{IN} = \frac{R_F + R_{OUT}}{1 + g_m R_{OUT}}. \quad \text{(A5)}$$

Appendix B

Table B1 Performance summary with comparison to other works

Parameter	Value/Description						
	Hermann *et al.* (2005)	Klumperink *et al.* (2004)	Furuta *et al.* (2007)	Poobuapheun *et al.* (2007)*	Safarian *et al.* (2005)	Hampel *et al.* (2010)	This work
Process	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.18-μm CMOS	65 nm CMOS	65 nm CMOS
RF frequency (GHz)	2.1–3	0.3–4	0.85–2.1	0.7–2.5	3–8.72	1–10.5	10.25–13.75
CG_{max} (dB)	5.4	11	13.2	38	5	14.5	≈10
$P_{in,1dB}$ (dBm)	–9.2	NA	–6	–25.8	NA	–13.8	–13
IIP3 (dBm)	3.5	4.1	4.5	11	5	–4.2	–3.4**
NF_{min} (dB)	14.8 (SSB)	14 (SSB)	12.3 (DSB)	10 (DSB)	6.8	6.5 (DSB)	7 (DSB)
P_{DC} (mW)	1.6	6.6	8.25	24	10.4	14.4	6
VDD (V)	0.6	1	1.5	1.5	1.8	1.2	1.2
FOM*** (dB)	9.45	10.3	9.37	22.6	10	9.037	10.5
Area (mm^2)	NA	0.0048	NA	NA	1.624	0.011	0.017

* Including narrowband opamp; ** IIP3=$P_{-1\,dB}$+9.6 (Razavi, 1988); *** $\mathrm{FOM}=10\lg\left(\frac{10^{G/20}\cdot 10^{(\mathrm{IIP3}-10)/20}}{10^{\mathrm{NF}/10}P(\mathrm{mW})}\right)$