3 Mm-wave CMOS PA design with linearity analysis

3.1 Differential PA design

A schematic of the differential PA design (PA4) along with a photograph of the fabricated chip in Globalfoundries 45 nm CMOS SOI technology are shown in Fig. 6. To ensure the operation of the frequency band, a 120 μm wide transistor is chosen. Considering that the knee voltage of the transistor is approximately 0.3 V, the peak source-drain swing is 1.2 V. To prevent breakdown of the uppermost transistor in the stack structure and stabilize the circuit operation, the maximum bias voltage of the transistors used in this paper is selected to be 1 V.

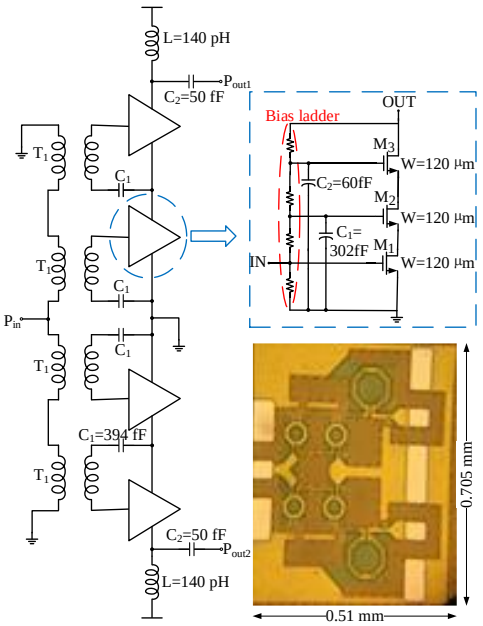

Fig. 6 Schematic and chip photograph of the differential power amplifier (PA4) implemented in this work

The input signal is converted through the transformer network to a differential signal amplified by two stacked power units, each giving a DC bias voltage of 6 V. The single-sided circuit has a triple stack per power cell, and the overall voltage swing can reach six transistors. Compared with the common source and cascode, the triple stack structure has higher gain, better isolation, better stability, and higher output impedance. C1 blocks the DC signal. C2 regulates the output signal phase while forming part of the impedance matching network. Compared to the single-ended design PA1, PA4 was further optimized to push the operation into deep class AB, resulting in a lower power gain, but slight improvements in both output power and PAE. Two-way differential combination increases the output power, and PAE improvement is achieved by adjusting the values of the resistors in the resistor ladder to set a slightly smaller drain current in the stack to make the transistor work in the deep class AB region.

Two voltage transformers T1 in series are used at each input, and the main coil is connected in series to 50 Ω to match the input, coupling the power into the transistor. To optimize the planar input transformer T1's width, radius and metal gaps, ANSYS Electronics is applied to realize a reasonably high Q and suitable inductance for input matching. As Fig. 7a and Fig. 7b show, the transformer utilizes the top metal lb as the primary coil, and ua and ub work together for the secondary coil. A coupling coefficient of nearly 0.7 is achieved to eliminate the magnetic flux and thus hysteresis loss and eddy current in transformer operation.

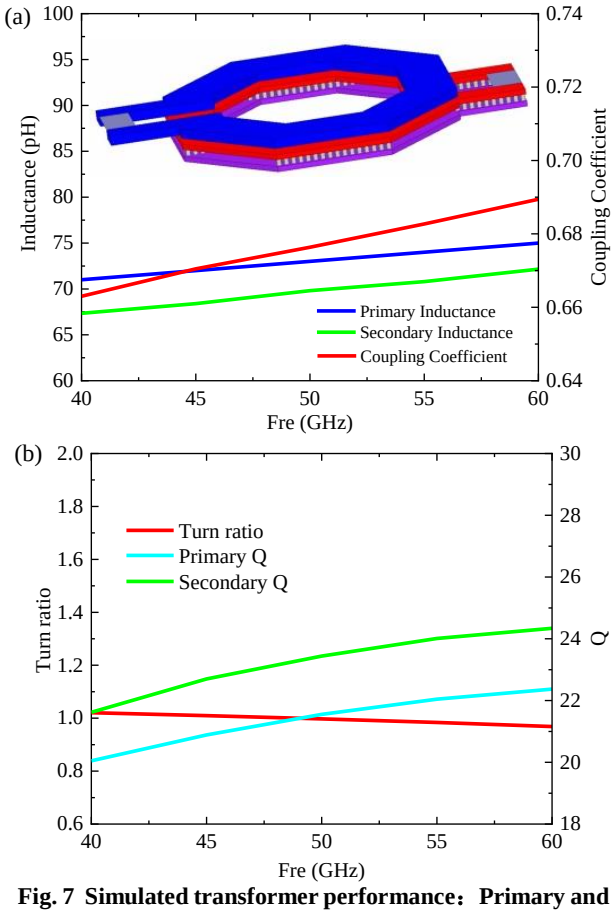

Fig. 7 Simulated transformer performance: Primary and secondary inductance and coupling coefficient (a), Primary and secondary Q value and turns ratio (b)

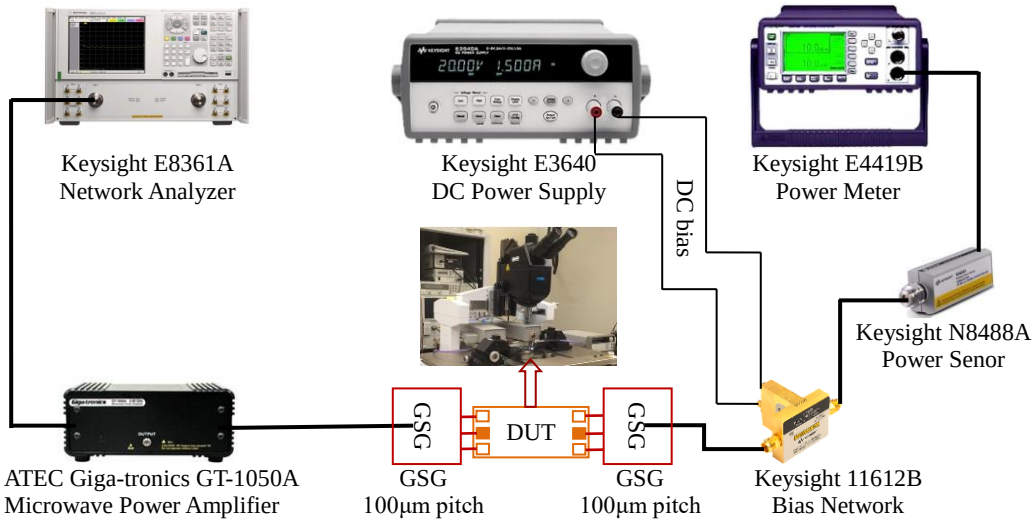

Fig. 8 Power measurement set up

3.2 Measurement results

Power measurements were preformed using Keysight E4419B power meters along with a Keysight N8488A power sensor at room temperature. The input power is provided by a Keysight E8361A PNA and a Giga-Tronic GT-1050A driver amplifier. Set the PNA as the signal source to CW mode, and the operating frequency is 44 GHz. The input power sweep range is from -20 dBm to 20 dBm. The characterization setup is illustrated in Fig. 8.

Before testing, the vector network instrument was turned on for a period of time to prevent subsequent temperature deviation. Use the GSG probe to calibrate the vector network analyser, and use the SOLT calibration technique, that is, by measuring the calibration piece with known characteristics (short-circuit, open circuit, load, through). After calibration, import the calibration results. The sweep frequency range was set to 35 GHz-55 GHz, the input signal power was set to 0 dBm, and the four S-parameter curves were obtained. Fig. 9 shows the measured S parameters of PA4, which closely confirm the simulation. A small signal gain of a maximum of 13.4 dB is seen at 47 GHz. To deal with the problem that the measured S-parameters shift to low frequency, the results are mainly caused by spurious and interference that are not considered. When we simulate, we match the circuit to high frequency to approximately 48 GHz.

Use the continuous wave generated by the signal source to test the power performance of the power amplifier. To accurately calibrate the power to the probe level, test all input power and input frequency three times, respectively, for straight-through, only load the input cable, and only load the output cable, calculate the actual transmission loss of each probe, and then weight them separately. to actual input power and output power for accurate on-chip performance. Fig. 10 shows the simulation and measured power performance, including output power P_{out}, power gain Gain, and PAE versus input power at 44 GHz under two bias conditions of 4.8 V (0.8 V/transistor) and 6 V (1 V/transistor).

The power amplifier uses a single-ended measurement technique, where one output was terminated with a 50 Ω load. Upon switching the output terminals, no discrepancy between the two output levels was observed. Under a supply voltage of 6 V and at 44 GHz, Differential PA4 delivers a maximum differential output power of 25.2 dBm and a maximum PAE of 47% with a linear differential gain of 11.4 dB, which agrees well with the simulation results. As shown in Fig. 10, the output power of the PA is still not saturated, and the maximum PAE point is not yet achieved. The setup losses, relatively small power gain and limited output power capability of the driver amplifier are the reasons that this PA cannot be characterized to its full potential. Moreover, the design shows a class AB behavior with a gain expansion for input powers up to 7 dBm and gain compression

for higher input powers. With a smaller supply voltage of 4.8 V, the maximum differential output power is reduced to 23.7 dBm and PAE is reduced to 38%. Comparing the simulated and measured results under the two bias conditions, increasing the value of V_{oQ} improves the overall circuit performance including linearity, output power, gain and PAE. The increase in power supply energy allows the device gain to be maintained.

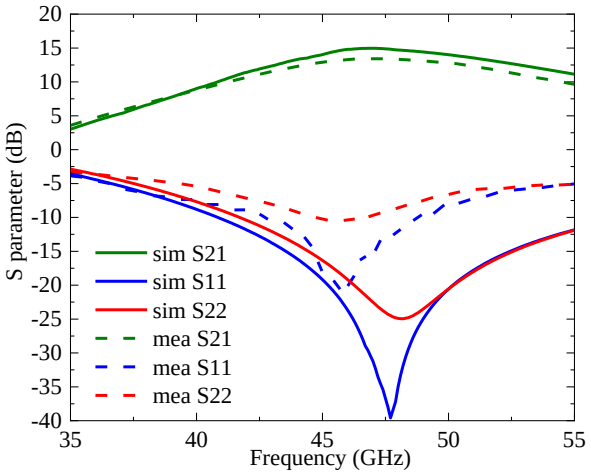

Fig. 9 Measured (dash line) and simulated (solid line) S parameters of the fabricated differential PA4 chip under 6V supply

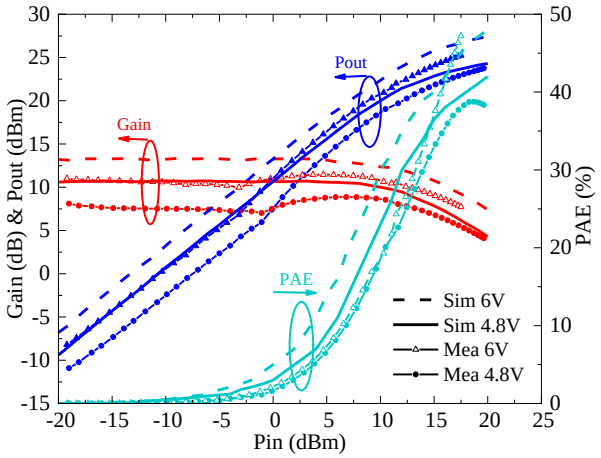

Fig. 10 Simulation and power measurements for the differential PA (PA4) at 44 GHz under two different bias conditions (4.8 V and 6 V)

Fig. 11 shows the simulation and measurement results of power characterizations of the differential PA (PA4) over a frequency range of 44 to 50 GHz. The comparison is also performed using two different values of supply voltage, namely, 4.8 V and 6 V. As shown in the figure the best output power and PAE performance are achieved at 44 GHz under a supply bias of 6 V. The maximum PAE under this bias condition decreases monotonically to 25% at 48 GHz and then increases slightly to 26% at 50 GHz. The maximum output power decreases from 25.2 dBm to 24.2 dBm as the frequency increases from 44 GHz to 50 GHz. The power gain reaches 13 dB at 46 GHz and then slightly decreases as the frequency increases to 50 GHz which agrees with the simulation results. The saturated output power remains close to 25 dBm for all the measured frequencies at a bias supply of 6 V. When the supply voltage is reduced to 4.8 V, all power performance metrics deteriorate except for the maximum PAE at 48 GHz and 50 GHz, which are slightly higher than those achieved with a 6 V power supply. In general, this mm-wave PA delivers excellent output power and PAE performance in the measured frequency range of 44 GHz to 50 GHz.

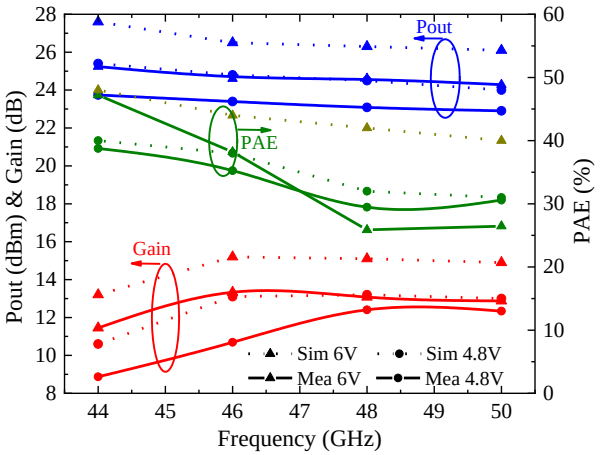

Fig. 11 Power simulation and measurement (P_{out}, Gain, PAE) vs. frequency for the differential PA (PA4) under two bias conditions (4.8 V & 6V)

3.3 Linearity analysis

As only one mm-wave signal source was available for testing, linearity characterizations based on two-tone measurement and complex modulation schemes (such as the WCDMA test) were not feasible. Instead, an IIP_3 simulation for the proposed differential PA4 under 6 V supply is shown in Fig. 12. It lists the 44 GHz and 50 GHz IIP_3 results of gain and third-order intermodulation distortion points with a

50 MHz gap. They further demonstrate our linearity analysis mentioned before for weakly nonlinear power amplifiers operating in class AB mode such as the mm-wave PA studied here. As OP_{1dB} relates to OIP_3 through Eq. (18), a measured above 19.4 dBm OP_{1dB} across 44 GHz to 50 GHz with a peak of 21.5 dBm at 44 GHz of PA4, which has been shown in Fig. 5, also reflects the linearity theory's accuracy. The differential PA4 design outperforms the other PAs (PA1-3) in terms of maximum linear output power P_{1dB} by at least 2 dB.

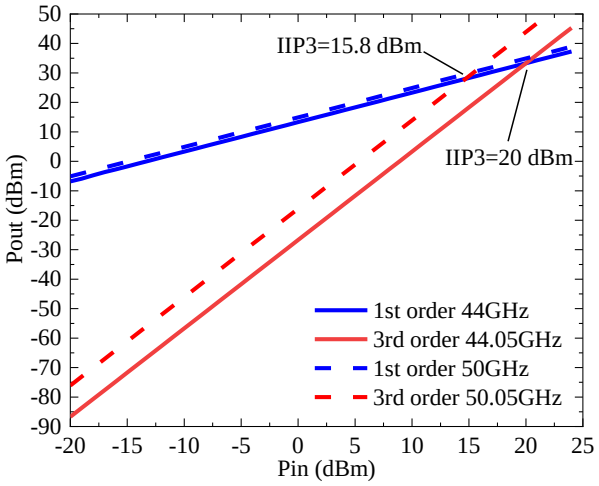

Fig. 12 IIP_3 simulation results of the differential PA4

4 Conclusion

Table 2 shows the performance comparison of U-band CMOS amplifiers. SOI CMOS shows its advantages in power and efficiency. Based on Globaldoundries 45 nm CMOS SOI technology, to improve the linearity of the circuit, after the calculation of OIP3, we can roughly estimate the value of P_{1dB}, and then select the size of the stacked transistor appropriately. We use the single-ended to differential two-way power amplification to combine to improve the output power, which will bring about the result of decreased efficiency. We improve PAE by adjusting the bias current of the power cell, reducing the DC power consumption of each channel, and making the transistor work in the deep AB region. To the authors' knowledge, PA4 with a maximum linear power of 25.24 dBm and maximum PAE of 47% measured at 44 GHz is the most efficient mm-wave CMOS power amplifier reported to date.

A linearity analysis that takes into account the nonlinearities of the transistor current and capacitances is introduced. The analysis leads to calculated OIP_3 values for cascode and triple cascode cells (Eqs. (11) and (18), respectively). The analysis also predicts the linearity of PA1 and PA2, indicating that PA1 (and PA4) that are designed based on the stacking of triple cascode cells are superior designs in terms of linearity. The differential power amplifier (PA4) has the best P_{1dB} value (21.5 dBm at 44 GHz) and is better than all the single-ended power amplifiers presented here. Considering the troublesome testing process of the differential structure, we will find a way to design a differential-to-single-ended balun to synthesize two paths of power to facilitate testing.

Contributors

Jie CUI designed the research. Weixing SHENG and Peipei LI processed the data. Jie CUI drafted the manuscript. Weixing SHENG and Peipei LI helped organize the manuscript. Jie CUI, Weixing SHENG and Peipei LI revised and finalized the paper.

Table 2 Comparison with prior-art U-band CMOS PAs

Reference	Technology	Frequency (GHz)	Gain (dB)	P_{SAT} (dBm)	Peak PAE(%)	P_{1dB} (dBm)
Chen et al. (2014)	130 nm CMOS	60	8.6	10.8	8.4	9.36
Jiang et al. (2017)	90 nm CMOS	45	20.3	21	14.5	17.8
Vigilante and Reynaert (2018)	28 nm CMOS	43	20.8	15.9	18.4	11.1
Xia et al. (2018)	45 nm CMOS SOI	57.2	15	18.5	25.5	16.2
Li et al. (2019)	45 nm CMOS SOI	39	15.6	18.9	36	17.4
Park et al. (2019)	28 nm CMOS	38.5	25.8	16.8	32.9	14.9
Wang et al. (2020)	28 nm CMOS	41	17.6	14.7	26.2	13
Mayeda et al. (2021)	22 nm FD-SOI	37	10.9	17.1	21.7	16.6
This work	**45 nm CMOS SOI**	**44**	**11.4**	**25.24**	**47.2**	**21.5**
		50	**12.8**	**24.2**	**26.1**	**19.3**

Compliance with ethics guidelines

Jie CUI, Weixing SHENG and Peipei LI declare that they have no conflict of interest.

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