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One-dimensional reconfigurable three-stage Doherty power amplifier with load mismatch resilience*

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Abstract: This article presents a comprehensive theoretical analysis of the resilience demonstrated by the three-stage Doherty power amplifier (DPA) when operating under load mismatch conditions. Additionally, a novel reconfigurable three-stage DPA architecture is introduced, with the aim of enhancing resilience to load mismatch using of exceptionally simple circuits and a one-dimensional (1-D) control method. To validate the efficacy of this proposed architecture and control approach, a DPA prototype employing commercial gallium nitride (GaN) active devices has been designed and meticulously fabricated at 2 GHz. With a matched 50 Ω load, the fabricated three-stage DPA achieves a high-efficiency range of 9.5 dB with $\geq$ larger than 51% back-off drain efficiency (DE). Through the proposed 1-D control, the DPA presents 47.0% - 55.1% back-off efficiency with $\leq$ 2 dB power fluctuation at a 2:1 voltage standing wave ratio (VSWR) over a 360° phase span. When driven by a 20 MHz long term evolution (LTE) signal with an 8 dB peak to average power ratio (PAPR), the DPA achieves 46.2% - 53.9% average efficiency and better than -21 dBc adjacent channel power ratio (ACPR) without digital pre-distortion (DPD) under load mismatch conditions.

Key words: Doherty power amplifier; Load mismatch; 1-D control; Reconfigurable; Three-stage
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1 Introduction

As wireless communication systems transition into the 5G era, MIMO and phased array technologies are extensively utilized to boost spectral efficiency and enable beam scanning capabilities. However, with the increasing popularity of large-scale arrays, the integration of nonreciprocal components, such as circulators and isolators, into wireless communication equipment has become a crucial design challenge. This poses a significant obstacle, as the load condition of array systems often varies with different beam scanning configurations. Consequently, there is a strong demand for wireless communication equipment that exhibits resilience against load mismatches. Additionally, the compact size requirements of terminal devices present a similar challenge, further emphasizing the need for innovative solutions in this domain.

Power amplifiers (PAs), as the active component closest to the antenna in the transmitter, are normally sensitive to load mismatch, which can seriously affect their performance in current and future wireless communication systems. Moreover, to adapt to the widely adopted high peak-to-average power ratio (PAPR) signal characteristics, PA architectures with a large high-efficiency range such as Doherty power amplifier (DPA) (Fang et al., 2018; Nikandish et al., 2020; Zhou et al., 2020; Pang et al., 2022) and out-phasing (Barton, 2016; Barton et al., 2016; Wang et al., 2020) have been widely used, and these architectures present even worse load mismatch

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adaptability due to their more complex circuits. To improve the PA load resilience, several techniques have been explored in recent years, such as dynamic supply voltage (Gonçalves et al., 2021, 2022), six-port network load mismatch correction(Singh et al., 2021), reconfigurable output matching network (OMN) (Donahue et al., 2020), digital Doherty architecture (Hu et al., 2015), dual-mode Doherty operation (Lyu and Chen, 2020; Lyu et al., 2021; Lyu and Chen, 2022; Shi et al., 2023) and modified load modulated balanced amplifier (LMBA)(Quaglia et al., 2022b; Guo et al., 2023).

It is noteworthy to mention that, due to the originally employed PA architectures, the majority of resilience enhancement methods currently available offer a high-efficiency range of $\leq$ 6 dB. This falls short of satisfying the signal PAPR requirements, which typically range from 8 dB to 12 dB for 5G and beyond 5G systems. In efforts to expand the high-efficiency range for normal matched loads, several techniques have been explored. These include asymmetrical (Kim et al., 2011; Jang et al., 2014; Pang et al., 2016) and multi-way/multi-stage Doherty architectures (Neo et al., 2007; Golestaneh et al., 2013; Xia et al., 2019; Gao et al., 2022; Zhou et al., 022a; Piacibello et al., 2023), DPAs employing complex combining loads (Fang and Cheng, 2014), load-modulated balanced amplifiers (LMBA) with extended high efficiency ranges (Quaglia and Cripps, 2018; Cao et al., 2019, 2021; Quaglia et al., 2022a), distributed efficient power amplifiers (DEPA) (Saad et al., 2018; Lv et al., 2022), and circulator load-modulated power amplifiers (CLMA) (Zhou et al., 022b, 2023). However, despite their ability to expand the high-efficiency range, these amplifier architectures often lack mismatch resilience either.

Recently, a three-way dual-mode DPA architecture has been introduced, exhibiting a remarkably high-efficiency range against load mismatch (Pang et al., 2024). This innovation underscores the potential of multi-branch Doherty architectures to simultaneously achieve an extensive high-efficiency range and resilience against load mismatch. Nevertheless, the dual-mode reciprocal gate bias configuration employed in the three-way DPA, as described in (Pang et al., 2024), necessitates the control of numerous circuit variables. This increases the complexity of the circuits, echoing the challenges encountered in other dual-mode DPAs (Li et al., 2019; Lyu et al., 2021; Lyu and Chen, 2022; Shi et al., 2023). To address this challenge, a modified sequential LMBA was introduced in (Guo et al., 2023), which uses one-dimensional (1-D) drain voltage control to achieve a significant high-efficiency range against load mismatch. This approach effectively reduces the number of circuit control variables. However, controlling the large drain current remains a challenge, limiting the application of this method in high-power scenarios.

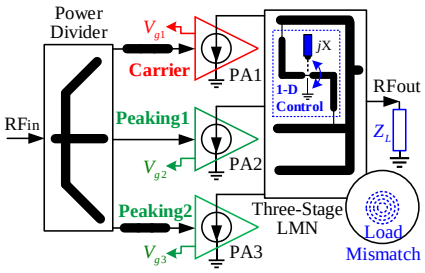


Fig 1 Proposed three-stage DPA architecture. DPA, Doherty power amplifier; LMN, load modulation network; PA, power amplifier.

In this paper, we propose a novel three-stage DPA architecture that provides a large high-efficiency range against load mismatch, achieved through the utilization of a 1-D control method. The mismatch adaptability of three-stage DPAs is analyzed in detail based on a nonlinear active device model. Additionally, a simple 1-D control circuit is introduced to enhance the mismatch resilience of the proposed DPA, by changing the reactance conditions at a single control port in the proposed load modulation network (LMN).

The remainder of this paper is structured as follows: Section 2 delves into the theoretical analysis of the proposed three-stage DPA, providing a comprehensive understanding of its underlying principles. Section 3 outlines the detailed design procedures for implementing the proposed three-stage DPA using commercial gallium nitride (GaN) transistors. In Section 4, we present the measurement results of the fabricated DPA, highlighting its performance and validating our theoretical analysis. Finally, Section 5 concludes the article, summarizing the findings and contributions.

2 Theoretical analysis

By harnessing the diverse responses exhibited by various branches in the multi-branch architecture to alterations in load impedance, it is possible to

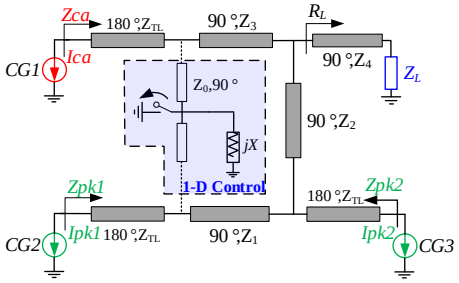


Fig 2 Theoretical block diagram of the proposed sub-network. CG, current generator.

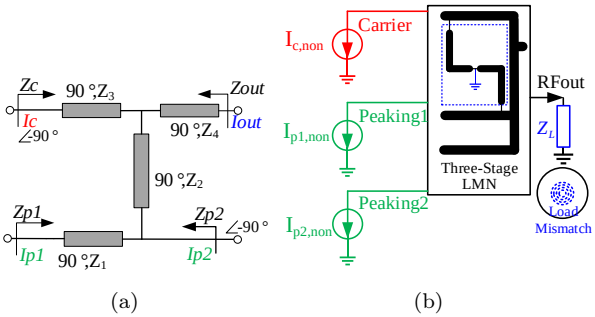


Fig 3 Proposed initial three-stage DPA LMN when 1-D control grounded: (a) theoretical block diagram and (b) schematic to analyze the three-stage DPA performance under load mismatch conditions using nonlinear current models. DPA, Doherty power amplifier; LMN, load modulation network.

partially enhance the impedance mismatch resilience of the PA, a prime example of this is the balanced PA. Similarly, according to the theory of transmission lines, for a 90° transmission line, the change of impedance at its ends has an opposite trend when the load changes. Therefore, it can be hypothesized that a PA constructed utilizing this structure has the potential to compensate for impedance transformations at both ports, mitigating the effects of load mismatch and thus enhancing resistance to such mismatches.

The three-stage DPA architecture has proven to be an effective way to increase the high-efficiency range. In this architecture, the carrier PA and one of the peaking PAs have a 90° phase difference. According to previous conjectures, the structure may be able to guarantee a high-efficiency range in the case of load mismatch. To discuss this ability, a nonlinear model of the current source will be established in this section to analyze the load impedance mismatch resistance of the three-stage DPA architecture. Meanwhile, a simple 1-D circuits control method will be proposed to improve the load mismatch resilience.

The architecture of the proposed three-stage DPA is shown in Fig. 1. The input power is distributed to three identical sub-PAs using a three-way equal power divider. At the output port, a modified three-stage LMN is used to combine the output power of the three sub-PAs and provide the three-stage Doherty operation. By adding a reconfigurable 1-D control network between the carrier PA and peaking PA1, the reactance condition at the control port can be changed based on different load mismatch conditions, thereby improving mismatch resilience. To ensure that the currents are in the same phase at the combiner, some phase compensation lines are added in front of the sub-PAs. The load mismatch resilience performance of the proposed three-stage DPA will be discussed in detail later in this section.

2.1 Load mismatch analysis of three-stage DPA using non-Linear current model

In order to analyze the operation of the proposed architecture, the modified three-stage DPA LMN in Fig. 1 is simplified to the theoretical block diagram shown in Fig. 2, where current generators (CGs) are used instead of sub-PAs, I_{ca} denotes the current of the carrier PA, and I_{pk1} and I_{pk2} denote the currents of two peaking PAs, respectively.

When the load is matched, no control is added, and the transmission line is grounded to counteract its effect according to the characteristics of the 90° transmission line, which is then operated as shown in Fig. 3(a). From Golestaneh et al. (2013), the impedance of 90° transmission lines that comprises the structure can be expressed as

$$\begin{cases} Z_1 = \dfrac{R_{opt}}{k_2(\frac{1}{k_1}-1)} \\ Z_2 = \sqrt{\dfrac{R_L \cdot R_{opt}}{k_1}} \cdot \dfrac{1}{(\frac{1}{k_1}-1)} \\ Z_3 = \sqrt{\dfrac{R_L \cdot R_{opt}}{k_1}} \\ Z_4 = \sqrt{Z_L \cdot R_L} \end{cases} \tag{1}$$

where k_1 indicates the ratio of input current to transistor saturation current when peaking1 is turned on, k_2 indicates the ratio of input current to transistor saturation current when peaking2 is turned on, and R_{opt} indicates the optimum load impedance of the

transistor. In this paper, we choose $k_1 = 1/3$, $k_2 = 0.5$, and $R_L = R_{opt}$ to achieve a high-efficiency range of 9.5 dB.

In Fig. 2, 180° transmission lines are used between the output of CGs and LMN as OMNs for load modulation, with the characteristic impedance Z_{TL} of R_{opt}, do not participate in the load modulation process as part of the impedance transformation, thus simplifying the theoretical architecture of Fig. 2 to the four-port networks shown in Fig. 3(a), where Z_c, Z_{p1}, Z_{p2}, Z_{out} and I_c, I_{p1}, I_{p2}, I_{out} denote the impedance and current of each port, respectively. The voltage-current relationship between the ports of the simplified structure shown in Fig. 3(a) can be expressed as

$$\begin{bmatrix} V_c \\ V_{p1} \\ V_{p2} \\ V_{\text{out}} \end{bmatrix} = \hat{\mathbf{Z}}\mathbf{1} \begin{bmatrix} I_c \\ I_{p1} \\ I_{p2} \\ I_{\text{out}} \end{bmatrix} \tag{2}$$

where V_c, V_{p1}, V_{p2}, V_{out} denote the voltage of each port, respectively. $\hat{Z}$ denotes the Z-parameter matrix of LMN network.

Based on the voltage-current transformations at each port, the Z-parameter matrix of Fig. 3(a) at the center frequency is derived as

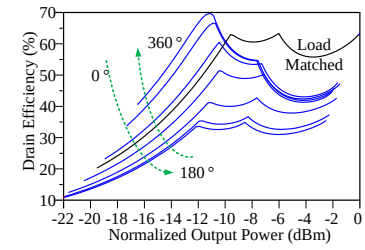
$$\hat{\mathbf{Z}}\mathbf{1} = R_{opt} \begin{bmatrix} 0 & -j2 & 0 & 0 \\ -j2 & 0 & +j & -j\frac{5}{2\sqrt{3}} \\ 0 & +j & 0 & 0 \\ 0 & -j\frac{5}{2\sqrt{3}} & 0 & 0 \end{bmatrix} \tag{3}$$

To simplify the analysis, the currents mentioned in Fig. 3(a) and (2) refer only to the current amplitude, and its phase correspondence can be described as

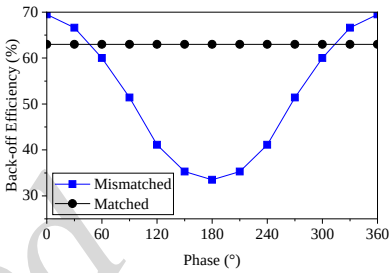
$$\left[\; I_{ca}, \quad I_{pk1}, \quad I_{pk2} \; \right] = \left[\; -jI_c, \quad I_{p1}, \quad -jI_{p2} \; \right] \tag{4}$$

To ensure the three-stage Doherty operation, the linear current relationship of the sub-PAs can be described as

$$I_c = \begin{cases} I_{max} \cdot v_{in}, 0 \le v_{in} < V_{\max} \\ I_{max}, v_{in} \ge V_{max} \end{cases} \tag{5}$$



(a)



(b)

Fig 4 Theoretical DE versus normalized output power when VSWR = 2:1: (a) [0°,360°] and (b) DE at OBO. DE, drain efficiency; OBO, output back-off; VSWR, voltage standing wave ratio.

$$I_{p1} = \begin{cases} 0, v_{in} < V_{max}/3 \\ I_{max} \cdot (1.5 \cdot v_{in} - 0.5), V_{max}/3 \le v_{in} < V_{\max} \\ I_{max}, v_{in} \ge V_{max} \end{cases} \tag{6}$$

$$I_{p2} = \begin{cases} 0, v_{in} < V_{max}/2 \\ I_{max} \cdot (2 \cdot v_{in} - 1), V_{max}/2 \le v_{in} < V_{\max} \\ I_{max}, v_{in} \ge V_{max} \end{cases} \tag{7}$$

According to Golestaneh et al. (2013), in Eq (5), (6) and (7), the high-efficiency range when the load is matched can be derived as 9.5 dB when the load is matched.

To analyze the operation of DPA of this design under condition of impedance mismatch, we change the load impedance Z_L on the circle of equal reflection coefficients with voltage standing wave ratio (VSWR) = 2:1. In this situation, the operating state of the CG voltage and current is beyond the extent that can be described by the linear current model, so we introduce the nonlinear current model used in Chen et al. (2022); Pang et al. (2024). Based on the linear current relationship described in Eqs (5), (6),

(7), and the non-linear current model introduced in Chen et al. (2022); Pang et al. (2024), the nonlinear current model for the three-stage DPA can be established as

$$I_{c,non} = \begin{cases} I_{\max} \cdot v_{in} \cdot \tanh(v_{ds}/v_{knee}), \\ \quad 0 \le v_{in} < V_{\max} \\ I_{\max} \cdot \tanh(v_{ds}/v_{knee}), \\ \quad v_{in} \ge V_{max} \end{cases} \tag{8}$$

$$I_{p1,non} = \begin{cases} 0 \quad , 0 \le v_{in} < V_{\max}/3 \\ I_{\max} \cdot (1.5 \cdot v_{in} - 0.5) \cdot \tanh(v_{ds}/v_{knee}), \\ \quad V_{\max}/3 \le v_{in} < V_{\max} \\ I_{\max} \cdot \tanh(v_{ds}/v_{knee}), \\ \quad v_{in} \ge V_{max} \end{cases} \tag{9}$$

$$I_{p2,non} = \begin{cases} 0 \quad , 0 \le v_{in} < V_{\max}/2 \\ I_{\max} \cdot (2 \cdot v_{in} - 1) \cdot \tanh(v_{ds}/v_{knee}), \\ \quad V_{\max}/2 \le v_{in} < V_{\max} \\ I_{\max} \cdot \tanh(v_{ds}/v_{knee}), \\ \quad v_{in} \ge V_{max} \end{cases} \tag{10}$$

where v_{ds} and v_{knee} refer to the drain-source voltage and knee voltage at the turn-on point of the field effect transistor, respectively. Using the nonlinear current model (8) (9) (10) instead of the CGs in Fig. 2, the voltage-current relationship at each port of the four-port network shown in Fig. 3(a) can still be expressed by Eq. (2).

Once the current behaviour is established, the operating state of the proposed DPA can be represented by the model shown in Fig. 3(b), grounding the control port, i.e. without making any changes to the original three-stage DPA circuit structure. In this case, the load impedance Z_L is mismatched and the phase is rotated on the circle of equal reflection coefficients with VSWR=2:1 to analyze the variation of output power and drain efficiency (DE) in the mismatched condition, and at the same time compare it

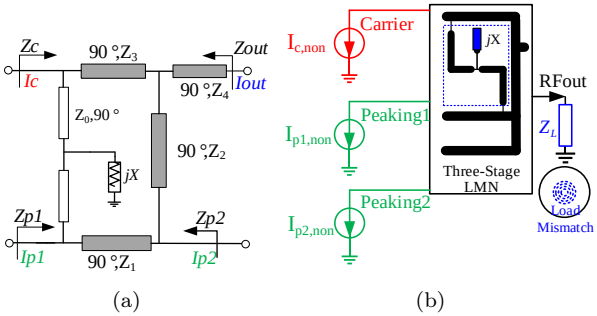


Figure 5 Proposed 1-D control LMN: (a) theoretical block diagram and (b) schematic to analyze the three-stage Doherty performance under load mismatch conditions using nonlinear current models. LMN, load modulation network.

with the matched condition. The variation of output power and DE under the load matched and mismatched conditions are presented in Fig. 4(a). It can be observed that the overall efficiency of the DPA can still able to maintain the three-stage Doherty characteristic under load mismatch, but a high-efficiency range can only be achieved only in a part of the phase interval of VSWR=2:1. From Fig. 4(a) we can see that compared to the load-matched condition, the saturated output power under mismatch conditions decreases by 2 dB, and the DE shows different variations depending on the VSWR phase. Nevertheless, the three-stage Doherty operation can be maintained under load mismatch conditions, while the efficiency performance decreass significantly in some VSWR phase condtions.

To better present the effect of mismatch on the OBO efficiency of the three-stage DPA, the back-off efficiencies under different VSWR phase conditions are plotted in Fig. 4(b). From Fig. 4(b), it is evident that the DPA can still able to maintain high efficiency at the OBO point, especially when the VSWR phase is within the range of [0°, 90°] and [270°, 360°], with back-off DE above 50%. However, when the VSWR phase is within the range of [120°, 240°], the back-off efficiency of the DPA under mismatch condition is lower than 43%, so the circuit structure might need to be adjusted appropriately.

2.2 Proposed 1-D control for three-stage DPA against load mismatch

From the above analysis, we can see that the three-stage DPA itself has a certain degree of load mismatch resilience. However, this resilience does

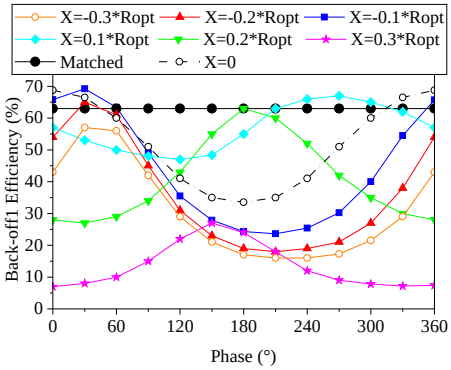


Fig 6 Theoretical DE at OBO1 versus phase with different X of 1-D control. DE, drain efficiency; OBO1, output back-off1.

not guarantee that the three-stage DPA maintains a high back-off efficiency in all VSWR phase intervals. To improve the mismatch resilience, the architecture shown in Fig. 3(a) has been modified, by adding a control network to reconfigure the output network of the three-stage DPA with one circuit variable. Based on the architectural nuances, the resilience of the three-stage DPA against load mismatch can be attributed to the distinct impedance variations exhibited by the carrier and peaking PA1 under such conditions. This divergence in impedance behavior stems from the quarter-wavelength TL spacing between the two sub-PAs, resulting in the formation of load mismatch resilience in the overall three-stage DPA configuration. Therefore, it is natural to consider further enhancing the mismatch resilience by adjusting the impedance characteristics of these two sub-PAs. As shown in Fig. 5(a), the modified 1-D reconfigurable three-stage DPA is realized by adding the reactance jX to the outputs of the carrier and peaking PA1 through two 90° TLs with a characteristic impedance of Z_0. In this scenario, the voltage-current relationship of the proposed DPA is similar to that described in Eq. (2), but the Z-parameter matrix of the modified LMN will be changed as follows:

$$\hat{\mathbf{Z}}\mathbf{2} = R_{opt}\begin{bmatrix} 0 & \frac{-j2}{1+\beta} & 0 & 0 \\ \frac{-j2}{1+\beta} & 0 & \frac{+j}{1+\beta} & \frac{-j\frac{5}{2\sqrt{3}}}{1-\beta} \\ 0 & \frac{+j}{1+\beta} & 0 & \frac{-j\frac{5}{4\sqrt{3}}}{\beta} \\ 0 & \frac{-j\frac{5}{2\sqrt{3}}}{1-\beta} & \frac{-j\frac{5}{4\sqrt{3}}}{\beta} & 0 \end{bmatrix}, \beta = \frac{2x}{z_0^2} \tag{11}$$

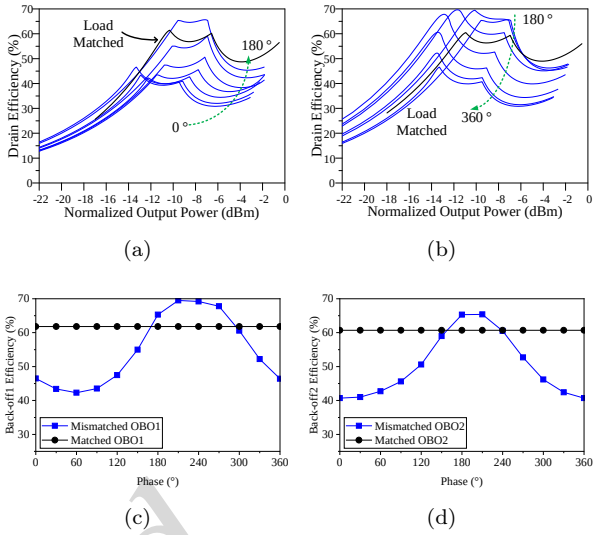


Fig 7 Theoretical DE versus normalized output power at inductive reactance jX modulation: (a) [0°,180°], (b) [180°,360°], (c) DE at OBO1 and (d) DE at OBO2. DE, drain efficiency; OBO1, output back-off1; OBO2, output back-off2.

where z_0 and x are the normalized values of Z_0 and X for R_{opt}.

Using a similar method illustrated in Section 2.1 with the nonlinear current models, we can build a simulation schematic, as shown in Fig. 5(b), to analyze the DPA operation under load mismatch condition when considering the proposed 1-D control method. Similarly, the load impedance is varied with the phase when VSWR = 2:1, and the results under the load matched condition would also be given as a comparison. It is important to note that the effect of different control reactance under load mismatch will be discrepant for the proposed DPA. As shown in Fig. 6, under the condition of load mismatch condition, selecting different X values will result in different variations of the first back-off DE. Since the situation is similar for the second back-off point, it will not be repeated. It can be seen that for values of X between -0.1R_{opt} and 0.1R_{opt}, there is a significant improvement in the corresponding regions compared to the original conditions. In the following analysis, we will select two different sets of values as examples to illustrate the impact of different jX on the proposed DPA.

Firstly, the variation of DE versus output power under load mismatch condition for inductive reactance jX is obtained, as shown in Fig. 7. In this scenario, X takes the value of 0.14 R_{opt}, with Z_0 =

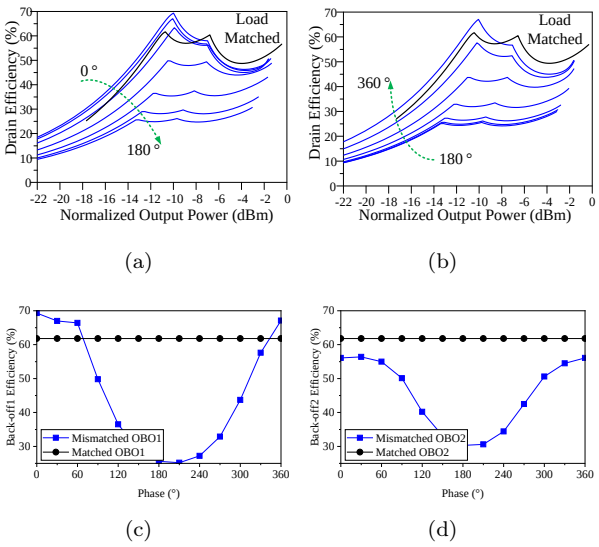


Fig 8 Theoretical DE versus normalized output power at capacitive reactance jX modulation: (a) [0°,180°], (b) [180°,360°] (c) DE at OBO1 and (d) DE at OBO2. DE, drain efficiency; OBO1, output back-off1; OBO2, output back-off2.

R_{opt}. Compared to the results obtained in Section 2.1, there are significant changes in the VSWR phase range corresponding to high-efficiency performance, while the saturated output power is just slightly reduced in both [0, 60°], [300°, 360°] VSWR phase conditions. Defining the turn-on point for peaking1 as output back-off1 (OBO1) and the turn-on point for peaking2 as output back-off2 (OBO2), Fig. 7(c) and Fig. 7(d) plots the performance of DE at OBO points for different VSWR phase changes after adding the capacitive reactance, which more intuitively demonstrates that there is a great improvement in the efficiency throughout the VSWR phase range of [120°, 240°]. More than a 20% efficiency improvement can be achieved compared to the initial three-stage DPA setting. However, at other phase conditions, there is a significant reduction in efficiency compared to the initial DPA.

Secondly, we consider adjusting jX to capacitive to observe the change in saturated output power and DE under different VSWR phase conditions. By tuning the control reactance X in the opposite direction towards a capacitive reactance of -0.04R_{opt}, a similar simulation is performed again. The simulation produces diverse DE outcomes with varying VSWR phases, monitoring the DE precisely at the OBO points, as shown in Fig. 8(c) and Fig. 8(d). As clearly depicted in Fig. 8, there is a discernible

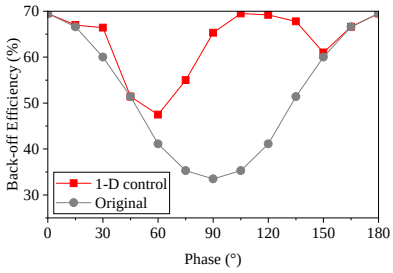


Fig 9 Theoretical DE at OBO1 versus phase with versus without 1-D control. DE, drain efficiency; OBO1, output back-off1.

reduction in the saturated output power within the angular range of [120°, 240°]. Conversely, a remarkable improvement in efficiency is observed within [0°, 60°], whereas a substantial decrease in efficiency is evident at other phase angles.

From the above analysis, we can see that by switching the control reactance to zero (ground connection) or different jX of 1-D control, the efficiency performance exhibited by the proposed three-stage DPA under load mismatch conditions can be significantly improved. Comparing Fig. 8 and Fig. 7, we can see that using different jX in different phase ranges can achieve better mismatch resistance. To more visually see the impact of 1-D reconfiguration on OBO1 efficiency, the comprehensive outcome of this control method is graphically depicted in Fig. 9. Compared to the case where no adjustments are made to the circuit, reconfiguration through 1-D circuitry can lead to a significant increase in circuit performance in the presence of mismatches. By 1-D switching different reactance at the control port, it becomes feasible to regulate the DE to surpass 47% even in the presence of a load mismatch. Meanwhile, over 60% back-off efficiency can be obtained in most VSWR phase conditions.

3 Circuits design

In the previous section, the theoretical feasibility of the proposed 1-D reconfigurable three-stage DPA architecture for resilience against load mismatch was established. This section aims to validate this theory by designing a three-stage DPA operating at 2 GHz, adhering to the aforementioned architecture. The target design specifications include a high-efficiency OBO range of 9.5 dB for matched loads, with an anticipated maintenance of a high-efficiency range of 8 dB under VSWR conditions of

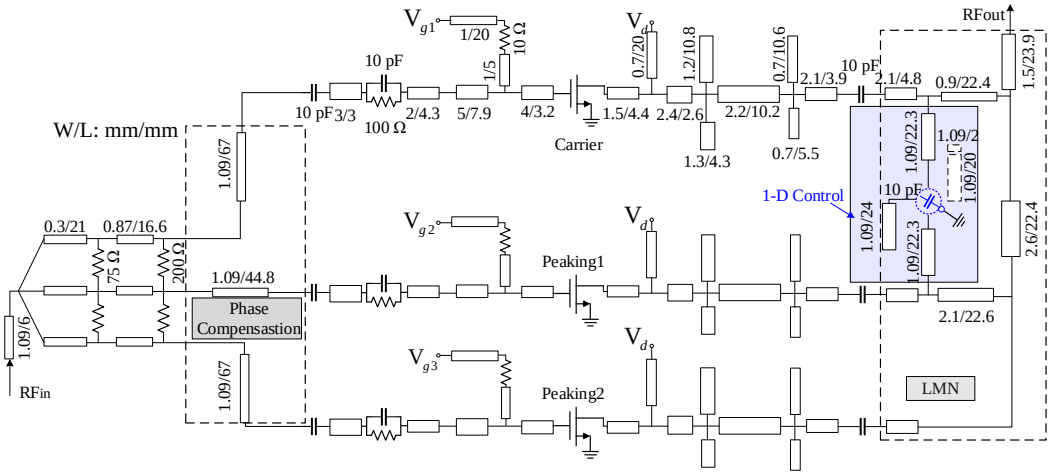


Fig 10 Circuits details of the proposed three-stage DPA. DPA, Doherty power amplifier; LMN, load modulation network.

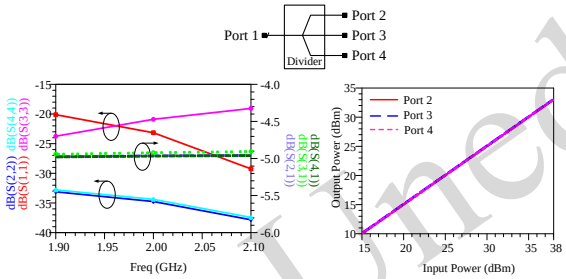


Fig 11 Simulated S-parameters and output power versus input power of three-way divider.

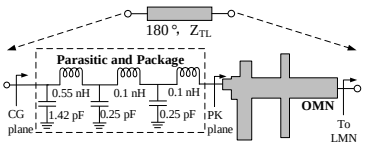


Fig 12 Equivalent OMN Containing Package Parameters. OMN, output matching network.

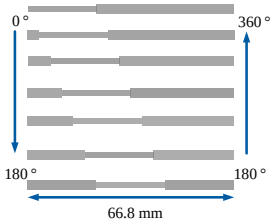


Fig 13 VSWR = 2:1, phase adjustment from 0° to 360°. VSWR, voltage standing wave ratio.

2:1. For this design, we have chosen the GaN transistor CG2H40010F from Wolfspeed to serve as the carrier PA and peaking PAs. These transistors have a maximum output current, II_{max} of 1.5 A, and all three sub-PAs operate with the same drain voltage of 28 V. When operating in class B, the optimal output impedance of the PA, R_{opt} is 32 Ω. The actual substrate used for fabrication is Rogers 4350B, which boasts a dielectric constant ε_r of 3.66 and a thickness of 20 mil, ensuring high-performance and reliability for the DPA design.

Fig. 10 provides a detailed insight into the designed DPA circuit, highlighting its specific dimensions. A two-stage three-way power divider serves as the initial component, effectively dividing the input signal's power into three equal parts. From Fig. 11, it can be seen from the simulation of passive and active respectively that the designed power divider has good performance at the operating frequency. However, due to the varying turn-on points of the three sub-PAs, which induce a phase difference in the currents, it is necessary to incorporate corresponding phase compensation lines before the input matching networks (IMNs). The sizing of these compensation lines necessitates careful consideration of the subsequent layout, while ensuring that the carrier PA and peaking PA2 maintain a 90° phase difference from peaking PA1. The IMN design has been optimized with a T-shaped structure, and capacitors and resistors have been incorporated to guarantee circuit stability. For the sake of simplicity, an identical IMN has been employed for all three sub-PAs.

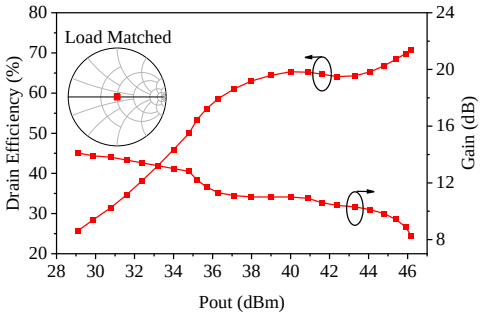


Fig 14 Simulated DE and gain versus output power in matched load condition. DE, drain efficiency.

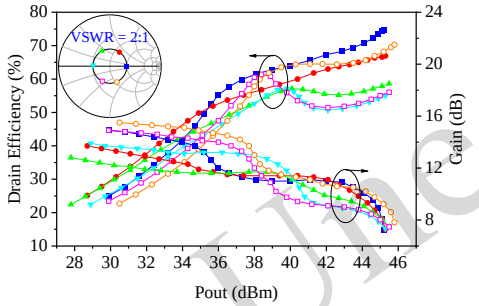


Fig 15 Simulated DE and gain versus output power under different load mismatch condition when VSWR=2:1. DE, drain efficiency; VSWR, voltage standing wave ratio.

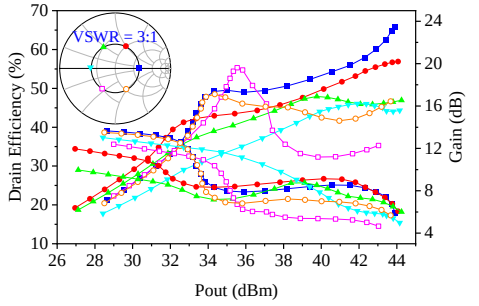


Fig 16 Simulated DE and gain versus output power under different load mismatch condition when VSWR=3:1. DE, drain efficiency; VSWR, voltage standing wave ratio.

The output matching networks (OMNs) needs to match the optimal impedance of the transistor at the CG plane to the characteristic impedance of the LMN, while absorbing the parasitic and package parameters, as shown in Fig. 12. Since the impedance of the transistor output and the characteristic impedance of the LMN are both R_{opt}, OMN together with the package parameters, is equivalent to a 180° network with an equivalent characteristic impedance $Z_{TL} = R_{opt}$. To enhance the efficiency of the designed DPA, four open TLs with varying electrical lengths have been integrated for harmonic suppression. All three sub-PAs employ identical OMNs. The LMN is designed using the structure discussed in Section II, comprising four 90° TLs. For realizing the proposed 1-D control, additional 90° TLs are positioned between the carrier PA and peaking PA1, which can be terminated to ground or a control reactance. By connecting to different reactances, distinct one-dimensional tuning effects can be achieved. In practical design, the different reactance is also realized using open circuit TLs with different electrical lengths. Considering the potential effects of the coupling of lines in the fabricated DPA will lead to inaccuracy in the measurement, a number of transmission lines with slightly different lengths have been added for tuning in the 1-D control section. Furthermore, leveraging the unique properties of 90° TLs, when the control port is grounded, the circuit reverts to an un-tuned state.

In order to measure the DPA performance with different phases when VSWR=2:1, it is necessary to design a peripheral part piece for impedance change and phase adjustment. Therefore, a 90° TL with a characteristic impedance of 70.7 Ω is first used to transfer the load impedance to 100 Ω, and then several transmission lines with different lengths are used to change the VSWR phase for different mismatch conditions. The layout of this mismatch tuner is shown in Fig. 13. A small capacitor is used for switching, which does not affect the results.

After designing the circuit, we need to build an EM-model of the entire circuit and observe the performance through harmonic balance simulation. Fig. 14 shows the variation of DE and gain with output power for the designed DPA when the load is matched. As can be seen from Fig. 14, when the 1-D control port is grounded, the DPA has a saturated output power of 46.3 dBm, DE of 70.8%

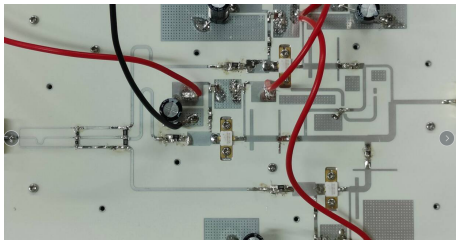


Fig 17 Photograph of the fabricated three-stage DPA. DPA, Doherty power amplifier.

at saturation, and can achieve 59.4% DE at 9.5 dB OBO, with load matching to 50 Ω.

Next, the performance of the designed DPA under mismatch conditions is simulated. With 1-D circuit reconstruction, the DPA can select the optimal case at different phases. When VSWR = 2:1, the DPA achieved a saturated output power of 45.2-45.8 dBm, saturated DE of 55-74.6%, saturated gain of 7.2-7.8 dB, and 8 dB back-off DE of 49.6-59.8%, as shown in Fig. 15. It can be seen that the DPA maintains good performance under load mismatch conditions, both in output power and DE. The difference between the saturated output power of the DPA in the matched and mismatched states $\leq$ 1.5 dB. The DPA still exhibits good performance in the presence of load mismatch compared to when it is matched, thus confirming its resilience under load mismatch conditions.

For a clearer comparison of DPA performance under higher mismatch conditions, we simulated the DE and gain when VSWR = 3:1, and mismatch resistant property is still demonstrated compared to the case without 1-D control, but with more performance degradation. Based on the theory above, it is reasonable to think that taking more stages of DPA or more complex control parts may be able to achieve greater load mismatch resilience under the higher mismatch conditions. Since the same type of article is designed under VSWR = 2:1, we use VSWR = 2:1 to design for comparison and overall performance considerations. The DPA circuits will be fabricated and measured then.

4 Measurement results

The photo of the fabricated three-stage DPA is shown in the Fig. 17. The three sub-PAs use the same drain supply voltage of 28 V. Depending on the turn-on sequence, the gate voltage is set to -2.8 V for the carrier PA, -4.5 V for the peaking PA1, and

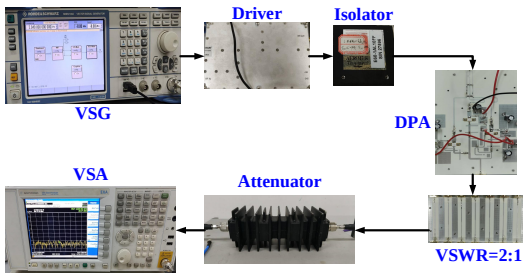


Fig 18 Measurement setup for testing the proposed DPA. DPA, Doherty power amplifier; VSA, vector spectrum analyzer; VSG, vector signal generator; VSWR, voltage standing wave ratio.

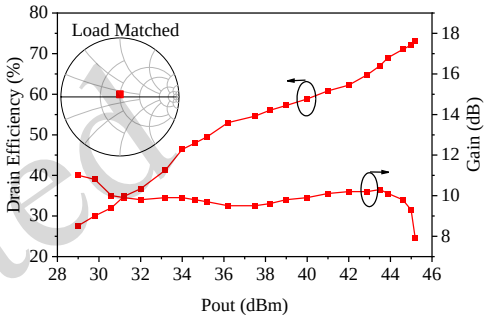


Fig 19 Measured DE and gain versus output power of the fabricated DPA for matched load condition. DE, drain efficiency; DPA, Doherty power amplifier.

-6 V for the peaking PA2, with a quiescent current of 60 mA. Similar to the simulation, the fabricated DPA will be tested in both matched and mismatched states.

Fig. 18 shows the platform used for measurement. The input signal is generated by a vector signal generator (VSG) and through a driver and isolator, the signal is fed into DPA through a driver and isolator. When the DPA is measured for a matched load, its output is connected to an attenuator and finally the results are displayed on the vector spectrum analyzer (VSA). When the DPA is measured under mismatch conditions, a designed VSWR tuner is used between the DPA output and attenuator to adjust the impedance and VSWR phase to achieve different mismatch conditions. To better demonstrate the performance of the DPA, both continuous wave (CW) and modulated measurements are performedy.

4.1 CW signal measurements

The three-stage DPA is initially assessed using continuous-wave (CW) signals. Under matched load conditions, the output impedance is set to 50 Ω, and

Table 1 Performance comparison of recently published PAs with load mismatch adaptability.

Ref.	This work		Gonçalves et al. (2022) 2022		Shi et al. (2023) 2023		Guo et al. (2023) 2023		Pang et al. (2024) 2023	
Freq (GHz)	2		3.6		2.4		2.1		2.0	
Load (Z_0/VSWR)	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1
Control Variables	1-D		2-D		3-D		1-D		3-D	
P_{sat} (dBm)	45.2	43.4-45.3	43.5	42.6-43.4	43.4/43.7	41.5-43.3	42*	39.1-40.9	46.4/46.7	44.8-46.3
DE_{sat} (%)	73.1	56.5-66.5	64	49-64	69.1/70.8	52.8-60.7	72*	60.1-66.4	70.3/72.2	50.2-65.8
OBO (dB)	9.5	8	5		6		10		9	
DE@OBO (%)	51.0	47.0-55.1	53	35-46	>60	50.1-62.5	64*	43.0-62.8	62.8/60.7	47.8-56.7

* - Graphically estimated, P_{sat} - saturation output power, DE_{sat} - saturation drain efficiency, OBO - output power back-off.

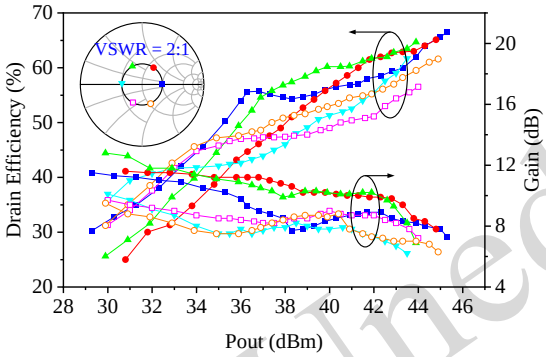


Fig 20 Measured DE and gain versus output power under different load mismatch condition. DE, drain efficiency; VSWR, voltage standing wave ratio.

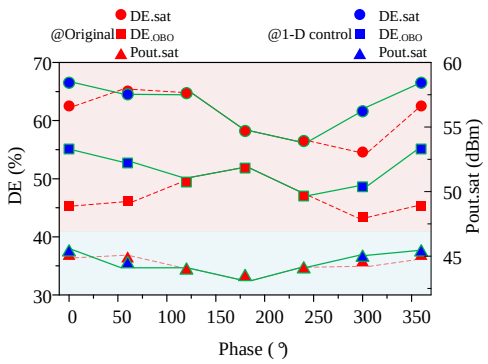


Fig 21 Measured drain efficiency and gain versus output power under different load mismatch condition when VSWR = 2:1. DE, drain efficiency; VSWR, voltage standing wave ratio.

the 1-D control port is grounded, indicating that the circuit is not actively regulated. Consequently, the DE and gain versus output power at this particular moment are depicted in Fig. 19. Upon reaching saturation, the DPA demonstrates an output power of 45.2 dBm, accompanied by DE of 73.1% and gain of 7.9 dB, and the DE maintains 51.0% at 9.5 dB back-off. However, when comparing these measured results to the simulations, a certain degree of performance degradation is observed. This degradation could be attributed to the intricate complexity of the circuit design and the inevitable discrepancies in phase and harmonic behavior that arise due to the inherent gap between simulation and actual physical conditions. Nevertheless, the fabricated DPA continues to exhibits a large efficiency range.

When assessing the performance of the DPA under load mismatch conditions, the 1-D control is then employed to optimize the circuit. By adjusting the reactance at the 1-D control port, the output power at saturation can be elevated to 43.4-45.3 dBm, with a DE ranging from 56.5% to 66.5%, a gain ranging from 6.2 dB to 7.8 dB, and at 8 dB OBO, a DE of 47%–55.1%. Fig. 20 illustrates the variation in DE and gain of the DPA with respect to output power under varying mismatch conditions. As shown in Fig. 20, the DPA responds differently to 1-D control under diverse phase conditions during load mismatch. This overall trend aligns with the analysis presented in Section II and further validates the necessity of incorporating 1-D control in the design of a three-stage DPA.

To further illustrate the performance of the DPA under mismatch conditions, and better demonstrate the usefulness of 1-D reconfigured circuits, test results using 1-D reconfiguration are compared to those of the initial circuits. Fig. 21 is presented, highlight-

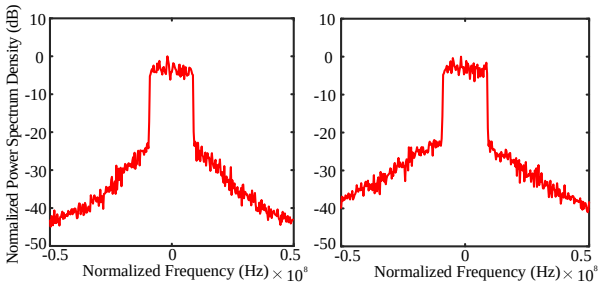


Fig 22 Output spectrum of the proposed DPA with load mismatch. (a) 30° and (b) 90° with 1-D control. DPA, Doherty power amplifier.

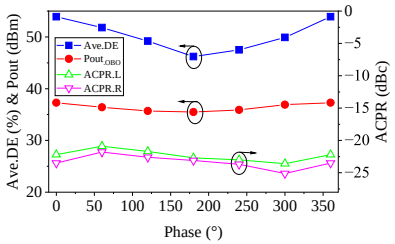


Fig 23 Average drain efficiency, output power and ACPR over 2:1 VSWR under modulated signal stimulation, with 1-D control. ACPR, adjacent channel power ratio; DE, drain efficiency; VSWR, voltage standing wave ratio.

ing the saturated output power, saturated DE, and the DE at 8 dB OBO for various VSWR phases. It also depicts the performance of the DPA across different modes of 1-D control. By comparing these performances, the optimal mode of 1-D control is identified and connected with a green solid line in the figure. The selection of the DPA's 1-D control mode is based on its performance. Specifically, within the VSWR phase range of [120°, 240°], the DPA's DE is better in its original state with the 1-D control port grounded. Additionally, for the VSWR phase ranges of [0°, 100°] and [260°, 360°], switching to the jX mode enables the DPA to achieve a superior operating state under mismatch conditions.

In summary, the introduction of the proposed 1-D control reconfiguration has allowed the fabricated DPA to achieve a saturated output power ranging from 43.4 dBm to 45.3 dBm under load mismatch conditions, while maintaining a saturated DE of 56.5 to 66.5%. Notably, even at an output power back-off of 8 dB, the DE remains stable at 47 to 55.1%. The negligible difference in saturated output power, ≤ 2 dB, between the matched and mismatched states of the DPA suggests that this three-stage design with 1-D control exhibits good resilience against load mismatch.

4.2 Modulated signal measurements

To demonstrate the performance of the fabricated three-stage DPA in practical wireless communication applications, the DE and adjacent channel power ratio (ACPR) of the DPA at the OBO point are measured using a modulated signal with a bandwidth of 20 MHz and a peak-to-average ratio (PAPR) of 8 dB.

At an average output power of 35.2 dBm, the DPA exhibited an average DE of 46.7% and an ACPR better than -24.4 dBc. Subsequently, under the load mismatch condition with a VSWR of 2:1, the DPA's performance was measured across various VSWR phase points. For illustrative purposes, the output spectra corresponding to VSWR phase angles of 60° and 180° are shown in Fig. 22.

To comprehensively illustrate the resilience of the DPA to load mismatch at VSWR = 2:1, Fig. 23 depicts the output power, average back-off DE, and ACPR as a function of the mismatch VSWR phase. Fig. 23 demonstrates that, upon switching the 1-D control port, the fabricated DPA achieves an average output power of 35.5-37.3 dBm, coupled with an average DE of 46.9%-53.9% and an ACPR better than -21 dBc.

4.3 Performance Comparison

Table 1 provides a comparative comparison of the proposed 1-D reconfigurable three-stage DPA with load mismatch resilience, against similar types of power amplifiers (PAs) reported in recent years. Upon comparing key performance metrics such as saturated output power, high-efficiency range, DE, and control variables, it becomes evident that the proposed DPA achieves comparable performance under load mismatch conditions using a lower-dimensional circuit reconfiguration approach. This underscores the effectiveness and simplicity of the proposed design.

5 Conclusions

In this paper, the load mismatch resilience of three-stage DPA is analyzed based on nonlinear current models. To further improve the mismatch resilience, a novel three-stage DPA with very simple 1-D circuits control method is then proposed. A DPA

operating at 2 GHz was designed to verify the proposed method and architecture. The designed DPA has a 9.5 dB OBO DE of 51% for matched load and maintains DE of 47%-55.1% at 8 dB OBO against load mismatch when VSWR = 2:1. The proposed three-stage DPA architecture with 1-D control offers a brand-new solution to provide load mismatch insensitivity with a very simple circuit configuration.

Contributors

Yi ZHANG and Jingzhou PANG designed the research. Yi ZHANG drafted the paper. Shuang LIU, Yujie HAN, Meng REN and Hanhui LIN helped organize the paper. Jingzhou PANG revised and finalized the paper.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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