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SHORT CIRCUIT CURRENT LIMITER IN AC NETWORK

WU Zhao-lin(吴兆麟), CHEN Ping-ping(谌平平), TAN Ling-yun(谭凌云), JIANG Dao-zhuo(江道灼)

(*State Key Laboratory of Power Electronics, Zhejiang University, Hangzhou 310027, China*)

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Abstract: Short circuit is a serious fault in power network. Some novel circuit topologies of current limiter using power electronic technology have been developed, which can limit the fault current to any desired level without much penalty. The operating principle and control strategies of such current limiters are discussed in detail. Simulation and experimental results are given to verify the performance of the current limiter, which can meet the requirements set for locations of bus tie, feeder, as well as the main transformer in the distribution network.

Key words: short circuit protection, current limiter, solid state switchgear, solid state current limiter
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INTRODUCTION

Short circuit in power systems is a serious fault, which may damage the equipment in the system . It requires the protection system to switch off the very high level of fault current. The traditional method to limit the short circuit current level is to serially connect a limiting reactor in the system. However the consideration of voltage drop and power dissipation of the reactor in normal operation limits the effect of the reactor. Some new approaches for short circuit limiting had been proposed. The EPRI (Electrical Power Research Institute) in the USA carried out a series of investigations into the technologies, which may possibly be used as short circuit limiter. The results of the investigation (Slade et al., 1992; Smith et al., 1993) proposed that a limiter consisting of solid state device such as GTO (in Fig. 1) may be the best approach among other possible approaches . The reactor in Fig. 1 is bypassed by the GTOs in normal operation. If short circuit occurs the GTOs should be switched off very quickly before the short circuit current rises to a high level. It requires fast response of the protection system. When the GTOs are switched off, the reactor L is inserted into the fault circuit. The interrupted current in GTO will transfer to the reactor L with very large di/dt. A high frequency resonance will be excited which causes large over-voltage with very rapid dv/dt applied to the GTOs as well as other equipment in the system. To reduce the negative effect , the value of reactor used has to be limited. A traditional breaker S is also needed to finally switch off the limited short circuit current.

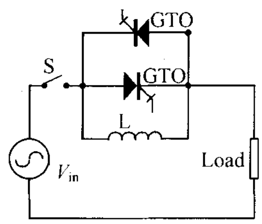

Fig.1 Current limiter with GTO

Another current limiting approach, the so called lossless resistor (LLR) was proposed (Chen et al., 1994; Chen et al., 1997), which uses IGBTs to form a bridge circuit and PWM technique in power electronics (Fig. 2). According to the authors, if the bridge is operating as rectifier and inverter alternately with modulating frequency higher than the mains frequency, the equivalent resistance of LLR can be controlled. The higher the modulating frequency is, the higher is the value of LLR. With much higher modulating frequency at short circuit, the equivalent value of LLR could be large enough to limit the short circuit current to a desired level.

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With such a topology, the modulated current in the positive half cycle is the same as that in the negative half cycle. The simple topology could not operate properly. Furthermore the switch devices in the bridge are operating in hard switching condition with relatively high modulating frequency and the switching loss is considerable even in normal condition. Abundant harmonics also exist with the approach.

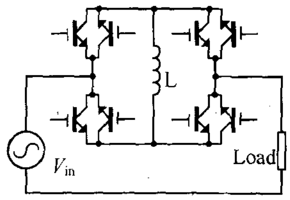

Fig.2 Current limiter (Chen et al., 1994)

A novel approach for current limiting was developed recently using power electronics technology, which can limit the current to any desired level without much penalty.

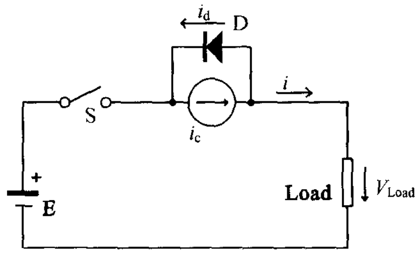

Fig.3 Current limiter in DC

In engineering practice, the current source i_c in Fig. 3 can be replaced by a reactor L. In this case the reactor, as well as the load, will be charged to its steady state through initial transients. In short circuit the current is limited by the reactor to rise slowly, which allows the protection system to respond easily and switch off the relatively low short circuit current. The reactor current will pass through the paralleled diode (as a freewheeling diode) after switching off without any transient overvoltage until the energy stored in the reactor is exhausted.

CURRENT LIMITER IN DC CIRCUIT

Fig. 3 shows the principle of the proposed current limiter. If the current of the current source i_c in normal condition keeps larger than the value of load current i, the diode D will always be at on state. Compared with the high voltage of the voltage source, the very low on state voltage drop of D will not affect the load voltage. In the case of short circuit, the source voltage acts on the diode D reversely and turns it off. The fault current rises instantaneously to and is limited by the current of the current source i_c. Once the value of i_c is set, the peak value of the short circuit current will be limited automatically to the value of i_c, which is easily switched off by the switch S.

CURRENT LIMITER IN AC CIRCUIT

The idea of DC current limiter can be extended to AC network as shown in Fig.4 (Wu, 1996; Wu et al., 1999). In Fig.4 b) with L_1, L_2 to replace the current source in Fig.4 a), the currents of L_1 and L_2 will reach the peak value of the sinusoidal load current after the initial stage transients have receded. If the power loss of the reactor and diode is negligible compared to the energy stored in the reactor, the current of each reactor keeps constant and the current in each diode always flows except during the peak of the load current (Fig.4c). Therefore the load current is theoretically sinusoidal and without distortion. If a short circuit fault occurs at any instant in a

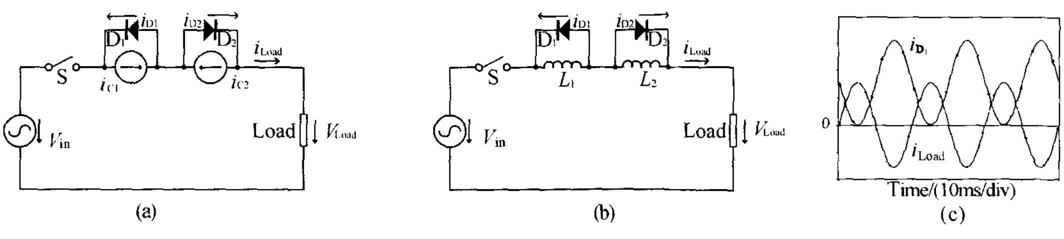

Fig.4 Current limiter in AC

(a) current limiter with current source; (b) current limiter with reactors; (c) current waveform period, one of the diodes must be reversely biased and the fault current will jump at normal load current amplitude to one of the inductors, then rises slowly due to the limiting function of the inductor which is automatically inserted into the fault circuit. If a pair of parallel reversely connected thyristors is used as S shown in Fig. 4, the fault current will be switched off automatically at the first point of source voltage across zero without transient. The longest fault current interruption time is one half cycle. Then the current in each reactor keeps flowing through its freewheeling diode. The reactance of the reactors L_1, L_2 can be designed such that the short circuit current should be limited to the desired level.

TOPOLOGY INNOVATION OF CURRENT LIMITER IN AC CIRCUIT

The current limiter topology (Fig. 4 b) used in AC circuit can be converted to a bridge topology shown in Fig.5, in which only one reactor is needed. In steady state the current in reactor L is almost equal to the amplitude of the sinusoidal load current. The two diodes function as freewheeling diodes and are always at on state (Fig. 5 b). With the two diodes at on state, the limiter has no obvious effect on the load current. If short circuit occurs, the fault current rises instantaneously to the value of the reactor current and one of the two diodes is reversely biased. The reactor L is inserted into the fault circuit automatically to limit the short circuit current. If the gate pulses are blocked in time the conducting thyristor will be turned off at the next point of source voltage across zero (Fig.5 c). The current in the reactor is then freewheeled through the two diodes. At short circuit, the fault current can be calculated as follows:

$$\because \quad v_{in} = L\frac{di_s}{dt} \quad i_s = I_0 + \Delta i$$

$$\therefore \quad \Delta i = \frac{1}{L}\int_{\omega t_0}^{\pi} \sin\omega t \, d\omega t = \frac{V_m}{\omega L}(1 + \cos\omega t_0)$$

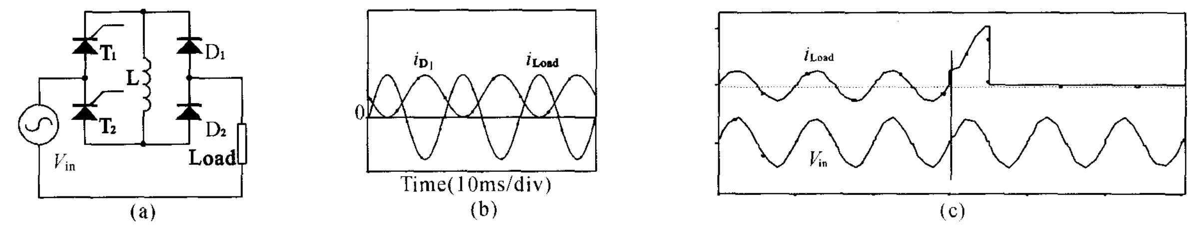

Fig.5 Bridge type current limiter
(a) circuit topology; (b) current waveform; (c) short circuit current limiting

Therefore the largest fault current occurred during short circuit at the voltage of source v_{in} across zero, when $t_0 = 0$. The peak value of the fault current i_{ps} in this case is:

$$i_{ps} = \frac{2V_m}{\omega L} + I_m$$

Here I_m is the reactor current just before short circuit, which is equal to the amplitude of steady state load current.

Considering the current limiter topology of the DC circuit in Fig. 3, the bridge circuit in Fig. 5 can be further improved as shown in Fig.6. Here a switch device such as GTO can be used as switch S and the diode D_0 is used as freewheeling diode. In steady state, due to the freewheeling diode, the bridge has no effect on the load current. In fault condition the gate controlled switch can be switched off within tens of microseconds. With such a short period the reactance of the limiting reactor L can be designed much smaller than that of the topology in Fig. 5. Also in Fig.6, when the fault current is switched off by the switch S, the current of reactor L is freewheeled by diode D_0. So the turning off of the switch S is easily without transient resonance activated by the limiting reactor.

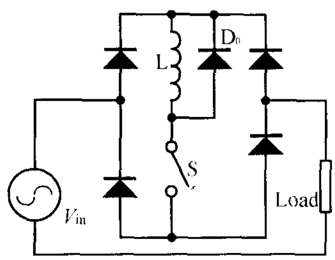

Fig.6 Fast interruption limiter

FURTHER IMPROVEMENT OF CURRENT LIMITER IN AC CIRCUIT

The topology of the current limiter in Fig.5 is a half-controlled bridge, in which the energy of the reactor can only be charged in but can not feed back to the source. If a full controlled bridge is used as shown in Fig.7, it can be operated as a rectifier or an inverter only depending on the trigger angle of the controlled pulses. Therefore, the energy stored in reactor L can flow bilaterally. In normal operating condition, with thyristors S_2 and S_3 fuctioning as freewheeling diodes with gate control pulses on them continuously, S_1 and S_4 are switched on and off alternately to keep load current flowing freely. So the operating performance is the same as that in Fig.5. In case of short circuit, say in the positive half cycle of source voltage at t_1 in Fig.8 a, the fault current rises quickly to the value of the reactor current and the thyristor S_3 is reversely biased to be switched off. In the period $t_1 - t_2$ the reactor is inserted in the fault circuit automatically with only S_1 and S_2 at on state. The fault current then rises slowly L until t_2. During $t_2 - t_3$ the gate trigger pulses are controlled such that the bridge operates as an inverter, so the energy stored in the reactor at t_2 feeds back to the voltage source. And the reactor current, as well as the fault current, falls to zero to automatically turn off the conducting thyristors.

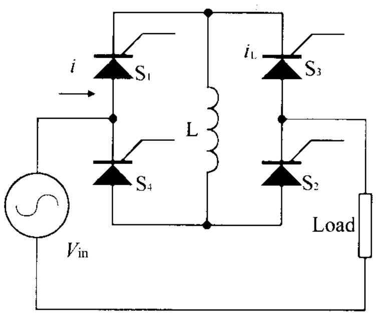

Fig.7 Full controlled bridge type limiter

In some cases, if time delay of switching off is required for coordination protection requirements, a special control strategy is developed. In Fig. 8 (a) after t_3, when the fault current falls to zero, the bridge is controlled to operate as a controllable rectifier with the trigger angle α greater than 90°. With only a reactor L at the DC side, the steady state short circuit current can be maintained as long as desired. In this case the desired short circuit current can be adjusted as the trigger angle α is controllable. The larger the α is, the smaller is the short circuit current even if the reactance of L is the same. It means that with the same desired current if α is greater than 90°, a smaller L can be used. When α is equal to 90°, the steady state fault current reaches its greatest value. With such a control strategy, multiple reclosing operation of the fault circuit can easily be realized without producing transients. When reclosing is required, the trigger angle α should be controlled such that initially it is very large, then it is decreased smoothly until the thyristors are fully conducting.

Fig.8 (a) is the simulation result of the current limiter operation. After interrupting the short circuit current, a reclosing operation is carried out successfully with the load current increasing smoothly to its normal value. Fig.8 (b)

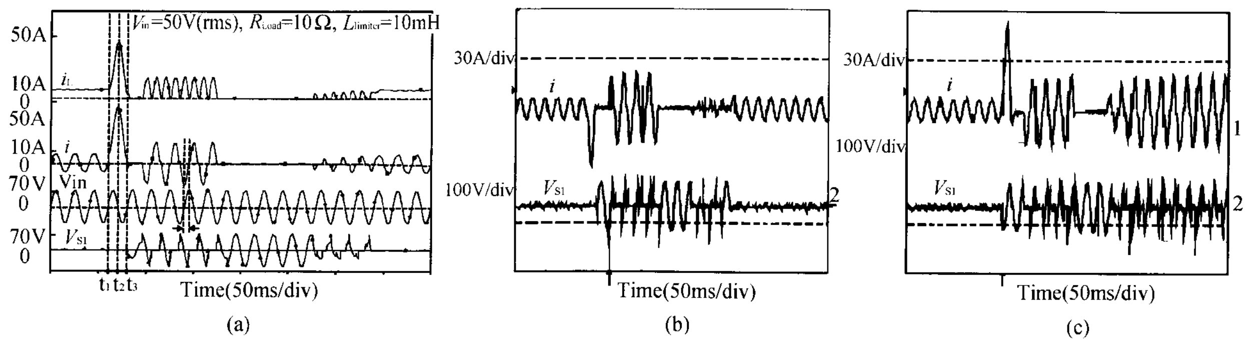

Fig.8 Short circuit protection

(a) simulation result; (b) experimental result of reclosing success; (c) experimental result of reclosing failure is the experimental result of the limiter, which verifies the simulation, as well as the theoretical analysis results discussed above. Fig. 8 (c) shows the experimental result of reclosing to a permanent fault. With the reclosing control strategy discussed above, reclosing of a fault circuit with very large current impulse can be fully avoided. It means that soft reclosing strategy can easily be realized.

APPLICATIONS OF CURRENT LIMITER IN DISTRIBUTION POWER SYSTEMS

In some papers (Slade et al., 1992; Smith et al., 1993) the applications of CLD (current limiting device) or CLID (current limiting interrupting device) to power systems and their requirements are discussed in detail with the typical diagram of substation in Fig.9. The proposed topology shown in Fig.5 can be applied as CLID at the bus tie location "1"(Fig.9) to limit the fault current through the bus to as low as desired and interrupt the fault current quickly within one half cycle to meet all requirements mentioned (Slade et al., 1992). If very fast interruption is required the topology proposed in Fig. 6 should be applied, with which the fault current can be interrupted within tens of microseconds. In this case with the limiting function of the reactor and so short duration of interruption, the fault current through the bus can not rise obviously from that just before the short circuit.

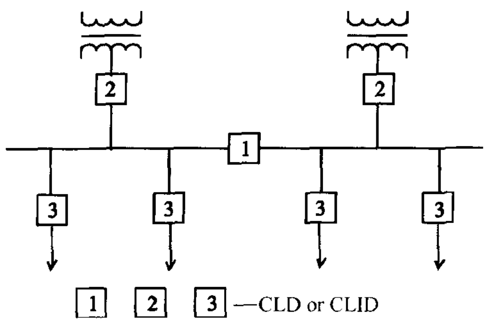

Fig.9 Diagram of distribution system

The control strategy of the current limiter topology proposed in Fig.7 is very flexible. This topology can be used as a CLID functioning the same way as that of the topology shown in Fig.5 (a). Furthermore, as a CLD or CLID, it can also maintain the limited fault current for as long as desired to meet all requirements for coordinating downstream and upstream protecting devices, including reclosing requirement. Therefore it can be used as CLD or CLID for application to any part of a distribution network (Fig.9) such as bus tie, feeder, and mains transformer.

CONCLUTIONS

More attention has been paid in recent year to the use of current limiting devices for limiting fault current in power networks. Some novel topologies of current limiter using power electronic technology are presented. Their operating principles, performances, and control strategies are discussed in detail. Simulations and experiments on prototype models were carried out to verify the analysis results. The novel CLDs and CLIDs proposed in this paper can meet all requirements concluded by EPRI (Slade et al., 1992; Smith et al., 1993) for CLD and CLID applied to distribution systems at locations of bus tie, feeders and mains transformers.

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